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Features

- **Incorporates the ARM926EJ-S™ ARM® Thumb® Processor**
  - DSP Instruction Extensions
  - ARM Jazelle® Technology for Java® Acceleration
  - 4 Kbyte Data Cache, 4 Kbyte Instruction Cache, Write Buffer
  - 265 MIPS at 240 MHz
  - Memory Management Unit
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- **Multi-layer AHB Bus Matrix for Large Bandwidth Transfers**
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- **One 32-KByte internal ROM, Single-cycle Access at Maximum Speed**
- **One 64-KByte internal SRAM, Single-cycle Access at Maximum Speed**
  - 4 Blocks of 16 Kbytes Configurable in TCM or General-purpose SRAM on the AHB Bus Matrix
  - Single-cycle Accessible on AHB Bus at Bus Speed
  - Single-cycle Accessible on TCM Interface at Processor Speed
- **2-channel DMA**
  - Memory to Memory Transfer
  - 16 Bytes FIFO
  - LInked List
- **External Bus Interface (EBI)**
  - EBI Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- **LCD Controller (for AT91SAM9RL64 only)**
  - Supports Passive or Active Displays
  - Up to 24 Bits per Pixel in TFT Mode, Up to 16 bits per Pixel in STN Color Mode
  - Up to 16M Colors in TFT Mode, Resolution Up to 2048x2048, Virtual Screen Support
- **High Speed (480 Mbit/s) USB 2.0 Device Controller**
  - On-Chip High Speed Transceiver, UTMI+ Physical Interface
  - Integrated FIFOs and Dedicated DMA
  - 4 Kbyte Configurable Integrated DPRAM
- **Fully-featured System Controller, including**
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer and Real-time Clock
- **Reset Controller (RSTC)**
  - Based on Two Power-on Reset Cells
  - Reset Source Identification and Reset Output Control
- **Shutdown Controller (SHDC)**
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- **Clock Generator (CKGR)**
  - Selectable 32768 Hz Low-power Oscillator or Internal Low-power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 12 MHz On-chip Oscillator for Main System Clock and USB Clock
  - One PLL up to 240 MHz

AT91 ARM Thumb Microcontrollers

AT91SAM9R64
AT91SAM9RL64

Summary

6289CS–ATARM–28-May-09

- – One PLL 480 MHz Optimized for USB HS
- **Power Management Controller (PMC)**
  - – Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - – Two Programmable External Clock Signals
- **Advanced Interrupt Controller (AIC)**
  - – Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - – One External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- **Debug Unit (DBGU)**
  - – 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
  - – Mode for General Purpose 2-wire UART Serial Communication
- **Periodic Interval Timer (PIT)**
  - – 20-bit Interval Timer plus 12-bit Interval Counter
- **Watchdog Timer (WDT)**
  - – Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- **Real-time Timer (RTT)**
  - – 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- **Real-time Clock (RTC)**
  - – Time, Date and Alarm 32-bit Parallel Load
  - – Low Power Consumption
  - – Programmable Periodic Interrupt
- **One 6-channel 10-Bit Analog-to-Digital Converter**
  - – Touch Screen Interface Compatible with Industry Standard 4-wire Sensitive Touch Panels
- **Four 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC and PIOD)**
  - – 118 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os for 217-ball BGA Package
  - – Input Change Interrupt Capability on Each I/O Line
  - – Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- **22-channel Peripheral DMA Controller (PDC)**
- **One MultiMedia Card Interface (MCI)**
  - – SDCard/SDIO 1.0 and MultiMediaCard™ 4.3 Compliant
  - – Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- **Two Synchronous Serial Controllers (SSC)**
  - – Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - – I²S Analog Interface Support, Time Division Multiplex Support
  - – High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- **One AC97 Controller (AC97C)**
  - – 6-channel Single AC97 Analog Front End Interface, Slot Assigner
- **Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
  - – Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - – Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
- **One Master/Slave Serial Peripheral Interface (SPI)**
  - – 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - – High-speed Synchronous Communications
- **One Three-channel 16-bit Timer/Counter (TC)**
  - – Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - – Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **Two Two-wire Interfaces (TWI)**
  - – Compatible with Standard Two-wire Serial Memories
  - – One, Two or Three Bytes for Slave Address
  - – Sequential Read/Write Operations

- – **Master, Multi-master and Slave Mode Operation**
- – **Bit Rate: Up to 400 Kbits**
- – **General Call Supported in Slave Mode**
- – **Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode Only (TWI0 only)**
- **SAM-BA® Boot Assistant**
  - – **Default Boot Program**
  - – **Interface with SAM-BA Graphic User Interface**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Required Power Supplies:**
  - – **1.08 to 1.32V for VDDCORE, VDDUTMIC, VDDPLLB and VDDBU**
  - – **3.0V to 3.6V for VDDPLLA, VDDANA, VDDUTMII and VDDIOP**
  - – **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM**
- **Available in a 144-ball BGA (AT91SAM9R64) and a 217-ball LFBGA (AT91SAM9RL64) Package**

1. Description

The AT91SAM9R64/RL64 device is based on the integration of an ARM926EJ-S processor with a large fast SRAM and a wide range of peripherals.

The AT91SAM9R64/RL64 embeds one USB Device High Speed Controller, one LCD Controller (for AT91SAM9RL64 only), one AC97 controller, a 2-channel DMA Controller, four USARTs, two SSCs, one SPI, two TWIs, three Timer Counter channels, a 4-channel PWM generator, one Multimedia Card interface and a 6-channel Analog-to-digital converter that also provides resistive touch screen management.

The AT91SAM9R64/RL64 is architectured on a 6-layer bus matrix. It also features an External Bus Interface capable of interfacing with a wide range of memory and peripheral devices.

Some features are not available for AT91SAM9R64 in the 144-ball BGA package.

Separate block diagrams and PIO multiplexing are provided in this document. Table 1-1 lists the features and signals of AT91SAM9RL64 that are not available or partially available for AT91SAM9R64. When the signal is multiplexed on a PIO, the PIO line is specified.

Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
AC97	Full	AC97FS AC97CK AC97TX AC97RX	PD1 PD2 PD3 PD4	-
EBI	Partial	D16-D31 NCS2 NCS5/CFCS1	PB16-PB31 PD0 PD13	-
LCDC	Full	LCDMOD LCDCC LCDVSYNC LCDHSYNC LCDDOTCK LCDDEN LCDD0-LCDD23	PC2 PC3 PC4 PC5 PC6 PC7 PC8-PC31	-

Table 1-1. Unavailable or Partially Available Features and Signals in AT91SAM9R64

Feature	Full/Partial	Signal	Peripheral A	Peripheral B
PWM	Partial	PWM2	PD5 and PD12	-
SPI	Partial	NPCS2 NPCS3	PD8	 PD9 and PD13
SSC1	Full	RF1 RK1 TD1 RD1 TK1 TF1	-	PA8 PA9 PA13 PA14 PA29 PA30
Touchscreen ADC	Partial	AD3YM GPAD4 GPAD5	PA20 PD6 PD7	-
TC	Partial	TIOA1 TIOB1 TCLK1 TIOA2 TIOB2	-	PC29 PC30 PC31 PD10 PD11
TWI	Full	TWD1 TWCK1	PD10 PD11	-
USART0	Partial	SCK0 RTS0 CTS0 DSR0 DTR0 DCD0 RI0	PA8 PA9 PA10 PD14 PD15 PD16 PD17	-
USART1	Partial	SCK1	-	PD2
USART2	Partial	SCK2 RTS2 CTS2	PD9 PA29 PA30	-
USART3	Partial	SCK3 RTS3 CTS3	-	PA20 PD3 PD4

2. Block Diagrams

Figure 2-1. AT91SAM9R64 Block Diagram

MASTER → SLAVE

System Controller

TST
FIQ
IRQ
DRXD
DTXD
PCK0-PCK1

AIC
DBGU
PDC

JTAG Selection and Boundary Scan

In-Circuit Emulator

ARM926EJ-S Processor

TDI TDO TMS TCK RTCK NTRST JTAGSEL

GNDUTMI VDDUTMII VDDUTMIC VBG DFSDP DFSDM DHSDP DHSDM BMS

HS UTMI Transceiver

USB Device HS

DMA

PLLRCA
XIN
XOUT

PLLA
12 MHz OSC
UPLL

PMC

TCM Interface ITCM DTCM | ICache 4 Kbytes | DCache 4 Kbytes

I   D

WDT   PIT

5-layer AHB Bus Matrix

XIN32
XOUT32

RC
32 kHz OSC

4 GPBREG
RTT

SRAM 64K Bytes

ROM 32K Bytes

Peripheral Bridge

Peripheral DMA Controller

2-channel DMA

SHDN
WKUP

SHDC

RTC

APB

VDDBU

POR

PDC | PDC | PDC | PDC | PDC | PDC | PDC

VDDCORE

POR

RSTC

NRST

MCI | TWI0 | USART0 USART1 USART2 USART3 | SPI | PWM | TC0 TC1 TC2 | SSC0 | 3-channel 10-bit ADC

PIOA   PIOB
PIOC   PIOD

DA0-DA3 CDA CK TWD0 TWCK0 CTS1 RTS1 RXD0-RXD3 TXD0-TXD3 NPCS0-NPCS1 SPCK MOSI MISO PWM0 PWM1 PWM3 TCLK0 TCLK2 TIOA0 TIOB0 TK0 TF0 TD0 RD0 RF0 RK0 TSADTRG AD0 AD1 AD2 TSADVREF VDDANA GNDAN

EBI

CompactFlash NAND Flash & ECC

SDRAM Controller

Static Memory Controller

D0-D15
A0/NBS0
A1/NBS2/NWR2
A2-A15
A16/BA0
A17/BA1
NCS0
NCS1/SDCS
NRD/CFOE
NWR0/NWE/CFWE
NWR1/NBS1/CFIOR
NWR3/NBS3/CFIOW
SDCK, SDCKE
RAS, CAS
SDWE, SDA10

NWAIT
A23-A24, A18-A20
A21/NANDALE
A22/NANDCLE
A25/CFRNW
NCS4/CFCS0
NCS3/NANDCS
CFCE1-CFCE2
NANDOE, NANDWE

AT91SAM9R64/RL64

AT91SAM9R64/RL64

Figure 2-2. AT91SAM9RL64 Block Diagram
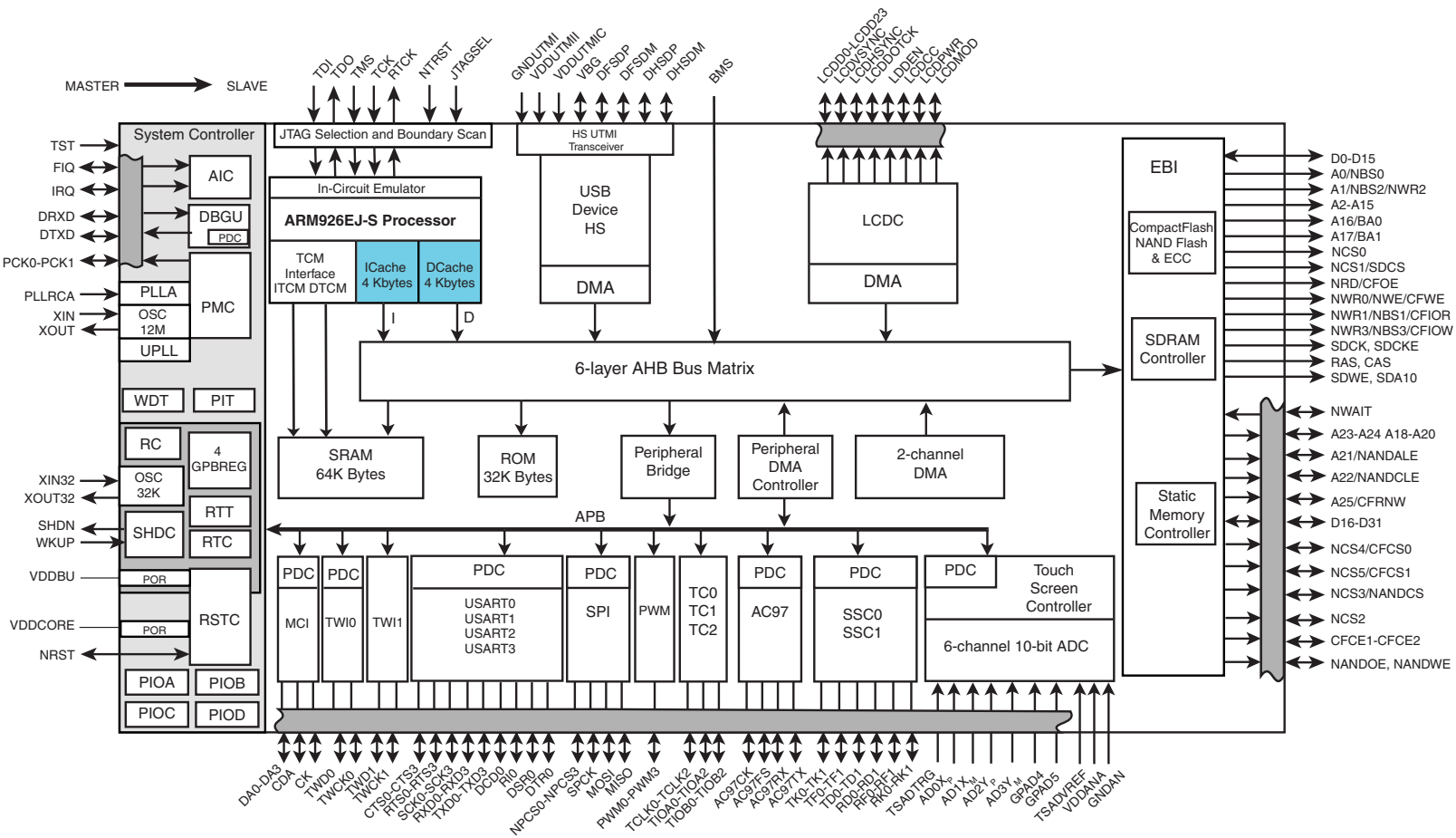
3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDIOM	EBI I/O Lines Power Supply	Power		1.65V to 3.6V
VDDIOP	Peripherals I/O Lines Power Supply	Power		3.0V to 3.6V
VDDUTMII	USB UTMI+ Interface Power Supply	Power		3.0V to 3.6V
VDDUTMIC	USB UTMI+ Core Power Supply	Power		1.08V to 1.32V
GNDUTMI	USB UTMI Ground	Ground		
VDDBU	Backup I/O Lines Power Supply	Power		1.08V to 1.32V
GNDBU	Backup Ground	Ground		
VDDPLLA	PLL Power Supply	Power		3.0V to 3.6V
GNDPLLA	PLL Ground	Ground		
VDDPLLB	UTMI PLL and OSC 12M Power Supply	Power		1.08 V to 1.32V
GNDPLLB	UTMI PLL and OSC 12M Ground	Ground		
VDDANA	ADC Analog Power Supply	Power		3.0V to 3.6V
GNDANA	ADC Analog Ground	Ground		
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
GNDCORE	Ground	Ground		
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
XIN32	Slow Clock Oscillator Input	Input		
XOUT32	Slow Clock Oscillator Output	Output		
VBG	Bias Voltage Reference	Analog		
PLLRCA	PLL A Filter	Input		
PCK0 - PCK1	Programmable Clock Output	Output		
Shutdown, Wakeup Logic				
SHDN	Shutdown Control	Output		Driven at 0V only. 0: The device is in backup mode. 1: The device is running (not in backup mode.)
WKUP	Wake-Up Input	Input		Accept between 0V and VDDBU
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NTRST	Test Reset Signal	Input	Low	Pull-up resistor.
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor
TST	Test Mode Select	Input		Pull-down resistor
BMS	Boot Mode Select	Input		Must be connected to GND or VDDIOP. No pullup resistor BMS = 0 when tied to GND BMS = 1 when tied to VDDIOP
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
Advanced Interrupt Controller - AIC				
IRQ	External Interrupt Input	Input		
FIQ	Fast Interrupt Input	Input		
PIO Controller - PIOA - PIOB - PIOC-PIOD				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD21	Parallel IO Controller D	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset. D16-D31 not present on AT91SAM9R64.
A0 - A25	Address Bus	Output		0 at reset
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller - SMC				
NCS0 - NCS5	Chip Select Lines	Output	Low	NCS2, NCS5 not present on AT91SAM9R64.
NWR0 - NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	CFCS1 not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Multimedia Card Interface MCI				
CK	Multimedia Card Clock	I/O		
CDA	Multimedia Card Slot A Command	I/O		
DA0 - DA3	Multimedia Card Slot A Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter USARTx				
SCKx	USARTx Serial Clock	I/O		SCKx not present on AT91SAM9R64.
TXDx	USARTx Transmit Data	I/O		
RXDx	USARTx Receive Data	Input		
RTSx	USARTx Request To Send	Output		RTS0, RTS2, RTS3 not present on AT91SAM9R64.
CTSx	USARTx Clear To Send	Input		CTS0, CTS2, CTS3 not present on AT91SAM9R64.
DTR0	USART0 Data Terminal Ready	I/O		Not present on AT91SAM9R64.
DSR0	USART0 Data Set Ready	Input		Not present on AT91SAM9R64.
DCD0	USART0 Data Carrier Detect	Output		Not present on AT91SAM9R64.
RI0	USART0 Ring Indicator	Input		Not present on AT91SAM9R64.
Synchronous Serial Controller - SSCx				
TD0 - TD1	SSC Transmit Data	Output		TD1 not present on AT91SAM9R64.
RD0 - RD1	SSC Receive Data	Input		RD1 not present on AT91SAM9R64.
TK0 - TK1	SSC Transmit Clock	I/O		TK1 not present on AT91SAM9R64.
RK0 - RK1	SSC Receive Clock	I/O		RK1 not present on AT91SAM9R64.
TF0 - TF1	SSC Transmit Frame Sync	I/O		TF1 not present on AT91SAM9R64.
RF0 - RF1	SSC Receive Frame Sync	I/O		RF1 not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
AC97 Controller - AC97C				
AC97RX	AC97 Receive Signal	Input		Not present on AT91SAM9R64.
AC97TX	AC97 Transmit Signal	Output		Not present on AT91SAM9R64.
AC97FS	AC97 Frame Synchronization Signal	Output		Not present on AT91SAM9R64.
AC97CK	AC97 Clock signal	Input		Not present on AT91SAM9R64.
Timer/Counter - TC				
TCLKx	TC Channel x External Clock Input	Input		TCLK1 not present on AT91SAM9R64.
TIOAx	TC Channel x I/O Line A	I/O		TIOA1, TIOA2 not present on AT91SAM9R64.
TIOBx	TC Channel x I/O Line B	I/O		TIOB1, TIOB2 not present on AT91SAM9R64.
Pulse Width Modulation Controller- PWMC				
PMWx	Pulse Width Modulation Output	Output		PWM2 not present on AT91SAM9R64.
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low	NPCS2, NPCS3 not present on AT91SAM9R64.
Two-Wire Interface - TWIx				
TWDx	TWIx Two-wire Serial Data	I/O		TWD1 not present on AT91SAM9R64.
TWCKx	TWIx Two-wire Serial Clock	I/O		TWCK1 not present on AT91SAM9R64.
Touch Screen Analog-to-Digital Converter				
GPAD0-GPAD5	Analog Inputs	Analog		GPAD4, GPAD5 not present on AT91SAM9R64.
$AD0X_P$	Touch Panel Right side	Analog		Multiplexed with AD0
$AD1X_M$	Touch Panel Left side	Analog		Multiplexed with AD1
$AD2Y_P$	Touch Panel Top side	Analog		Multiplexed with AD2
$AD3Y_M$	Touch Panel Bottom side	Analog		Multiplexed with AD3. Not present on AT91SAM9R64.
TSADTRG	ADC Trigger	Input		
TSADVREF	ADC Reference	Analog		
LCD Controller - LCDC				
LCDD0 - LCDD23	LCD Data Bus	Output		Not present on AT91SAM9R64.
LCDVSYNC	LCD Vertical Synchronization	Output		Not present on AT91SAM9R64.
LCDHSYNC	LCD Horizontal Synchronization	Output		Not present on AT91SAM9R64.
LCDDOTCK	LCD Dot Clock	Output		Not present on AT91SAM9R64.
LCDDEN	LCD Data Enable	Output		Not present on AT91SAM9R64.
LCDCC	LCD Contrast Control	Output		Not present on AT91SAM9R64.
LCDPWR	LCD panel Power enable control	Output		Not present on AT91SAM9R64.
LCDMOD	LCD Modulation signal	Output		Not present on AT91SAM9R64.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
USB High Speed Device				
DFSDM	USB Device Full Speed Data -	Analog		
DFSDP	USB Device Full Speed Data +	Analog		
DHSDM	USB Device High Speed Data -	Analog		
DHSDP	USB Device High Speed Data +	Analog		

4. Package and Pinout

The AT91SAM9R64 is available in a 144-ball BGA package. The AT91SAM9RL64 is available in a 217-ball LFBGA package.

4.1 144-ball BGA Package Outline

Figure 4-1 shows the orientation of the 144-ball BGA package.

Figure 4-1. 144-ball BGA Pinout (Top View)
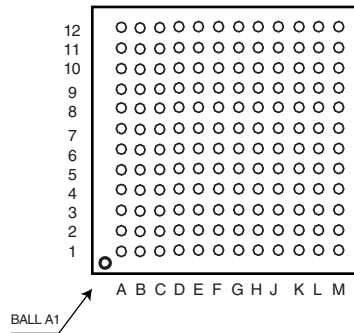
4.2   Pinout

Table 4-1.   AT91SAM9R64 Pinout for 144-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	DFSDM	D1	PLLRCA	G1	PB[10]	K1	A[5]
A2	DHSDM	D2	VDDUTMII	G2	PB[11]	K2	A[6]
A3	XIN	D3	NWR3/NBS3/CFIOW	G3	PB[12]	K3	A[13]
A4	XOUT	D4	NWR1/NBS1/CFIOR	G4	PB[9]	K4	A[15]
A5	XIN32	D5	JTAGSEL	G5	PB[13]	K5	RAS
A6	XOUT32	D6	GNDBU	G6	GND	K6	D[3]
A7	TDO	D7	TCK	G7	GND	K7	D[6]
A8	PA[31]	D8	PA[26]	G8	GND	K8	D[13]
A9	PA[22]	D9	PA[24]	G9	GNDUTMI	K9	VDDIOM
A10	PA[16]	D10	PA[13]	G10	VDDCORE	K10	VDDIOM
A11	PA[14]	D11	PA[6]	G11	VDDIOP	K11	D[11]
A12	PA[11]	D12	PD[20]	G12	VDDIOP	K12	PB[1]
B1	DFSDP	E1	GNDPLLA	H1	PB[14]	L1	A[7]
B2	DHSDP	E2	NWR0/NWE/CFWE	H2	PB[15]	L2	A[8]
B3	NC	E3	NRD/CFOE	H3	A[0]	L3	A[11]
B4	VDDPLLB	E4	NCS0	H4	A[2]	L4	A[16]
B5	GNDPLLB	E5	NCS1/SDCS	H5	SDA10	L5	SDWE
B6	TMS	E6	PB[2]	H6	D[1]	L6	D[4]
B7	RTCK	E7	NRST	H7	GND	L7	D[7]
B8	PA[27]	E8	BMS	H8	GND	L8	D[15]
B9	PA[21]	E9	PA[25]	H9	VDDIOM	L9	PC[1]
B10	PA[12]	E10	PA[15]	H10	SDCKE	L10	PC[0]
B11	PD[21]	E11	PA[5]	H11	VDDCORE	L11	PB[0]
B12	PA[10]	E12	PA[4]	H12	VDDIOP	L12	GNDANA
C1	VDDPLLA	F1	PB[5]	J1	A[4]	M1	A[9]
C2	VBG	F2	PB[6]	J2	A[1]	M2	A[10]
C3	VDDBU	F3	PB[7]	J3	A[3]	M3	A[12]
C4	SHDN	F4	PB[8]	J4	A[14]	M4	A[17]
C5	WKUP	F5	PB[3]	J5	CAS	M5	D[0]
C6	NTRST	F6	PB[4]	J6	D[2]	M6	SDCK
C7	TDI	F7	TST	J7	D[5]	M7	D[8]
C8	PA[28]	F8	VDDUTMIC	J8	D[12]	M8	ADVREF
C9	PA[23]	F9	PA[3]	J9	D[14]	M9	VDDANA
C10	PA[7]	F10	PA[2]	J10	VDDIOM	M10	PA[17]
C11	PD[19]	F11	PA[0]	J11	D[10]	M11	PA[18]
C12	PD[18]	F12	PA[1]	J12	D[9]	M12	PA[19]

4.3 217-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 217-ball LFBGA package.

Figure 4-2. 217-ball LFBGA Pinout (Top View)

AT91SAM9R64/RL64
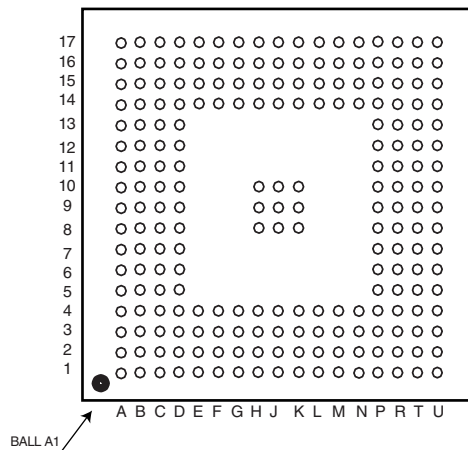
4.4 Pinout

Table 4-2. AT91SAM9RL64 Pinout for 217-ball LFBGA Package [1]

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	DFSDM	D5	SHDN	J14	PD[1]	P17	PC[11]
A2	DHSDP	D6	JTAGSEL	J15	PD[0]	R1	A[0]
A3	VDDPLLB	D7	NTRST	J16	PC[30]	R2	A[2]
A4	XIN	D8	BMS	J17	PC[31]	R3	A[7]
A5	XOUT	D9	TDO	K1	PB[14]	R4	A[10]
A6	GNDPLLB	D10	PA[30]	K2	PB[15]	R5	A[14]
A7	XOUT32	D11	GND	K3	PB[17]	R6	SDA10
A8	GND	D12	PA[23]	K4	PB[16]	R7	D[0]
A9	NRST	D13	PA[15]	K8	VDDUTMIC	R8	VDDIOM
A10	RTCK	D14	PA[12]	K9	VDDIOP	R9	D[6]
A11	PA[29]	D15	PA[8]	K10	PC[28]	R10	D[9]
A12	PA[26]	D16	PD[13]	K14	PC[25]	R11	NC
A13	PA[22]	D17	PD[16]	K15	PC[24]	R12	VDDIOM
A14	PA[14]	E1	GNDPLLA	K16	PC[26]	R13	PC[1]
A15	PA[10]	E2	NCS1/SDCS	K17	PC[27]	R14	PB[1]
A16	PD[20]	E3	NCS0	L1	PB[18]	R15	PC[5]
A17	PD[17]	E4	NWR3/NBS3/CFIOW	L2	PB[19]	R16	PC[6]
B1	DFSDP	E14	PD[15]	L3	PB[21]	R17	PC[7]
B2	DHSDM	E15	PD[14]	L4	PB[20]	T1	A[3]
B3	VBG	E16	PA[5]	L14	PC[21]	T2	A[5]
B4	NC	E17	PA[4]	L15	PC[20]	T3	A[8]
B5	NC	F1	NRD/CFOE	L16	PC[22]	T4	A[12]
B6	XIN32	F2	PB[2]	L17	PC[23]	T5	A[16]
B7	TST	F3	NWR0/NWE/CFWE	M1	PB[22]	T6	RAS
B8	GND	F4	PB[3]	M2	PB[23]	T7	D[2]
B9	TMS	F14	PA[1]	M3	PB[25]	T8	D[4]
B10	VDDCORE	F15	PA[0]	M4	PB[24]	T9	D[7]
B11	PA[28]	F16	PA[2]	M14	PC[17]	T10	D[10]
B12	PA[25]	F17	PA[3]	M15	PC[16]	T11	D[14]
B13	PA[21]	G1	GND	M16	PC[18]	T12	VDDANA
B14	PA[13]	G2	VDDIOM	M17	PC[19]	T13	PA[17]
B15	PD[21]	G3	PB[5]	N1	PB[26]	T14	PA[19]
B16	PD[19]	G4	PB[4]	N2	PB[27]	T15	PC[2]
B17	PA[9]	G14	PD[12]	N3	PB[29]	T16	PC[3]
C1	VDDPLLA	G15	PD[11]	N4	PB[28]	T17	PC[4]
C2	VDDUTMII	G16	PD[10]	N14	PC[13]	U1	A[4]
C3	GND	G17	PD[9]	N15	PC[12]	U2	A[6]
C4	GNDUTMI	H1	PB[8]	N16	PC[14]	U3	A[9]
C5	VDDBU	H2	PB[9]	N17	PC[15]	U4	A[13]
C6	WKUP	H3	PB[7]	P1	PB[30]	U5	A[17]
C7	GNDBU	H4	PB[6]	P2	PB[31]	U6	SDWE
C8	TCK	H8	VDDCORE	P3	A[1]	U7	D[3]
C9	TDI	H9	VDDIOP	P4	A[11]	U8	SDCK
C10	PA[31]	H10	PD[4]	P5	A[15]	U9	D[11]
C11	PA[27]	H14	PD[8]	P6	CAS	U10	D[12]
C12	PA[24]	H15	PD[5]	P7	D[1]	U11	D[13]
C13	PA[16]	H16	PD[2]	P8	SDCKE	U12	TSADVREF
C14	PA[11]	H17	PD[3]	P9	D[5]	U13	PA[18]
C15	PD[18]	J1	PB[12]	P10	D[8]	U14	PA[20]
C16	PA[7]	J2	PB[13]	P11	D[15]	U15	PD[6]
C17	PA[6]	J3	PB[11]	P12	PC[0]	U16	PD[7]
D1	PLLRCA	J4	PB[10]	P13	PB[0]	U17	GNDANA
D2	NWR1/NBS1/CFIOR	J8	VDDCORE	P14	PC[8]		
D3	GND	J9	VDDIOP	P15	PC[9]		
D4	GND	J10	PC[29]	P16	PC[10]		

Note: 1. Shaded cells define the pins powered by VDDIOM.

5. Power Considerations

5.1 Power Supplies

The AT91SAM9R64/RL64 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDIOM pins: Power the External Bus Interface; voltage ranges between 1.65V and 1.95V (1.8V nominal) or between 3.0V and 3.6V (3.3V nominal).
- VDDIOP pins: Power the Peripherals I/O lines; voltage ranges from 3.0V and 3.6V, 3.3V nominal.
- VDDBU pin: Powers the Slow Clock oscillator and a part of the System Controller; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDPLLA pin: Powers the PLL cell; voltage ranges from 3.0V and 3.6V, 3.3V nominal.
- VDDPLLB pin: Powers the UTMI PLL (480MHz) and OSC 12M cells; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDUTMII pin: Powers the UTMI+ interface; voltage ranges from 3.0V and 3.6V, 3.3V nominal.
- VDDUTMIC pin: Powers the UTMI+ core; voltage ranges from 1.08V and 1.32V, 1.2V nominal.
- VDDANA pin: Powers the ADC cell; voltage ranges from 3.0V and 3.6V, 3.3V nominal.

The power supplies VDDIOM and VDDIOP are identified in the pinout table and the PIO multiplexing tables. These supplies enable the user to power the device differently for interfacing with memories and for interfacing with peripherals.

Ground pins GND are common to VDDCORE, VDDIOM and VDDIOP pins power supplies.

Separated ground pins are provided for VDDBU, VDDPLLA, VDDPLLB and VDDANA. These ground pins are respectively GNDBU, GNDPLLA, GNDPLLB and GNDANA. A common ground pin is provided for VDDUTMII and VDDUTMIC. This ground pin is GNDUTMI.

Caution: VDDCORE and VDDIO constraints at startup to be checked in the Core Power Supply POR Characteristics in the Electical Characteristics section of the datasheet.

5.1.1 USB Power Supply Considerations

To achieve the best performances on the UDPHS, care must be taken in the power supplies choice and especially on VDDPLLB, VDDUTMIC and VDDUTMII.

The USB High speed requires power supplies with a ripple voltage < 20 mV on VDDPLLB and VDDUTMIC. The VDDUTMII powering the UTMI transceiver must also be filtered.

It is highly recommended to use an LDO linear regulator to generate the 1.2 volts for both VDDPLLB and VDDUTMIC. VDDUTMII can be connected on the 3.3 volts of the system via an LC filter.

The figure below gives an example of VDDPLLB, VDDUTMIC and VDDUTMII.

Figure 5-1. Example of PLL and USB Power Supplies
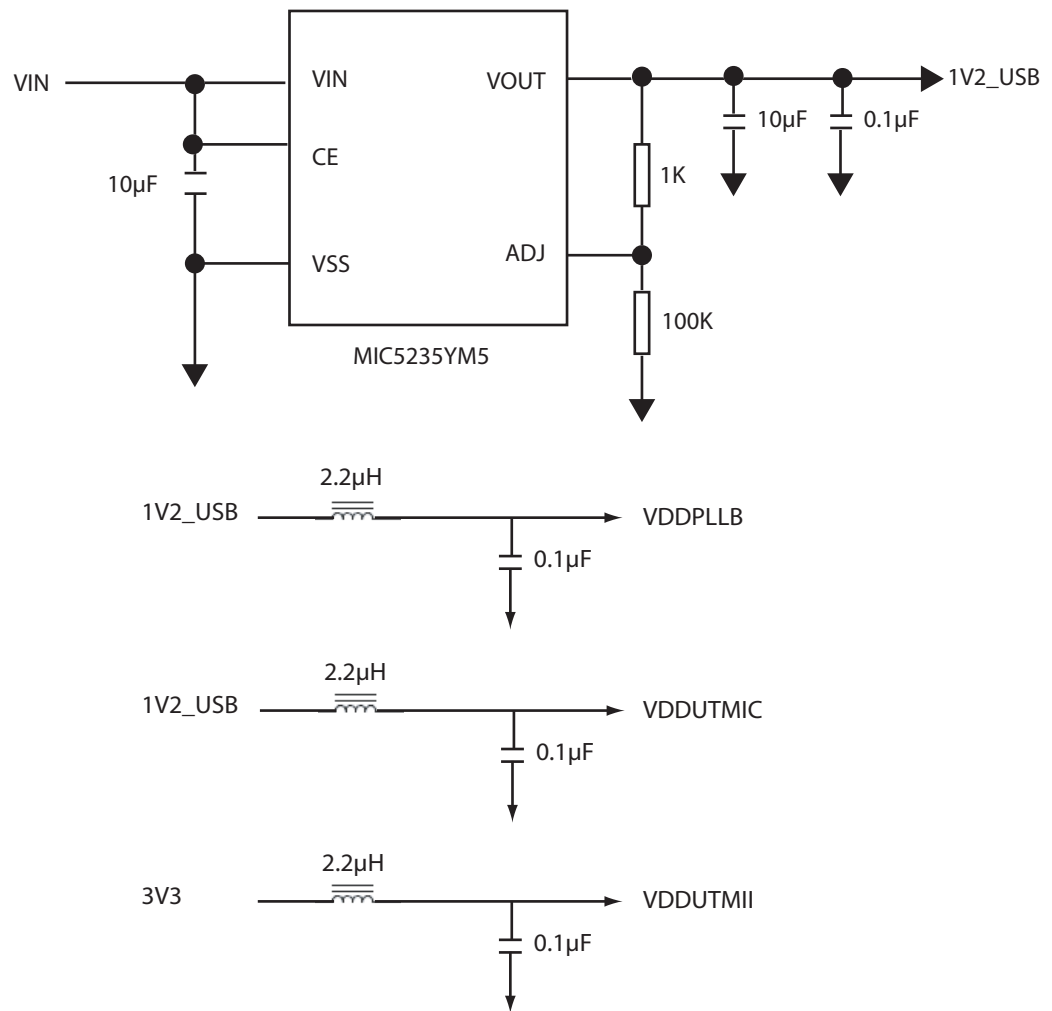
5.2 Programmable I/O Lines Power Supplies

The power supplies pins VDDIOM support two voltage ranges. This allows the device to reach its maximum speed either out of 1.8V or 3.3V external memories.

The maximum speed is MCK on the pin SDCK (SDRAM Clock) loaded with 30pF for power supply at 1.8V and 50 pF for power supply at 3.3V.

The maximum speed on the other signals of the External Bus Interface (control, address and data signals) is 50 MHz.

The voltage ranges are determined by programming registers in the Chip Configuration registers located in the Matrix User Interface.

At reset, the selected voltage defaults to 3.3V nominal and power supply pins can accept either 1.8V or 3.3V. The user must make sure to program the EBI voltage range before getting the device out of its Slow Clock Mode.

The PIO lines are supplied through VDDIOP and the speed of the signal that can be driven on them can reach 50 MHz with 50 pF load.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and have no pull-up resistors.

TDO is an output, driven at up to VDDIOP, and have no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations.

All the JTAG signals are supplied with VDDIOP except JTAGSEL supplied by VDDBU.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 15 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIOP.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pin can be left unconnected.

The NRST and NTRST pins integrates a permanent pull-up resistor of 100 kΩ typical to VDDIOP.

The NRST signal is inserted in the Boundary Scan.

6.4 PIO Controllers

All the I/O lines which are managed by the PIO Controllers integrate a programmable pull-up resistor. Refer to the section "AT91SAM9R64/RL64 Electrical Characteristics" in the product datasheet for more details.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that require to be enabled as Peripheral at reset. This is explicitly indicated in the column "Reset State" of the PIO Controller multiplexing tables.

6.5 Shutdown Logic Pins

The pin WKUP is an input-only. It can accept voltages only between 0V and VDDBU.

7. Processor and Architecture

7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets

- ARM High-performance 32-bit Instruction Set
- Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 4-Kbyte Data Cache, 4-Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

7.2 Matrix Masters

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	DMA Controller
Master 1	USB Device High Speed DMA
Master 2	LCD Controller DMA

Table 7-1. List of Bus Matrix Masters

Master 3	Peripheral DMA Controller
Master 4	ARM926™ Instruction
Master 5	ARM926 Data

7.3 Matrix Slaves

The Bus Matrix of the AT91SAM9R64/RL64 product manages 6 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal ROM
Slave 1	Internal SRAM
Slave 2	LCD Controller User Interface
Slave 3	UDP High Speed RAM
Slave 4	External Bus Interface (EBI)
Slave 5	Peripheral Bridge

7.4 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB Device High speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as "-" in the following table.

Table 7-3. AT91SAM9R64/RL64 Master to Slave Access

Masters		0	1	2	3	4	5
Slaves		DMA Controller	USB HS Device DMA	LCD Controller DMA	Peripheral DMA	ARM926 Instruction	ARM926 Data
0	Internal ROM	X	X		X	X	X
1	Internal SRAM	X	X	X	X	X	X
2	LCD Controller User Interface	-	-	-	-	X	X
3	UDP High Speed RAM	-	-	-	-	X	X
4	External Bus Interface	X	X	X	X	X	X
5	Peripheral Bridge	X	X	X	-	-	-

7.5 Peripheral DMA Controller (PDC)

- Acting as one AHB Bus Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer support, prevents strong real-time constraints on buffer management.

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

a.   TWI0 Transmit Channel

b.   DBGU Transmit Channel

c.   USART3 Transmit Channel

d.   USART2 Transmit Channel

e.   USART1 Transmit Channel

f.   USART0 Transmit Channel

g.   AC97 Transmit Channel

h.   SPI Transmit Channel

i.   SSC1 Transmit Channel

j.   SSC0 Transmit Channel

k.   TWI0 Receive Channel

l.   DBGU Receive Channel

m.   ADC Receive Channel

n.   USART3 Receive Channel

o.   USART2 Receive Channel

p.   USART1 Receive Channel

q.   USART0 Receive Channel

r.   AC97 Receive Channel

s.   SPI Receive Channel

t.   SSC1 Receive Channel

u.   SSC0 Transmit Channel

v.   MCI Receive/Transmit Channel

7.6   DMA Controller

- Acting as one Matrix Master
- Embeds 2 channels
- 16 bytes/FIFO for Channel Buffering
- Linked List support with Status Write Back operation at End of Transfer
- Word, Half-word, Byte transfer support

7.7   Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

8. Memories

Figure 8-1. AT91SAM9R64/RL64 Memory Mapping

6289CS–ATARM–28-May-09
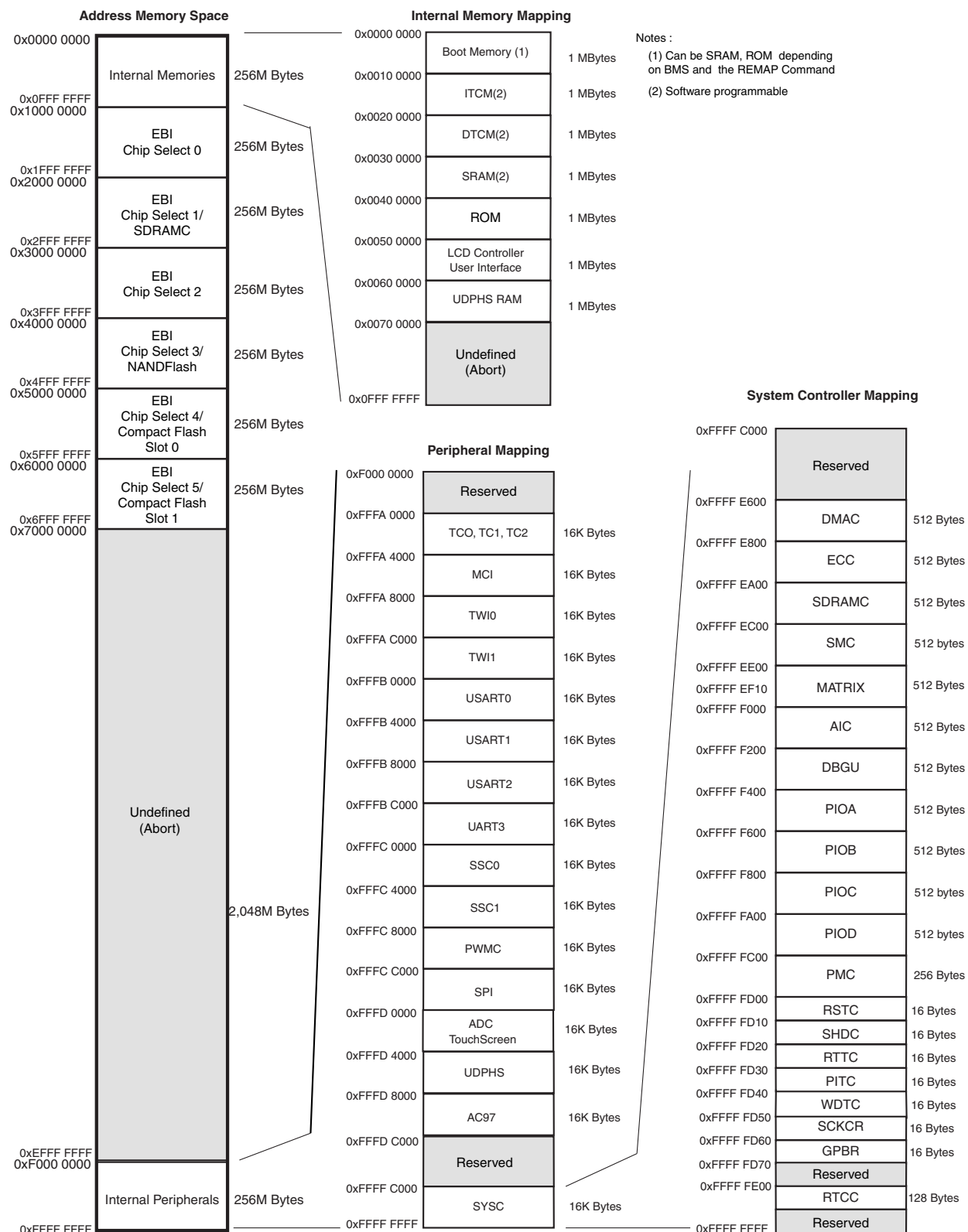
A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 8 are directed to the EBI that associates these banks to the external chip selects EBI_NCS0 to EBI_NCS5. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

8.1 Embedded Memories

- 32 KB ROM
  - Single Cycle Access at full bus speed
- 64 KB Fast SRAM
  - Single Cycle Access at full bus speed
  - Supports ARM926EJ-S TCM interface at full processor speed

8.1.1 Internal Memory Mapping

Table 8-1 summarizes the Internal Memory Mapping for each Master, depending on the Remap status (RCBx bit) and the BMS state at reset.

Table 8-1. Internal Memory Mapping

Address	RCBx[1] = 0		RCBx[1] = 1
	BMS = 1	BMS =0	
0x0000 0000	ROM	EBI_NCS0[2]	SRAM

Notes: 1. x = 0 to maximum Master number.
2. EBI NCS0 is to be connected to a 16-bit non-volatile memory. The access configuration is defined by the reset state of SMC Setup, SMC Pulse, SMC Cycle and SMC Mode CS0 registers.

8.1.1.1 Internal SRAM

The AT91SAM9R64/RL64 product embeds a total of 64Kbyte high-speed SRAM split in 4 blocks of 16KBytes.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0030 0000.

After Remap, the SRAM also becomes available at address 0x0.

This Internal SRAM can be allocated to threes areas. Its Memory Mapping is detailed in Table 8-2.

- Internal SRAM A is the ARM926EJ-S Instruction TCM. The user can map this SRAM block anywhere in the ARM926 instruction memory space using CP15 instructions and the TCR configuration register located in the Chip Configuration User Interface. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0010 0000.

• Internal SRAM B is the ARM926EJ-S Data TCM. The user can map this SRAM block anywhere in the ARM926 data memory space using CP15 instructions. This SRAM block is also accessible by the ARM926 Data Master and by the AHB Masters through the AHB bus at address 0x0020 0000.

• Internal SRAM C is only accessible by all the AHB Masters. After reset and until the Remap Command is performed, this SRAM block is accessible through the AHB bus at address 0x0030 0000 by all the AHB Masters. After Remap, this SRAM block also becomes accessible through the AHB bus at address 0x0 by the ARM926 Instruction and the ARM926 Data Masters.

Within the 64Kbyte SRAM size available, the amount of memory assigned to each block is software programmable as a multiple of 16K Bytes according to Table 8-2. This Table provides the size of the Internal SRAM C according to the size of the Internal SRAM A and the Internal SRAM B.

Table 8-2. Internal SRAM Block Size

Remaining Internal SRAM C		Internal SRAM A (ITCM) Size		
		0	16K Bytes	32K Bytes
Internal SRAM B (DTCM) size	0	64K Bytes	48K Bytes	32K Bytes
	16K Bytes	48K Bytes	32K Bytes	16K Bytes
	32K Bytes	32K Bytes	16K Bytes	0K Bytes

At reset, the whole memory is assigned to Internal SRAM C.

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16-Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-3 illustrates different configurations and the related 16-Kbyte blocks (RB0 to RB3) assignments.

Table 8-3. 16-Kbyte Block Allocation example

Decoded Area	Address	Configuration examples and related 16-Kbyte block assignments								
		I = 0K D = 0K A = 64K[1]	I = 16K D = 0K A = 48K	I =32K D = 0K A = 32K	I = 0K D = 16K A = 48K	I = 16K D = 16K A = 32K	I = 32K D = 16K A = 16K	I = 0K D = 32K A = 32K	I = 16K D = 32K A = 16K	I = 32K D = 32K A = 0K
Internal SRAM A (ITCM)	0x0010 0000		RB1	RB1		RB1	RB1		RB1	RB1
	0x0010 4000			RB0			RB0			RB0
Internal SRAM B (DTCM)	0x0020 0000				RB3	RB3	RB3	RB3	RB3	RB3
	0x0020 4000							RB2	RB2	RB2
Internal SRAM C (AHB)	0x0030 0000	RB3	RB3	RB3	RB2	RB2	RB2	RB1	RB0	
	0x0030 4000	RB2	RB2	RB2	RB1	RB0		RB0		
	0x0030 8000	RB1	RB0		RB0					
	0x0030 C000	RB0								

Note: 1.   Configuration after reset.

When accessed from the AHB, the internal Fast SRAM is single cycle accessible at full matrix speed (MCK). When accessed from the processor's TCM Interface, they are also single cycle accessible at full processor speed.

The AT91SAM9R64/RL64 embeds an Internal ROM, which contains the SAM-BA program.

At any time, the ROM is mapped at address 0x0040 0000. It is also accessible at address 0x0 (BMS =1) after the reset and before the Remap Command.

8.1.2   Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed with two parameters.

REMAP allows the user to layout the internal SRAM bank to 0x0 to ease the development. This is done by software once the system has boot. Refer to the Bus Matrix Section for more details.

When REMAP = 0 BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done by a hardware way at reset.

Note: All the memory blocks can always be seen at their specified base addresses that are not concerned by these parameters.

The AT91SAM9R64/RL64 Bus Matrix manages a boot memory that depends on the level on the pin BMS at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved to this effect.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

8.1.2.1   BMS = 1, boot on embedded ROM

The system boots on Boot Program.

- Boot on on-chip RC
- Enable the 32768 Hz oscillator
- Auto baudrate detection
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SDCard (boot ROM does not support high-capacity SDCards)
  - NAND Flash
  - SPI DataFlash® connected on NPCS0 of the SPI0
- SAM-BA Boot in case no valid program is detected in external NVM, supporting
  - Serial communication on a DBGU
  - USB Device HS Port

8.1.2.2   BMS = 0, boot on external memory

- Boot on on-chip RC