XRT7295AE

E3 (34.368Mbps)
Integrated line Receiver

March 2003

FEATURES

- Fully Integrated Receive Interface for E3 Signals
- Integrated Equalization (Optional) and Timing Recovery
- Loss-of-Signal and Loss-of-Lock Alarms
- Variable Input Sensitivity Control
- 5V Power Supply
- Compliant with G703, G.775 and G.824 Specifications

APPLICATIONS

- Interface to E3 Networks
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

GENERAL DESCRIPTION

The XRT7295AE E3 Integrated Line Receiver is a fully integrates receive interface that terminates a bipolar E3 (34.3684 Mbps) signal transmitted over coaxial Cable. This device can be used with the XRT7296 Integrated Line Transmitter (see Figure 10),

The device provides the functions of receive equalization (optional) automatic gain control (AGC), clock recovery and data re-timing, loss of signal and loss-of frequency lock detection. The digital system interface is a dual-rail with received positive and negative 1s appearing as unipolar digital signals on separate output leads. The on-chip equalizer is designed for cable losses of 0 to 15dB. The receive input has a variable input sensitivity control, providing three different sensitivity settings. High input sensitivity allows for significant amounts of flat loss or for use with input signals at the monitor level. Figure 1 shows the block diagram of the device.

The XRT7295AE is manufactured by using linear CMOS technology. The XRT7295AE is available in a 20-pin plastic SOJ package for surface mounting. A pin compatible version is available for DS3 or STS-1 applications. Please refer to the XRT7295AT data sheet

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRT7295AEIW	20 J-lead 300 MIL JEDEC SOJ	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017

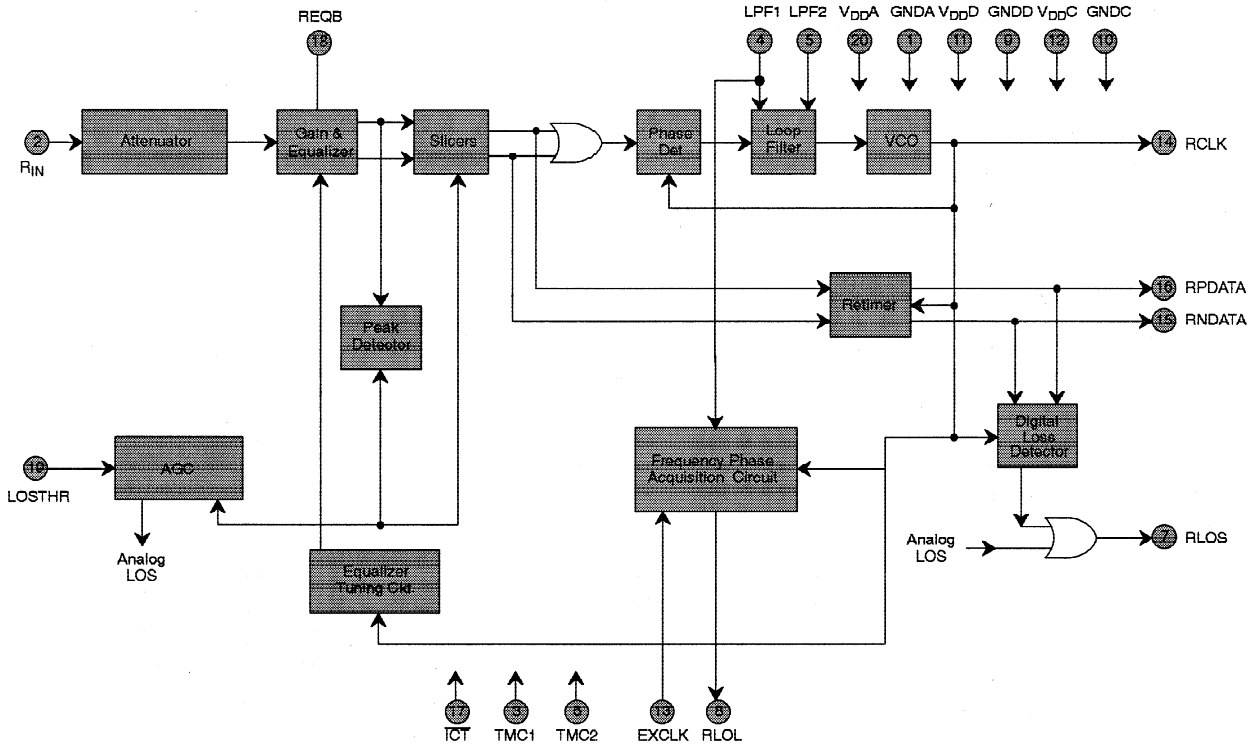
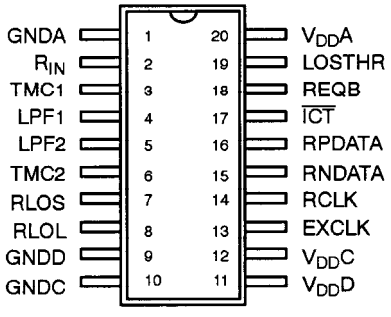


Figure 1. Block Diagram

PIN CONFIGURATION



20 Lead SOJ (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	GNDA		**Analog Ground.**
2	R_{IN}	I	**Receive Input.** Unbalanced analog receive input
3,6	TMC1-TMC2	I	**Test Mode Control 1 and 2.** Internal test modes are enabled within the device by using TMC1 and TMC2. Users must tie these pins to the ground plane.
4,5	LPF-1-LPF-2	I	**PLL Filter 1 and 2.** An external capacitor (0.1µF +/-20%) is connected between these pins (See Figure 3).
7	RLOS	O	**Receive Loss-of-Signal.** This pin is set high on loss of signal at the receive input.
8	RLOL	O	**Receive PLL Loss-of-Lock.** This pin is set high on loss of PLL frequency lock.
9	GNDD		**Digital Ground for PLL Lock.** Ground lead for all circuitry running synchronously with PLL clock.
10	GNDC		**Digital Ground for EXCLK.** Ground lead for all circuitry running synchronously with EXCLK.
11	$V_{DD}D$		**5V Digital Supply (+/-10%) for PLL Clock.** Power for all circuitry running synchronously with PLL clock.
12	$V_{DD}C$		**5V Digital Supply (+/-10%) for EXCLK.** Power for all circuitry running synchronously with EXCLK.
13	EXCLK	I	**External Reference Clock.** A valid E3 (34.368MHz +/-100ppm) clock must be provided at this input. The duty cycle of EXCLK, referenced to $V_{DD}/2$ levels, must be 40%-60%.
14	RCLK	O	**Receive Clock.** Recovered clock signal to the terminal equipment.
15	RNDATA	O	**Receive Negative Data.** Negative pulse data output to the terminal equipment.
16	RPDATA	O	**Receive Positive Data.** Positive pulse data output to the terminal equipment.
17	$\overline{ICT}$	I	**Output In-Circuit Test Control (Active-Low).** If $\overline{ICT}$ is forced low, all digital output pins (RCLK, RPDATA, RNDATA, RLOS, RLOL) are placed in a high-impedance state to allow for in-circuit testing.
18	REQB	I	**Receive Equalization Bypass.** A high on this pin bypasses the internal equalizer. A low places the equalizer in the data path.
19	LOSTHR	I	**Loss-of-Signal Threshold Control.** The voltage forced on this pin controls the input loss-of-signal threshold. Three settings are provided by forcing the GND, $V_{DD}/2$, or V_{DD} at LOSTHR.
20	$V_{DD}A$		**5V Analog Supply (+/-10%).**

DC ELECTRICAL CHARACTERISTICS

Test Conditions: -40°C < TA < +85°C, VDD = 5V +/-10%

Typical values are for V_{DD} =5.0V, 25°C, and random data. Maximum values for V_{DD} = 5.5V at 85°C all 1s data.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Electrical Characteristics						
I_{DD}	Power Supply Current					
	REQB=0		82	106	mA	
	REQB=1		79	103	mA	
Logical Interface Characteristics						
	Input Voltage					
V_{IL}	Low	GNDD		0.5	V	
V_{IH}	High	V_{DD}D -0.5		V_{DD}D	V	
	Output Voltage					
V_{OL}	Low	GNDD		0.4	V	-5.0mA
V_{OH}	High	V_{DD}D -0.5		V_{DD}D	V	5.0mA
C_I	Input Capacitance			10	pF	
C_L	Load Capacitance			10	pF	
I_L	Input Leakage	-10		10	µA	-0.5 to V_{DD} +0.5V (all input pins except 2 and 17)
		0.02		0.5	mA	0V (pin 17)
		10		100	µA	V_{DD} (pin 2)
		-50		-5	µA	GND (pin 2)

Note: Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... -0.5V to +6.5V

Storage Temperature ..... -40°C to +125°C

Voltage at any Pin ..... -0.5V to V_{DD} +0.5V

Power Dissipation 700mW

Maximum Allowable Voltages (R_{IN})
with Respect to GND ..... -0.5 to +5V

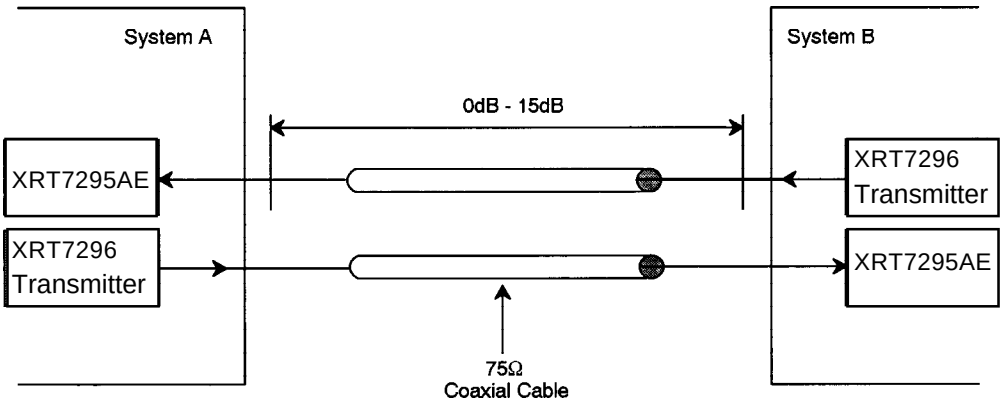


Figure 2. Application Diagram

SYSTEM DESCRIPTION

Receive Path Configurations

The diagram in Figure 2 shows a typical system application for the XRT7295AE. In the receive signal path (see Figure 1), the internal equalizer can be included by setting REQB=0 or bypass by setting REQB=1. The equalizer bypass option allows easy interfacing of the XRT7295AE into systems already containing the external equalizers. Figure 3 illustrates the receive path option for two separate cases.

In case 1, the signal from the coaxial cable feeds directly into the R_{IN} input. In this mode, the user should set REQB=0, engaging the equalizer in the data path if the cable loss is greater than 6dB. If the cable loss is less than 6dB, the equalizer is bypassed by setting the REQB=1.

In case 2, an external line and equalizer network precedes the XRT7295AE. In this mode, the signal at R_{IN} is already equalized, and the on-chip equalizer should be bypassed by setting REQB1=1. In both cases, the signal at R_{IN} must meet the amplitude limits described in Table 1.

The recommended receive termination is also shown in Figure 3. The 75Ω resistor terminates the coaxial cable with its characteristic impedance. In Figure 3 case 2, if the fixed equalizer includes the line termination, the 75Ω resistor is not required. The signal is AC coupled through the 0.01µF capacitor to R_{IN}. The DC bias at R_{IN} is generated internally. The input capacitance at the R_{IN} pin is typically 2.8pF (SOJ package).

Pulse Mask at the 34.368 Mbps Interface

Table 2 shows the pulse specifications at the transmitter output post and Figure 4 shows the pulse mask requirement for E3 as recommended in G.703.

REQB	LOSTHR	Minimum Signal		Unit3
		SOJ2	DIP	
0	0	80	115	mV pk
	$V_{DD}/2$	60	85	mV pk
	V_{DD}	40	60	mV pk
1	0	80	115	mV pk
	$V_{DD}/2$	80	115	mV pk
	V_{DD}	80	115	mV pk

NOTES:

1 *Maximum input amplitude under all conditions is 1.1 Vpk.*

2 *The SOJ package performance is enhanced by decreased package parasitics.*

3 *Although system designers typically use power in dBm to describe input levels, the XRT7295AE responds to peak input signal amplitude. Therefore, the XRT7295AE input signal limits are given in mV pk.*

Table 1. Receive Input Signal Amplitude Requirements

Line Termination and Input Capacitance

The recommended receive termination is shown in Figure 3. The 75Ω resistor terminates the coaxial cable with its characteristic impedance. The 0.01µF capacitor to R_{IN} couples the signal into the receive input without disturbing the internally generated DC bias level present on R_{IN}. The input capacitance at the R_{IN} pin is 2.8pF.

External Loop Filter Capacitor

Figure 3 shows the connection to an external 0.1µF capacitor at the LPF1/LPF2 pins. This capacitor is part of the PLL filter. A non-polarized, low-leakage capacitor should be used. A ceramic capacitor with the value 0.1µF +/-20% is acceptable.

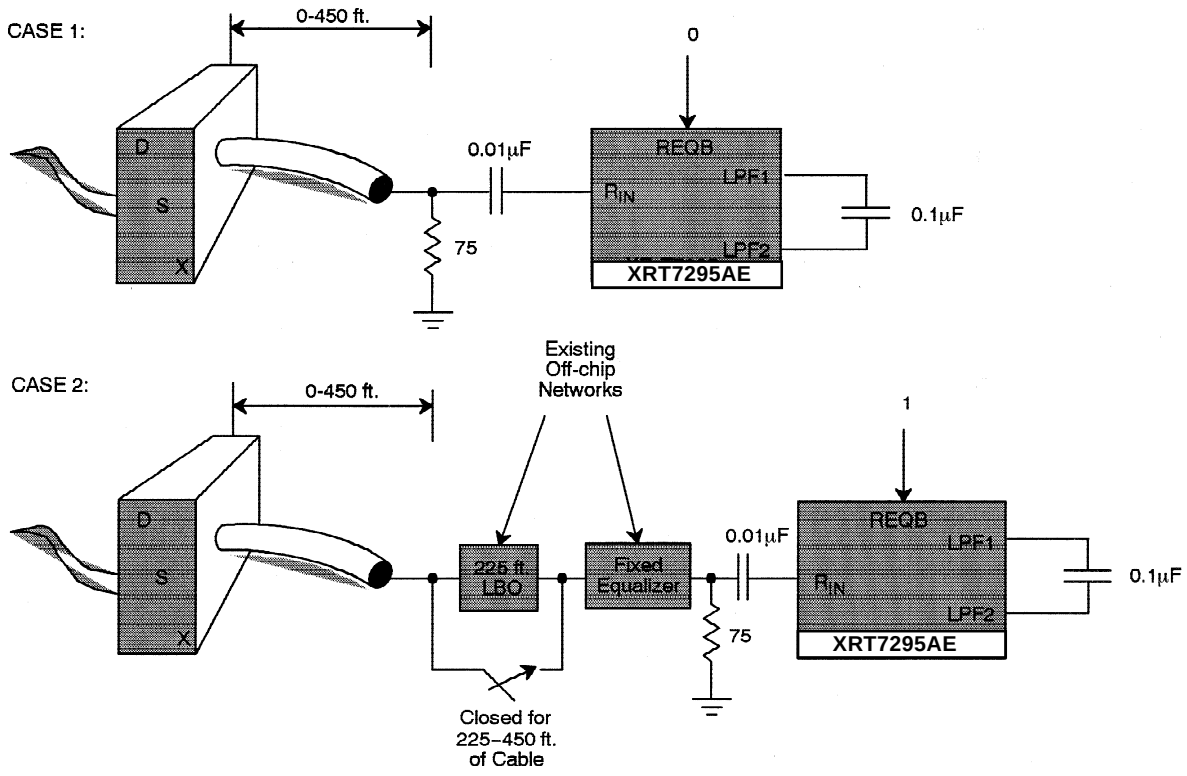


Figure 3. Receiver Configuration

TIMING RECOVERY

Output Jitter

The total jitter appearing on the RCLK output during normal operation consists of two components. First, some jitter appears on RCLK because of jitter on the incoming signal. (The following section discussed the jitter transfer characteristic, which describes the relationship between input and output jitter.) Second, noise sources within the XRT7295AE or noise sources that are coupled into the device through the power supplies create jitter on RCLK. The magnitude of this

internally generated jitter is a function of the PLL bandwidth, which in turn is a function of the input 1s density. For higher 1s densities, the amount of generated jitter decreases. Generated jitter also depends on the quality of the power supply bypassing networks used. Figure 8 shows the suggested bypassing network, and Table 3 lists the typical generated jitter performance achievable with this network.

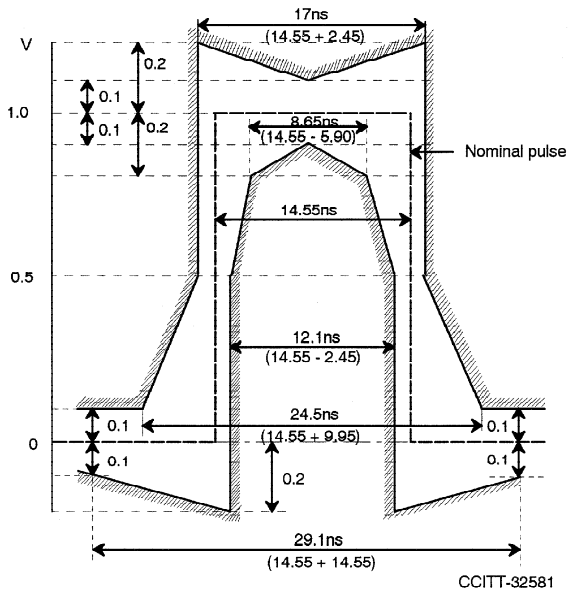


Figure 4. Pulse Mask at the 34.368 Mbit/s Interface

Parameter	Value
Pulse Shape (Nominally Rectangular)	All marks of a valid signal must conform with the mask (see Figure 4), irrespective of the sign
Pair(s) in Each Direction	One coaxial pair
Test Load Impedance	75Ω Resistive
Nominal Peak Voltage of a Mark (Pulse)	1.0V
Peak Voltage of a Space (No Pulse)	0V +/-0.1V
Nominal Pulse Width	14.55ns
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of a Pulse Interval	0.95 to 1.05
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05

Table 2. E3 Pulse Specification at the Transmitter Output Port

Jitter Transfer Characteristic

The jitter transfer characteristic indicates the fraction of input jitter that reaches the RCLK output as a function of input jitter frequency. Table 3 shows important jitter transfer characteristic parameters. Figure 6 also shows a typical characteristic , with the operating conditions as described in Table 3.

Parameter	Typ.	Max.	Unit
Generated Jitter[1]			
All-1s patter	1.0		ns peak-to-peak
Repetitive 1000 pattern	1.5		ns peak-to-peak
Jitter Transfer Characteristic[2]			
Peaking	0.05	0.1	dB
f3dB	205		kHz

Notes:

1 Repetitive input data pattern at nominal E3 level with V_{DD}=5V TA=25°C.

2 Repetitive 1000 input at nominal E3 level with V_{DD}=5V, TA=25°C.

Table 3. Generated Jitter and Jitter Transfer Characteristics

Jitter Accommodation

Under all allowable operating conditions, the jitter accommodation of XRT7295AE exceeds limits for error-free operation (BER < $1E^{-9}$). The typical (V_{DD} = 5V, T = 25°C, E3 nominal signal level) jitter accommodation of the device is shown in Figure 6.

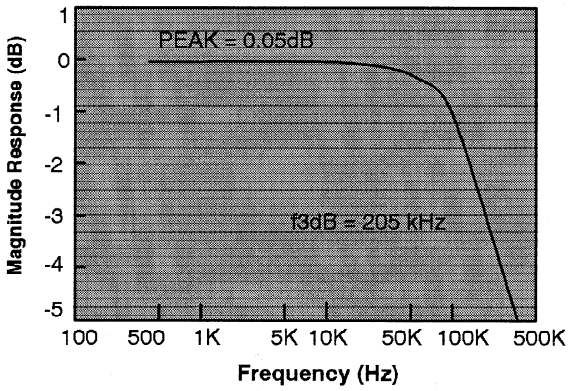


Figure 5. Typical PLL Jitter Transfer Characteristics

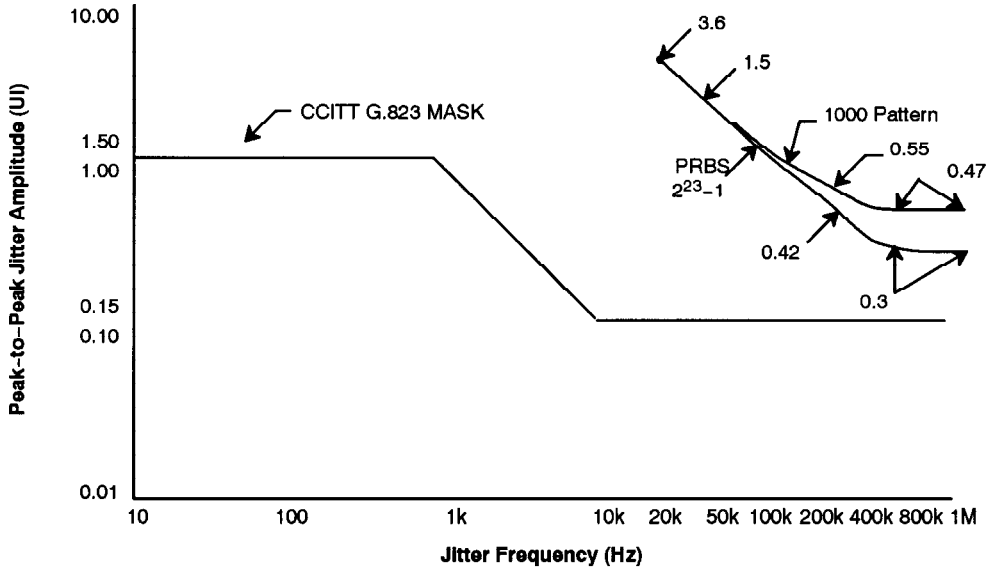


Figure 6. Lower Limit of Maximum Tolerable Input Jitter at 34.368Mbps

False-Lock Immunity

False-lock is defined as the condition where a PLL recovered clock obtains stable phase-lock at a frequency not equal to the incoming data rate. The XRT7295AE uses a combination frequency/phase-lock architecture to prevent false-lock. An on-chip frequency comparator continuously compares the EXCLK reference to the PLL clock. If the frequency difference between the EXCLK and PLL clock exceeds approximately +/-0.5% of EXCLK, correction circuitry acts to force the reacquisition of the proper frequency and phase.

Acquisition Time

If a valid input signal is assumed to be already present at RIN, the maximum time between the application of device power and error-free operation is 20ms. If power has already been applied, the interval between the application of valid data and error-free operation is 4ns.

Loss-of-Lock Indication

As previously stated, the PLL acquisition aid circuitry monitors the PLL clock frequency relative to the EXCLK frequency.

The acquisition circuit also monitors the resumed data to detect possible phase-lock which is 180° out of a normal phase alignment. The RLOL alarm is activated if either or both of the following conditions exist:

- The difference between the PLL clock and the EXCLK frequency exceeds approximately +/-0.5%.
- The retimed data is 180° out of a normal phase alignment.

A high RLOL output indicates that the acquisition circuit is working to bring the PLL into proper frequency lock. RLOL remains high until frequency lock has occurred; however, the minimum RLOL pulse width is 32 clock cycles.

Loss-of-Signal Detection

Figure 1 shows that analog and digital methods of loss-of-signal (LOS) detection are combined to create the RLOS alarm output. RLOS is set if either the analog or digital detection circuitry indicates LOS has occurred.

Data Rate	REQB	LOSTHR	Threshold MIN	Threshold Max	Unit
	0	0	60	220	mV pk
E3		V_{DD}/2	40	145	mV pk
34.368		V_{DD}	25	90	mV pk
Mbps	1	0	45	175	mV pk
		V_{DD}/2	30	115	mV pk
		V_{DD}	20	70	mV pk

Notes:

1 *The RLOS alarm is an indication of the presence of an input signal, not a bit error rate indication. Table 1 gives the minimum input amplitude needed for error-free operation (BER<1E^{-9}). Independent of the RLOS state, the device will attempt to recover correct timing and data.*

2 *The RLOS low-to-high transition typically occurs 1dB below the high-to-low transition.*

Analog Detection

The analog LOS detector monitors the peak input signal amplitude. RLOS makes a high-to-low transition (input signal regained) when the input signal amplitude exceeds the loss-of-signal threshold defined in Table 4. The RLOS low-to-high transition (input signal loss) occurs at a level typically 1.0dB below the high-to-low transition level. The hysteresis prevents RLOS chattering. Once set, the RLOS alarm remains high for at least 32 clock cycles, allowing for system detection of a LOS condition without the use of an external alarm latch.

To allow for varying levels of noise and crosstalk in different applications, three loss-of-signal threshold settings are available using the LOSTHR pin. Setting LOSTHR = V_{DD} provides the lowest loss-of-signal threshold; LOSTHR = V_{DD}/2 (can be produced using two 50kΩ +/-10% resistor as a voltage divider between V_{DD}D and GNDD) provides an intermediate threshold. LOSTHR = GND provides the highest threshold. The LOSTHR pin must be set to its desired value at power up and must not be changed during operation.

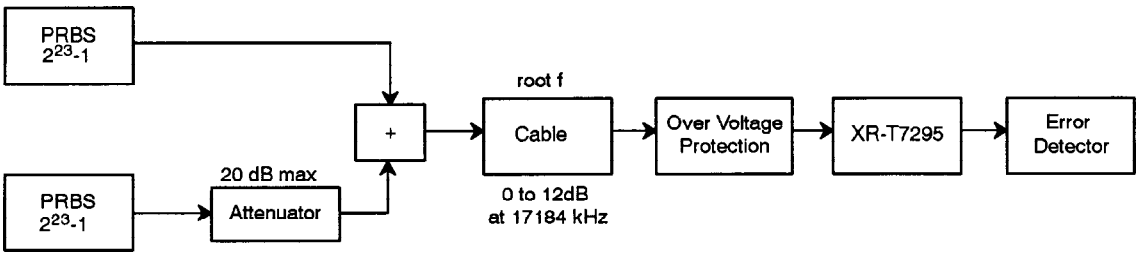


Figure 7. Test Set-up for Interference Immunity Requirements

Digital Detection

In addition to the signal amplitude monitoring of the analog LOS detector, the digital LOS detector monitors the recovered data 1s density. The RLOS alarm goes high if 160 +/-32 or more consecutive bits. The alarm goes low when at least eight 1s occur in a a string of 32 consecutive bits. This hysteresis minimizes RLOS chattering and guarantees a minimum RLOS pulse width of 32 clock cycles.

NOTE:

RLOS chatter can still occur. When REQB=1, input signal levels above the analog LOS threshold can still be low enough to result in a high but error rate. The resultant data stream (containing errors) can temporarily activate the digital LOS detector, ad RLOS chatter can occur. Therefore, RLOS should not be used as a bit error rate monitor. RLOS chatter can also occur when RLOL is activated (high).

Phase Hits

In response to a 180° phase hit in the input data, the XRT7295AE returns to error-free operation in less than 2ms. During the reacquisition time, RLOS may be temporarily indicated.

Recovered Clock and Data Timing

Table 6 and Figure 9 summarize the timing relationships between the high-speed logic signals RCLK, RPDATA, and RNDATA. All duty cycle and timing relationships are referenced to $V_{DD}/2$ threshold level. RPDATA and RNDATA change on the rising edge of RCLK and are valid during the falling edge of RCLK. A positive pulse at RIN creates a high level on RPDATA and a low level on RNDATA. A negative pulse creates a high level on RNDATA and a low level on RPDATA, and a received zero produces low levels on both RPDATA and RNDATA.

Parameter	Min.	Typ.	Max.	Unit
Attenuator	-20	-16		dB

Table 5. Interference Requirement

Interference Immunity

The XRT7295AE complies with the interference test detailed in Figure 7 and Table 5. The two data generators are non-synchronous.

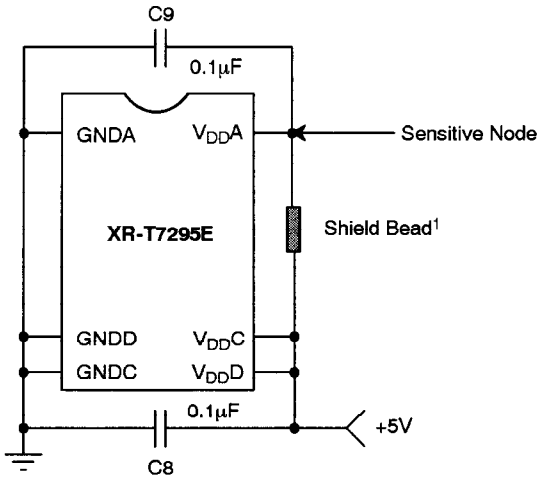
In-Circuit Test Capability

When pulled low, the $\overline{ICT}$ pin forces all digital output buffers (RCLK, RPDATA, RNDATA, RLOS, RLOL pins) to be placed in a high output impedance state, This feature allows in-circuit testing to be done on neighboring devices without concern for XRT7295AE buffer damage. When forced high, the $\overline{ICT}$ pin does not affect device operation. An internal pull-up device (nominally 50 kΩ) is provided on this pin; therefore, users can leave this pin open for normal operation. This is the only pin for which the internal pull-up/pull-down is provided.

BOARD LAYOUT CONSIDERATIONS

Power Supply Bypassing

Figure 8 illustrates the recommended power supply bypassing network. A 0.1µF capacitor bypasses the digital supplies. The analog supply $V_{DD}A$ is bypassed by using a 0.1µF capacitor and a shield bead that removes significant amounts of high-frequency noise generated by the system and by the device logic. Good quality, high-frequency (low lead inductance) capacitors should be used. Finally, it is most important that all ground connections be made to a low-impedance ground plane.



Note:

1 Recommended shield beads are the Fair-Rite 2643000101 or the Fair-Rite 2743019446 (surface mount).

Figure 8. Recommended Power Supply Bypassing Network

Receive Input

The connections to the receive input pin, RIN, must be carefully considered. Noise-coupling must be minimized along the path from the signal entering the board to the input pin. Any noise coupled into the XRT7295AE input directly degrades the signal-to-noise ratio of the input signal.

PLL Filter Capacitor

The PLL filter capacitor between pins LPF1 and LPF2 must be placed as close to the chip as possible. The LPF1 and LPF 2 pins are adjacent, allowing for short lead lengths with no crossovers to the external capacitor. Noise-coupling into the LPF1 and LPF2 pins may degrade PLL performance.

Handling Precautions

Although protection circuitry has been design into this device, proper precautions should be taken to avoid exposure to Electrostatic Discharge (ESD) during handling and mounting.

COMPLIANCE SPECIFICATIONS

Compliance with *CCITT Recommendations* G.703, G.775, and G.824, 1988.

TIMING CHARACTERISTICS

Test Conditions: All timing characteristics are measured with 10pF loading, -40°C < TA < 85°C, V_{DD} = 5V +/-10%

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRCH1RCH2	Clock Rise Time (10%-90%)			3.5	ns
tRCL1RCL1	Clock Fall Time (10% to 90%			2.5	ns
TRCGRD	Receive Propagation Delay[1]	0.6		3.7	ns
	Clock Duty Cycle	45	50	55	%

Note:

1 The total delay from RIN to the digital outputs RPDATA and RNDATA is three RCLK clocks.

Table 6. System Interface Timing Characteristics (See Figure 9)

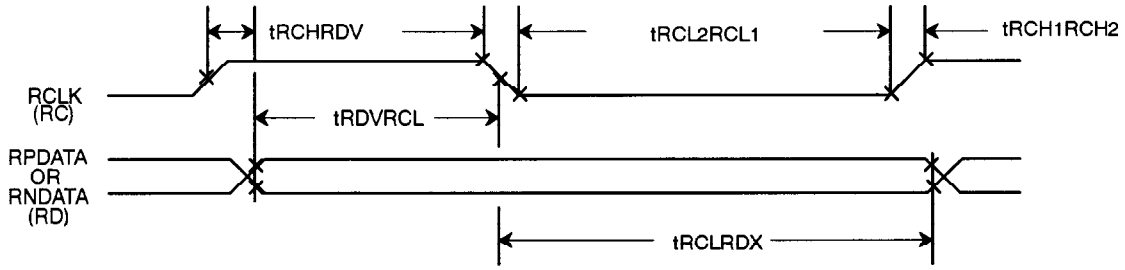


Figure 9. Timing Diagram for System Interface

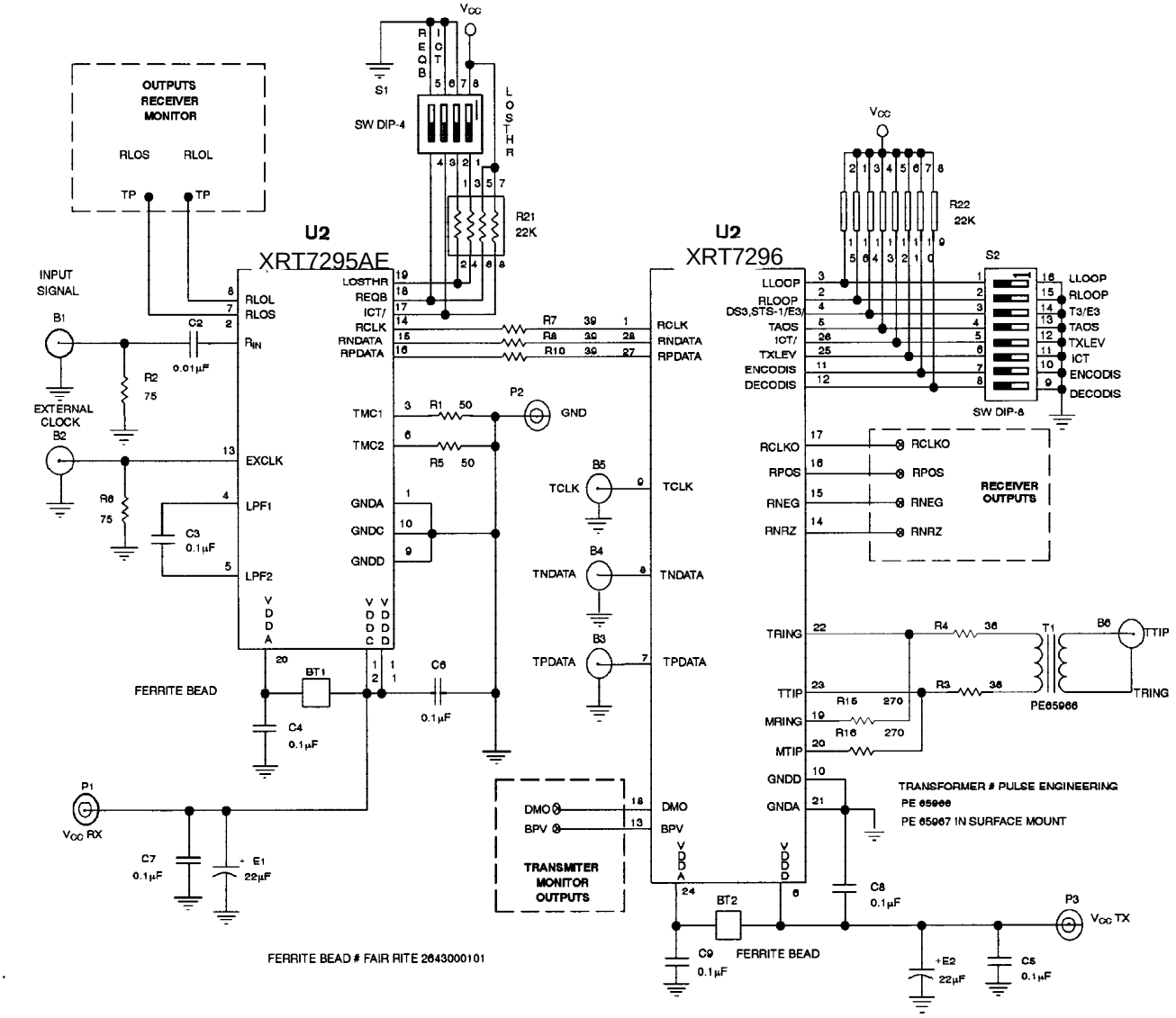
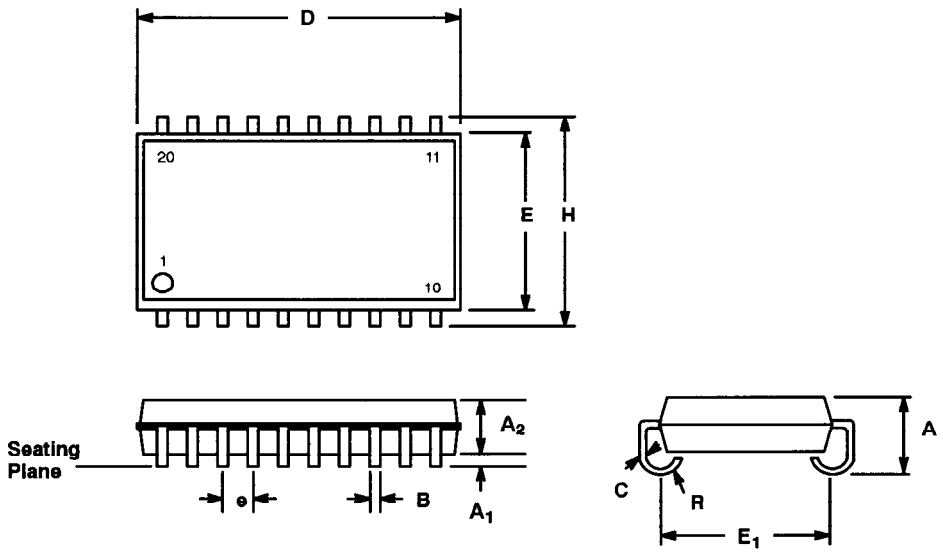


Figure 10. Evaluation System Schematic

20 LEAD SMALL OUTLINE J LEAD (300 MIL JEDEC SOJ)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.200	3.60	5.08
A_1	0.025	---	0.64	---
A_2	0.120	0.140	3.05	3.56
B	0.014	0.020	0.36	0.51
C	0.008	0.013	0.20	0.30
D	0.496	0.512	12.60	13.00
E	0.292	0.300	7.42	7.62
E_1	0.262	0.272	6.65	6.91
e	0.050 BSC		1.27 BSC	
H	0.335	0.347	8.51	8.81
R	0.030	0.040	0.76	1.02

Note: The control dimension is the inch column

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