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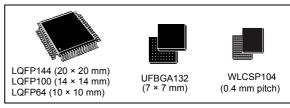
STM32L151xE STM32L152xE

Ultra-low-power 32-bit MCU ARM®-based Cortex®-M3 with 512KB Flash, 80KB SRAM, 16KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
 - 1.65 V to 3.6 V power supply
 - -40 °C to 105 °C temperature range
 - 290 nA Standby mode (3 wakeup pins)
 - 1.11 μA Standby mode + RTC
 - 560 nA Stop mode (16 wakeup lines)
 - 1.4 μA Stop mode + RTC
 - 11 μA Low-power run mode down to 4.6 μA in Low-power sleep mode
 - 195 µA/MHz Run mode
 - 10 nA ultra-low I/O leakage
 - 8 µs wakeup time
- Core: ARM[®] Cortex[®]-M3 32-bit CPU
 - From 32 kHz up to 32 MHz max
 - 1.25 DMIPS/MHz (Dhrystone 2.1)
 - Memory protection unit
- · Up to 34 capacitive sensing channels
- CRC calculation unit, 96-bit unique ID
- · Reset and supply management
 - Low-power, ultrasafe BOR (brownout reset) with 5 selectable thresholds
 - Ultra-low-power POR/PDR
 - Programmable voltage detector (PVD)
- · Clock sources
 - 1 to 24 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - Internal 16 MHz oscillator factory trimmed RC(+/-1%) with PLL option
 - Internal low-power 37 kHz oscillator
 - Internal multispeed low-power 65 kHz to 4.2 MHz oscillator
 - PLL for CPU clock and USB (48 MHz)
- Pre-programmed bootloader
 - USB and USART supported



- Up to 116 fast I/Os (102 I/Os 5V tolerant), all mappable on 16 external interrupt vectors
- Memories
 - 512 KB Flash memory with ECC (with 2 banks of 256 KB enabling RWW capability)
 - 80 KB RAM
 - 16 KB of true EEPROM with ECC
 - 128 Byte backup register
- LCD driver (except STM32L151xE devices) up to 8x40 segments, contrast adjustment, blinking mode, step-up converter
- Rich analog peripherals (down to 1.8 V)
 - 2x operational amplifiers
 - 12-bit ADC 1 Msps up to 40 channels
 - 12-bit DAC 2 ch with output buffers
 - 2x ultra-low-power comparators (window mode and wake up capability)
- DMA controller 12x channels
- 11x peripheral communication interfaces
 - 1x USB 2.0 (internal 48 MHz PLL)
 - 5x USARTs
 - Up to 8x SPIs (2x I2S, 3x 16 Mbit/s)
 - 2x I²Cs (SMBus/PMBus)
- 11x timers: 1x 32-bit, 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- Development support: serial wire debug, JTAG and trace

Table 1. Device summary

Reference	Part number
STM32L151xE	STM32L151QE, STM32L151RE, STM32L151VE, STM32L151ZE
STM32L152xE	STM32L152QE, STM32L152RE, STM32L152VE, STM32L152ZE

Contents

1	Intro	Introduction 9			
2	Desc	Description			
	2.1	Device	overview	11	
	2.2	Ultra-lo	ow-power device continuum	12	
		2.2.1	Performance	12	
		2.2.2	Shared peripherals	12	
		2.2.3	Common system strategy	12	
		2.2.4	Features	12	
3	Fund	ctional c	overview	13	
	3.1	Low-po	ower modes	14	
	3.2	$ARM^{ ext{ ext{@}}}$	Cortex®-M3 core with MPU	18	
	3.3	Reset	and supply management	19	
		3.3.1	Power supply schemes	19	
		3.3.2	Power supply supervisor	19	
		3.3.3	Voltage regulator	20	
		3.3.4	Boot modes	20	
	3.4	Clock r	management	21	
	3.5	Low-po	ower real-time clock and backup registers	23	
	3.6	GPIOs	g (general-purpose inputs/outputs)	23	
	3.7	Memor	ries	24	
	3.8	DMA (direct memory access)	24	
	3.9	LCD (li	iquid crystal display)	25	
	3.10	ADC (a	analog-to-digital converter)	25	
			Temperature sensor		
		3.10.2	Internal voltage reference (V _{REFINT})	26	
	3.11	DAC (d	digital-to-analog converter)	26	
	3.12	Operat	tional amplifier	26	
	3.13	-	ow-power comparators and reference voltage		
	3.14		n configuration controller and routing interface		
	3.15	•	sensing		
			<u> </u>		



	3.16	Timers	and watchdogs	. 28
		3.16.1	General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)	28
		3.16.2	Basic timers (TIM6 and TIM7)	. 29
		3.16.3	SysTick timer	. 29
		3.16.4	Independent watchdog (IWDG)	. 29
		3.16.5	Window watchdog (WWDG)	. 29
	3.17	Commi	unication interfaces	. 29
		3.17.1	I ² C bus	. 29
		3.17.2	Universal synchronous/asynchronous receiver transmitter (USART) .	. 29
		3.17.3	Serial peripheral interface (SPI)	. 30
		3.17.4	Inter-integrated sound (I2S)	. 30
		3.17.5	Universal serial bus (USB)	. 30
	3.18	CRC (c	cyclic redundancy check) calculation unit	. 30
	3.19		pment support	
		3.19.1	Serial wire JTAG debug port (SWJ-DP)	
		3.19.2	Embedded Trace Macrocell TM	
4	Pin d	lescrinti	ions) Z
-		•	oping	
5	Mem	ory mar		. 55
5	Mem	ory mar	oping	. 55 . 56
5	Mem Elect	ory mar	aracteristics	. 55 . 56
5	Mem Elect	ory map crical ch	aracteristicseter conditions	. 55 . 56 . 56
5	Mem Elect	ory mar crical ch Parame 6.1.1	aracteristics eter conditions Minimum and maximum values	. 55 . 56 . 56
5	Mem Elect	ory mar crical ch Parame 6.1.1 6.1.2	aracteristics eter conditions Minimum and maximum values Typical values	. 55 . 56 . 56 . 56
5	Mem Elect	ory map crical ch Parame 6.1.1 6.1.2 6.1.3	aracteristics eter conditions Minimum and maximum values Typical values Typical curves	. 56 . 56 . 56 . 56
5	Mem Elect	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor	. 56 . 56 . 56 . 56 . 56
5	Mem Elect	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage	. 55 . 56 . 56 . 56 . 56 . 56 . 56
5	Mem Elect	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme	. 55 . 56 . 56 . 56 . 56 . 56 . 56 . 56 . 56
5	Mem Elect	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme Optional LCD power supply scheme	. 55 . 56 . 56 . 56 . 56 . 56 . 56 . 58
5	Mem Elect 6.1	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8 Absolut	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme Optional LCD power supply scheme Current consumption measurement	. 55 . 56 . 56 . 56 . 56 . 56 . 56 . 56 . 57 . 58 . 58
5	Mem Elect 6.1	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8 Absolut	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme Optional LCD power supply scheme Current consumption measurement te maximum ratings	. 55 . 56 . 56 . 56 . 56 . 56 . 57 . 58 . 59
5	Mem Elect 6.1	ory map crical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8 Absolut	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme Optional LCD power supply scheme Current consumption measurement te maximum ratings ing conditions	. 55 . 56 . 56 . 56 . 56 . 56 . 58 . 58 . 58 . 59 . 60
4 5 6	Mem Elect 6.1	ory map rical ch Parame 6.1.1 6.1.2 6.1.3 6.1.4 6.1.5 6.1.6 6.1.7 6.1.8 Absoluti Operati 6.3.1	aracteristics eter conditions Minimum and maximum values Typical values Typical curves Loading capacitor Pin input voltage Power supply scheme Optional LCD power supply scheme Current consumption measurement te maximum ratings ing conditions General operating conditions	. 55 . 56 . 56 . 56 . 56 . 56 . 56 . 56 . 57 . 58 . 58 . 59 . 60 . 60



9	Revi	sion His	story	132
8	Part	number	ring	131
		7.6.1	Reference document	130
	7.6	Therma	al characteristics	
	7.5		P104, 0.4 mm pitch wafer level chip scale package ation	126
	7.4	array p	A132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid backage information	123
	7.3		64, 10 x 10 mm, 64-pin low-profile quad flat package ation	120
	7.2		00, 14 x 14 mm, 100-pin low-profile quad flat package ation	117
	7.1		44, 20 x 20 mm, 144-pin low-profile quad flat package ation	114
7	Pack	cage info	ormation	114
		6.3.22	LCD controller	113
		6.3.21	Comparator	
		6.3.20	Temperature sensor characteristics	111
		6.3.19	Operational amplifier characteristics	109
		6.3.18	DAC electrical specifications	107
		6.3.17	12-bit ADC characteristics	102
		6.3.16	Communications interfaces	
		6.3.15	TIM timer characteristics	
		6.3.14	NRST pin characteristics	
		6.3.13	I/O port characteristics	
		6.3.11 6.3.12	I/O current injection characteristics	
		6.3.10	EMC characteristics Electrical sensitivity characteristics	
		6.3.9	Memory characteristics	
		6.3.8	PLL characteristics	
		6.3.7	Internal clock source characteristics	
		6.3.6	External clock source characteristics	
		6.3.5	Wakeup time from low-power mode	
		6.3.4	Supply current characteristics	64



List of tables

Table 1.	Device summary	1
Table 2.	Ultra-low-power STM32L151xE and STM32L152xE device features and peripheral	
	counts	
Table 3.	Functionalities depending on the operating power supply range	
Table 4.	CPU frequency range depending on dynamic voltage scaling	16
Table 5.	Functionalities depending on the working mode (from Run/active down to	
	standby)	
Table 6.	Timer feature comparison	28
Table 7.	Legend/abbreviations used in the pinout table	36
Table 8.	STM32L151xE and STM32L152xE pin definitions	37
Table 9.	Alternate function input/output	46
Table 10.	Voltage characteristics	59
Table 11.	Current characteristics	
Table 12.	Thermal characteristics	60
Table 13.	General operating conditions	
Table 14.	Embedded reset and power control block characteristics	
Table 15.	Embedded internal reference voltage calibration values	
Table 16.	Embedded internal reference voltage	
Table 17.	Current consumption in Run mode, code with data processing running from Flash	
Table 18.	Current consumption in Run mode, code with data processing running from RAM	
Table 19.	Current consumption in Sleep mode	
Table 20.	Current consumption in Low-power run mode	
Table 21.	Current consumption in Low-power sleep mode	
Table 22.	Typical and maximum current consumptions in Stop mode	
Table 23.	Typical and maximum current consumptions in Standby mode	
Table 24.	Peripheral current consumption	
Table 24.	Low-power mode wakeup timings	
Table 25.	High-speed external user clock characteristics.	
Table 20.	Low-speed external user clock characteristics	
Table 27.	HSE oscillator characteristics	
Table 26.		
	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	
Table 30. Table 31.		
	LSI oscillator characteristics	
Table 32.	MSI oscillator characteristics	
Table 33.	PLL characteristics	
Table 34.	RAM and hardware registers	
Table 35.	Flash memory and data EEPROM characteristics	
Table 36.	Flash memory and data EEPROM endurance and retention	
Table 37.	EMS characteristics	
Table 38.	EMI characteristics	
Table 39.	ESD absolute maximum ratings	
Table 40.	Electrical sensitivities	
Table 41.	I/O current injection susceptibility	
Table 42.	I/O static characteristics	
Table 43.	Output voltage characteristics	
Table 44.	I/O AC characteristics	
Table 45.	NRST pin characteristics	
Table 46.	TIMx characteristics	93



Table 47.	I ² C characteristics	94
Table 48.	SCL frequency (f _{PCI K1} = 32 MHz, V _{DD} = VDD_I2C = 3.3 V)	95
Table 49.	SPI characteristics	
Table 50.	USB startup time	99
Table 51.	USB DC electrical characteristics	99
Table 52.	USB: full speed electrical characteristics	99
Table 53.	I2S characteristics	100
Table 54.	ADC clock frequency	102
Table 55.	ADC characteristics	102
Table 56.	ADC accuracy	104
Table 57.	Maximum source impedance R _{AIN} max	106
Table 58.	DAC characteristics	107
Table 59.	Operational amplifier characteristics	109
Table 60.	Temperature sensor calibration values	111
Table 61.	Temperature sensor characteristics	111
Table 62.	Comparator 1 characteristics	111
Table 63.	Comparator 2 characteristics	112
Table 64.	LCD controller characteristics	113
Table 65.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data	115
Table 66.	LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data	117
Table 67.	LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data	120
Table 68.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array	
	package mechanical data	
Table 69.	WLCSP104, 0.4 mm pitch wafer level chip scale package mechanical data	127
Table 70.	WLCSP104, 0.4 mm pitch recommended PCB design rules	128
Table 71.	Thermal characteristics	129
Table 72.	STM32L151xE and STM32L152xE Ordering information scheme	131
Table 73.	Document revision history	132



List of figures

Figure 1.	Ultra-low-power STM32L151xE and STM32L152xE block diagram	13
Figure 2.	Clock tree	
Figure 3.	STM32L15xZE LQFP144 pinout.	
Figure 4.	STM32L15xQE UFBGA132 ballout	
Figure 5.	STM32L15xVE LQFP100 pinout	
-	·	
Figure 6.	STM32L15xRE LQFP64 pinout	
Figure 7.	STM32L15xVEY WLCSP104 ballout	
Figure 8.	Memory map	
Figure 9.	Pin loading conditions	
Figure 10.	Pin input voltage	
Figure 11.	Power supply scheme	
Figure 12.	Optional LCD power supply scheme	
Figure 13.	Current consumption measurement scheme	
Figure 14.	High-speed external clock source AC timing diagram	
Figure 15.	Low-speed external clock source AC timing diagram	
Figure 16.	HSE oscillator circuit diagram	
Figure 17.	Typical application with a 32.768 kHz crystal	
Figure 18.	I/O AC characteristics definition	
Figure 19.	Recommended NRST pin protection	93
Figure 20.	I ² C bus AC waveforms and measurement circuit	95
Figure 21.	SPI timing diagram - slave mode and CPHA = 0	
Figure 22.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	97
Figure 23.	SPI timing diagram - master mode ⁽¹⁾	98
Figure 24.	USB timings: definition of data signal rise and fall time	99
Figure 25.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	
Figure 26.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	101
Figure 27.	ADC accuracy characteristics	
Figure 28.	Typical connection diagram using the ADC	
Figure 29.	Maximum dynamic current consumption on V _{REF+} supply pin during ADC	
J	conversion	106
Figure 30.	12-bit buffered /non-buffered DAC	
Figure 31.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline	
Figure 32.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package	
9	recommended footprint	116
Figure 33.	LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example	
Figure 34.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline	
Figure 35.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package	
i igui o oo.	recommended footprint	118
Figure 36.	LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example	
Figure 37.	LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline	
Figure 38.	LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package	120
i iguic 50.	recommended footprint	121
Figure 39.	LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example	
Figure 39.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline.	
Figure 40.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package	123
ı ıgul e 4 I.	recommended footprint	104
Figure 42.	UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package	1 ∠ 4
ı ıyur e 4 2.		105
	top view example	1∠⊃



List of figures

STM32L151xE STM32L152xE

Figure 43.	WLCSP104, 0.4 mm pitch wafer level chip scale package outline	126
Figure 44.	WLCSP104, 0.4 mm pitch wafer level chip scale package recommended footprint	127
Figure 45.	WLCSP104, 0.4 mm pitch wafer level chip scale package top view example	128
Figure 46.	Thermal resistance suffix 6	130
Figure 47.	Thermal resistance suffix 7	130



1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xE and STM32L152xE ultra-low-power ARM® Cortex®-M3 based microcontroller product line. STM32L151xE and STM32L152xE devices are microcontrollers with a Flash memory density of 512 Kbytes.

The ultra-low-power STM32L151xE and STM32L152xE family includes devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xE and STM32L152xE microcontroller family suitable for a wide range of applications:

- · Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xE and STM32L152xE datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note "Getting started with STM32L1xxxx hardware development" (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM[®] Cortex[®]-M3 core please refer to the ARM[®] Cortex[®]-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.



2 Description

The ultra-low-power STM32L151xE and STM32L152xE devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 512 Kbytes and RAM up to 80 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xE and STM32L152xE devices offer two operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xE and STM32L152xE devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, three USARTs, two UARTs and an USB. The STM32L151xE and STM32L152xE devices offer up to 34 capacitive sensing channels to simply add a touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xE devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xE and STM32L152xE devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.



10/134 DocID025433 Rev 8

2.1 Device overview

Table 2. Ultra-low-power STM32L151xE and STM32L152xE device features and peripheral counts

Peripheral		STM32L15xRE	STM32L15xVE	STM32L15xQE	STM32L15xZE		
Flash (Kbytes)		512					
Data EEPROM (Kb	ytes)		1	6			
RAM (Kbytes)			8	0			
	32 bit	1					
Timers	General-purpose	6					
	Basic		2	2			
	SPI		8(3	3) ⁽¹⁾			
	I ² S		2	2			
Communication interfaces	I ² C		2	2			
	USART		ţ	5			
	USB		•	1			
GPIOs		51	83	109	115		
Operational amplif	fiers		2	2			
12-bit synchronize Number of channe		1 21	1 25	1 40	1 40		
12-bit DAC Number of channe	ıls	2 2					
LCD ⁽²⁾ COM x SEG		1 4x32 or 8x28	1 4x44 or 8x40				
Comparators			2	2			
Capacitive sensing	g channels	23 33		34			
Max. CPU frequen	су	32 MHz					
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option					
Operating tempera	atures	Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 to + 110 °C					
Packages		LQFP64	LQFP100, WLCSP104	UFBGA132	LQFP144		

^{1. 5} SPIs are USART configured in synchronous mode emulating SPI master.

^{2.} STM32L152xx devices only.



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer the user needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

Note:

STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, the old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

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12/134 DocID025433 Rev 8

3 Functional overview

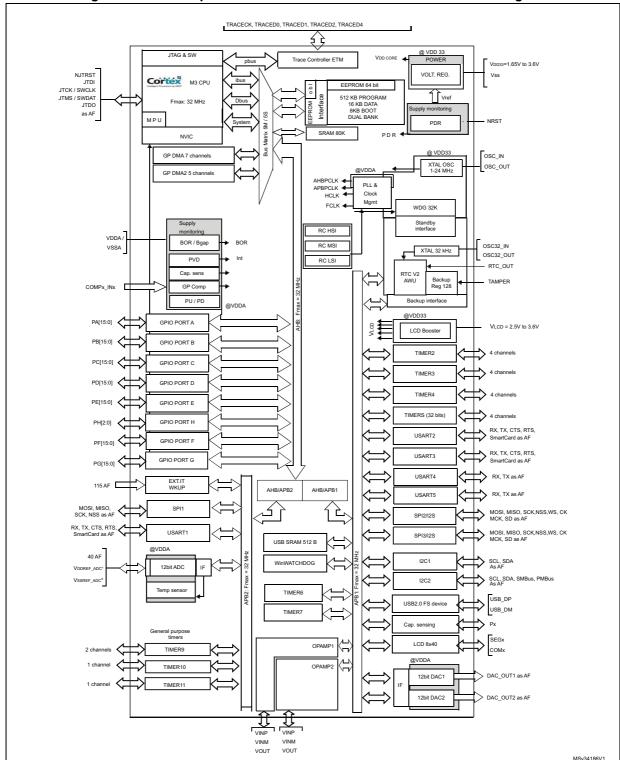


Figure 1. Ultra-low-power STM32L151xE and STM32L152xE block diagram



3.1 Low-power modes

The ultra-low-power STM32L151xE and STM32L152xE devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71 V 3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4 MHz (generated only with the multispeed internal RC oscillator clock source)

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

• Low-power run mode

This mode is achieved with the multispeed internal (MSI) RC oscillator set to the minimum clock (131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

• Low-power sleep mode

This mode is achieved by entering Sleep mode with the internal voltage regulator in Low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

Stop mode with RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

47/

Stop mode without RTC

Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 μ s. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

• Standby mode with RTC

Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC CSR).

The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

Standby mode without RTC

Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

The device exits Standby mode in $60~\mu s$ when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note:

The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
V _{DD} = V _{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V _{DD} =V _{DDA} = 1.71 to 1.8 V ⁽¹⁾	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
$V_{DD} = V_{DDA} = 1.8 \text{ to } 2.0 \text{ V}^{(1)}$	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance



Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range			
Operating power supply range	DAC and ADC operation	USB	Dynamic voltage scaling range	I/O operation
$V_{DD} = V_{DDA} = 2.0 \text{ to } 2.4 \text{ V}$	Conversion time up to 500 Ksps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation
V _{DD} =V _{DDA} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional ⁽²⁾	Range 1, Range 2 or Range 3	Full speed operation

CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 μs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 μs, then switch from 16 MHz to 32 MHz.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

^{2.} Should be USB compliant from I/O voltage standpoint, the minimum $\rm V_{\rm DD}$ is 3.0 V.

Table 5. Functionalities depending on the working mode (from Run/active down to standby)

lps	Run/Active	Sleep	Low- power Run	Low- power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Υ		Υ					
Flash	Υ	Y	Y	Y	-		-	
RAM	Y	Y	Y	Y	Υ			
Backup Registers	Y	Y	Y	Y	Υ		Υ	
EEPROM	Y	Y	Y	Y	Υ			
Brown-out rest (BOR)	Υ	Y	Υ	Y	Υ	Y	Y	
DMA	Y	Y	Y	Y			-	
Programmable Voltage Detector (PVD)	Υ	Y	Y	Y	Y	Y	Y	
Power On Reset (POR)	Y	Y	Y	Y	Υ	Y	Υ	
Power Down Rest (PDR)	Y	Y	Y	Y	Υ		Y	
High Speed Internal (HSI)	Y	Υ						
High Speed External (HSE)	Y	Υ						
Low Speed Internal (LSI)	Y	Y	Υ	Y	Υ		Y	
Low Speed External (LSE)	Y	Y	Υ	Y	Υ		Y	
Multi-Speed Internal (MSI)	Y	Y	Υ	Y				
Inter-Connect Controller	Y	Y	Υ	Y				
RTC	Υ	Υ	Y	Y	Υ	Y	Υ	
RTC Tamper	Υ	Υ	Y	Υ	Υ	Y	Υ	Y
Auto WakeUp (AWU)	Y	Y	Υ	Y	Υ	Y	Y	Y
LCD	Υ	Y	Υ	Υ	Υ		I	
USB	Υ	Y				Y	ł	
USART	Υ	Υ	Υ	Υ	Υ	(1)	1	
SPI	Υ	Υ	Y	Υ			-	
I2C	Υ	Υ	Y	Y		(1)		



Table 5. Functionalities depending on the working mode (from Run/active down to
standby) (continued)

lps	Run/Active	Sleep	Low- power Run	Low- power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
ADC	Y	Y						
DAC	Y	Y	Y	Y	Υ			
Tempsensor	Y	Y	Y	Y	Υ			
OP amp	Y	Y	Y	Y	Υ			
Comparators	Y	Y	Y	Y	Υ	Υ		
16-bit and 32-bit Timers	Y	Y	Y	Y				
IWDG	Y	Y	Υ	Y	Υ	Υ	Υ	Y
WWDG	Y	Y	Y	Y				
Touch sensing	Y	Y						
Systic Timer	Y	Y	Υ	Y				
GPIOs	Y	Y	Υ	Y	Υ	Y		3 pins
Wakeup time to Run mode	0 µs	0.4 µs	3 µs	46 µs	< 8 µs		58 µs	
Consumption V _{DD} =1.8 to 3.6 V (Typ)	Down to 195 μΑ/ΜΗz (from Flash)	Down to 38 μA/MHz (from Flash)	Down to 11 μA	Down to 4.6 μA	0.53 μA (no RTC) V _{DD} =1.8V		0.285 μA (no RTC) V _{DD} =1.8V	
					1.2 μA (with RTC) V _{DD} =1.8V		0.97 μA (with RTC) V _{DD} =1.8V	
					0.56 μΑ (no RTC) V _{DD} =3.0V		0.29 μA (no RTC) V _{DD} =3.0V	
					(v	with RTC) (with		1.11 µA vith RTC) _{DD} =3.0V

The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

18/134 DocID025433 Rev 8



The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xE and STM32L152xE devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xE and STM32L152xE devices embed a nested vectored interrupt controller able to handle up to 56 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the



power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for any external reset circuit.

Note:

The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot from Flash usually boots at the beginning of the Flash (bank 1). An additional boot mechanism is available through user option byte, to allow booting from bank 2 when bank 2 contains valid code. This dual boot capability can be used to easily implement a secure field software update mechanism.

The boot loader is located in System memory. It is used to reprogram the Flash memory by using USART1, USART2 or USB. See Application note "STM32 microcontroller system memory boot mode" (AN2606) for details.



3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- System clock source: three different clock sources can be used to drive the master clock SYSCLK:
 - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
 - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
 - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz).
 When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- Auxiliary clock source: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
 - 32.768 kHz low-speed external crystal (LSE)
 - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog.
 The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- RTC and LCD clock sources: the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- Clock security system (CSS): this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- Clock-out capability (MCO: microcontroller clock output): it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

I Standby supplied voltage domain Watchdog LSI tempo LSI BC LSE OSC LSE tempo Radio Sleep Time Radio Sleep Timer enable LS LS LS LS 1 MHz LCD enable → @V33 ADC enable MSI BC ck_lsi level shifters @V_{DDCORE} / 1,2,4,8,16 / 2,4,8,16 @ V33 not deepsleep HSI RC level shifters @V_{DDCORE} deepsleep not (sleep or deepsleep) @V33 HSE OSC ck hsi AHB level shifters prescaler / 1,2,..512 @V_{DDCORE} @V33 ck_p APB1 prescaler / 1,2,4,8,16 PLL X 3,4,6,8,12 16,24,32,48 APB2 prescaler / 1,2,4,8,16 @V33 ↓ 1 MHz clock / 2, 3, 4 detector Clock @V_{DDCORE} source HSE present or not CK_USB48 ck_usb = Vco / 2 (Vco must be atz96 MH CK_TIMTGO if (APB1 presc = 1)x1 else x2 apb2 periphen and (not deepsleep) MS18583V1

Figure 2. Clock tree

 For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 24 MHz or 32 MHz.



3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 115 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.



3.7 Memories

The STM32L151xE and STM32L152xE devices have the following features:

- 80 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
 - 512 Kbytes of embedded Flash program memory
 - 16 Kbytes of data EEPROM
 - Options bytes

Flash program and data EEPROM are divided into two banks, this enables writing in one bank while running code or reading data in the other bank.

The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose timers, DAC and ADC.

5//

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xE and STM32L152xE devices with up to 40 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 28 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are