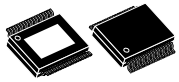
# VNHD7008AY

## H-bridge motor driver for automotive DC motor driving

**Datasheet - production data**



PowerSSO-36

GAPGCFT00004

## Features

| Type | $R_{DS(on)}$ | $I_{out}$ | $V_{CCmax}$ |
|---|---|---|---|
| VNHD7008AY | 8 mΩ typ (per channel) | 51 A | 38 V |

- AEC-Q100 qualified
- Output current: 51 A
- Dual fully protected HSD with MultiSense feedback
- Two integrated drivers for the external LSDs
- 3 V CMOS compatible inputs
- Protections:
  - Undervoltage shutdown
  - Overvoltage clamp
  - Thermal shutdown
  - Load current limitation
  - Self-limiting of fast thermal transients (Power Limitation)
  - Cross current protection
  - Shoot through protection
  - Loss of ground and loss of $V_{CC}$
  - Electrostatic discharge protection
  - Drain and source voltage monitoring of the external power MOSFETs, configurable via an external resistance (short-to-battery protection)
- PWM operation up to 20 kHz for external LSDs
- MultiSense monitoring functions
  - Analog motor current feedback
  - Chip temperature monitoring
  - Battery voltage monitoring
- MultiSense diagnostic functions
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to $V_{CC}$ detection
- Standby mode
- Half bridge operation
- Charge pump output for reverse battery protection
- Package: ECOPACK®

## Description

The device is a DC motor driver for automotive applications. It integrates a full protected dual high-side driver and the drivers and protections for the two external power MOSFETs in low-side configuration.

The device is designed using STMicroelectronics well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true PowerMOSFET with an intelligent signal/ protection circuitry. The device is housed in a PowerSSO-36 exposed pad package to optimize the dissipation performances.

The input signals $IN_A$ and $IN_B$ can directly interface the microcontroller to select the motor direction and the brake conditions. Two selection pins (SEL0 and SEL1) are available to address to the microcontroller the information available on the MultiSense. The MultiSense pin allows to monitor the motor current, provides a voltage proportional to the battery value and the information on the temperature of the chip. The integrated protections are: load current limitation, overload active power limitation (with latch-off), overtemperature shutdown (with latch-off) and cross current protection.

# Contents

# List of tables

# List of figures

# 1 Block diagram and pin description

**Figure 1. Block diagram**

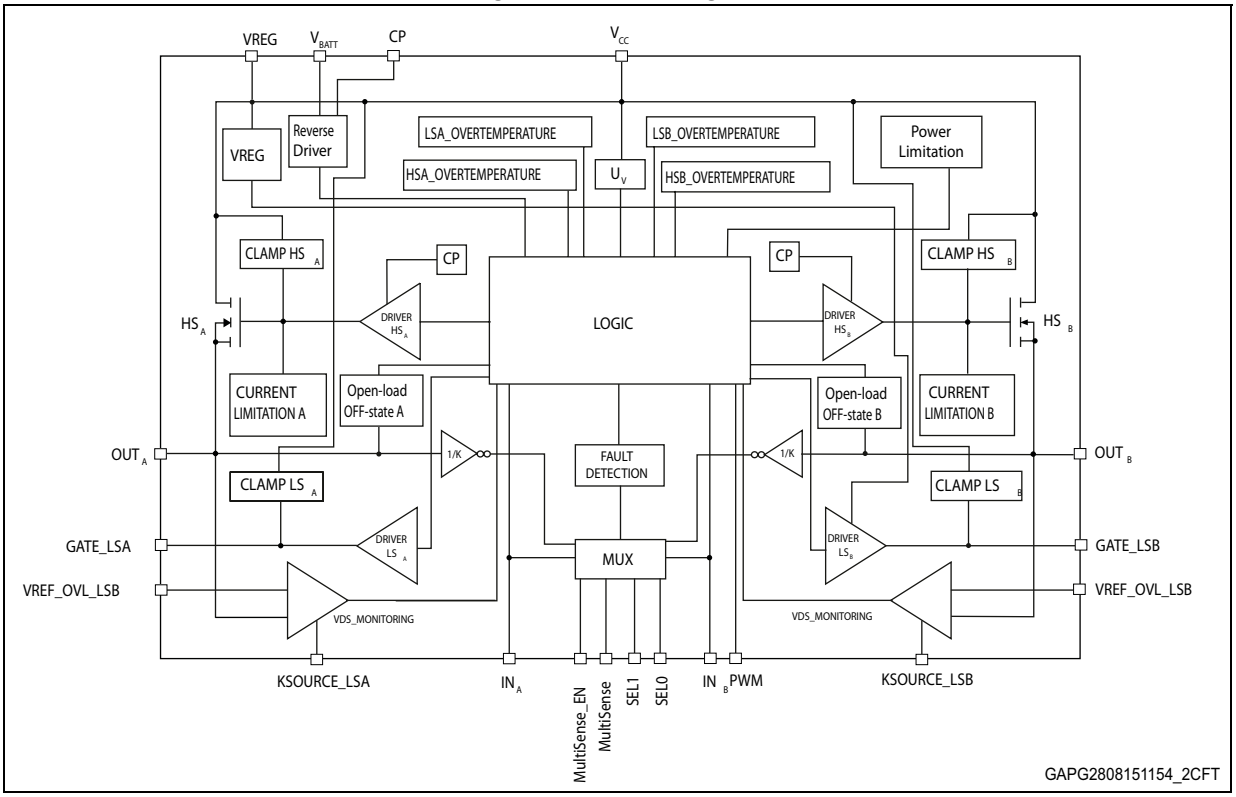



**Table 1. Block description**

| Name | Description |
|---|---|
| Logic control | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table. |
| Undervoltage ($U_S$) | Shuts down the device for battery voltage below (4 V). |
| High-side and low-side clamp voltage | Protect the high-side and the low-side switches from the high voltage on the battery line. |
| High-side and low-side driver | Drive the gate of the concerned switch to allow a proper $R_{on}$ for the leg of the bridge. |
| Current limitation | Limits the motor current in case of short circuit. |
| High-side overtemperature protection | In case of short-circuit with the increase of the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die. |
| VDS_MONITORING | Protection of LSD powers against short to battery failure |
| VREG | Internal voltage regulator that provides the supply for the gates of the external low-side switches |
| Fault detection | Signalizes an abnormal condition of the power stage (output shorted to ground or output shorted to battery) by a feedback on the MultiSense |

**Table 1. Block description (continued)**

| Name | Description |
|---|---|
| Power limitation | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition. |
| Open-load in OFF-state | Signalize, in combination with an external resistor, an open-load when the switches are off by a feedback on the MultiSense |
| $T_{chip}$ monitoring | Provides a signal linked to the Chip temperature by a feedback on the MultiSense |
| $V_{CC}$ monitoring | Provides a signal linked to the Chip temperature by a feedback on the MultiSense |
| Reverse driver | Drives an external PowerMOSFET to provide the reverse battery protection |
| CP | Charge pump to drive the external N-MOSFET used on the battery track for the reverse battery protection.<br>The N-MOSFET source must be connected to the $V_{batt}$ pin. |

**Figure 2. Configuration diagram (top view)**

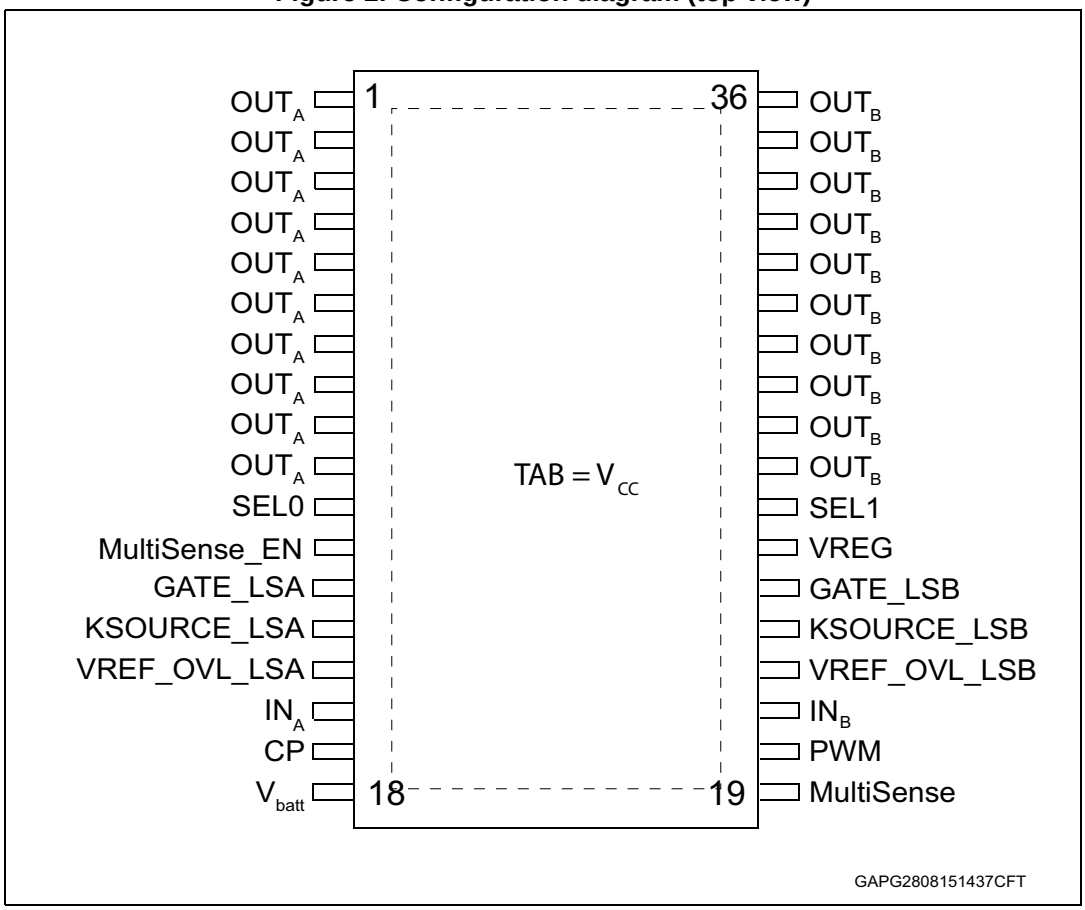


**Table 2. Pin definitions and functions**

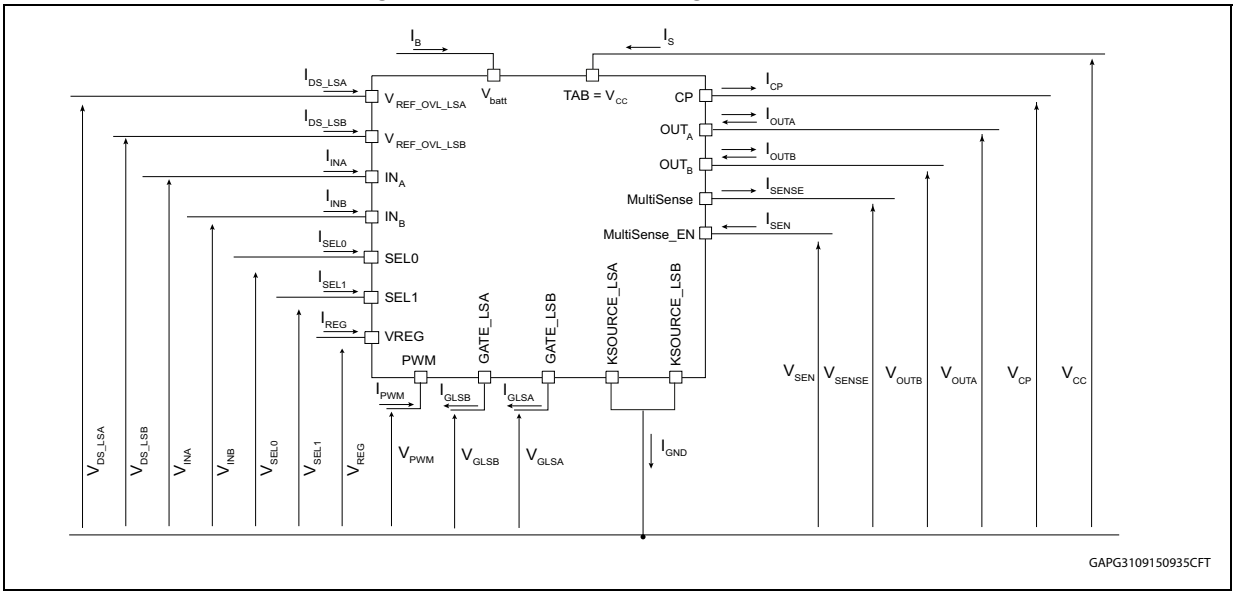
| Pin N° | Symbol | Function |
|---|---|---|
| 20 | PWM | PWM input. |
| 25 | VREG | Internal supply output |
| 16 | $IN_A$ | Clockwise input. |
| 18 | $V_{batt}$ | Battery supply, connection to the source of the external PowerMOS used for the reverse battery protection |
| 19 | MultiSense | Output of current sense and diagnostic feedback |
| 12 | MultiSense_EN | Enables the MultiSense diagnostic pin |
| 11 | SEL0 | Address the MultiSense multiplexer (refer to *Table 12*) |
| 26 | SEL1 | Address the MultiSense multiplexer (refer to *Table 12*) |
| 21 | $IN_B$ | Counter clockwise input. |
| 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 | $OUT_A$ | Source of high-side switch A |
| 27, 28, 29, 30, 31, 32, 33, 34, 35, 36 | $OUT_B$ | Source of high-side switch B |
| 17 | CP | Drives the gate of external P-MOSFET for the reverse battery protection |
| 15 | VREF_OVL_LSA | Sets the threshold for VDS_MONITORING feature for LSA |
| 22 | VREF_OVL_LSB | Sets the threshold for VDS_MONITORING feature for LSB |
| 13 | GATE_LSA | Gate driver of the external PowerMOS LSA |
| 24 | GATE_LSB | Gate driver of the external PowerMOS LSB |
| 14 | KSOURCE_LSA | Source of external LSA. Ground connection |
| 23 | KSOURCE_LSB | Source of external LSB. Ground connection |
| TAB | $V_{CC}$ | Supply voltage. Drain of the high-side switches and connection to the drain of the external PowerMOS used for the reverse battery protection |

**Table 3. Suggested connection for unused and not connected pins**

| Connection / pin | OUTA, OUTB | Inx, PWM, SELx, Multisense_EN | Multisense | GATE_LSA, GATE_LSB, CP, VREG | VREF_OVL_LSA, VREF_OVL_LSB |
|---|---|---|---|---|---|
| Floating | X | X | X | X | X |
| To ground | Not allowed | Through 10 kΩ resistor | | Not allowed | X |

# 2 Electrical specifications

**Figure 3. Current and voltage conventions**




## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | H-Bridge supply voltage | 38 | V |
| $V_{BAT}$ | Maximum battery voltage(1) | -16 to 38 | V |
| $I_{max}$ | DC output current | Internally limited | A |
| $I_R$ | Reverse output current (continuous)(2) | 30 | A |
| $I_{IN}$ | Input current ($IN_A$ and $IN_B$ pins) | -1 to 10 | mA |
| $I_{SEL}$ | $SEL_{0,1}$ DC input current | -1 to 10 | mA |
| $I_{PWM}$ | PWM Input current | -1 to 10 | mA |
| $I_{MultiSense\_EN}$ | SenseEnable DC input current | -1 to 1.5 | mA |
| $I_{MultiSense}$ | MultiSense pin DC output current ($V_{GND}$ = $V_{CC}$ and $V_{SENSE}$ < 0 V) | 10 | mA |
| | MultiSense pin DC output current in reverse ($V_{CC}$ < 0 V) | -20 | mA |
| $V_{REG}$ | $V_{REG}$ DC voltage | 12 | V |

**Table 4. Absolute maximum ratings (continued)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CP}$ | $V_{CP}$ DC voltage | $V_{BATT}$ -6 to $V_{BATT}$ +14 | V |
| VGATE_LSx | GATE_LAS, GATE_LSB DC voltage | 12 | V |
| VREF_OVL_LSx | VREF_OVL_LSA, VREF_OVL_LSB input current | -1 to 10 | V |
| $V_{ESD}$ | Electrostatic discharge (Human body model: R = 1.5 kΩ; C = 100 pF)<br>– MultiSenseVREG, VREF_OVL_LSx<br>– $IN_A$, $IN_B$, $OUT_A$, $OUT_B$, PWM, SEL0, SEL1, SENSE_EN<br>– GATE_LSx | <br>2<br>4<br>4 | kV |
| $T_c$ | Junction operating temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature | -55 to 150 | °C |
| $I_{K\_SOURCE\_LSx}$ | DC reverse ground pin current (per leg) | 100 | mA |

1. This applies with the n-channel MOSFET used for the reverse battery protection. Otherwise $V_{BAT}$ has to be shorted to $V_{CC}$.
2. Based on the internal wires capability.

*All logic pins cannot be left floating but they must be connected to GND if unused.*

## 2.2 Thermal data

**Table 5. Thermal data**

| Symbol | Parameter | Max. value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case (per leg channel) (JEDEC JESD 51-8) | 2.4 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-5)(1) | 50.6 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-7) | 16.6 | °C/W |

1. Device mounted on two-layers 2s0p PCB with 2 $cm^2$.heatsink copper trace.

## 2.3 Electrical characteristics

$V_{CC}$ = 7 V up to 28 V; -40 °C < $T_j$ < 150 °C, unless otherwise specified.

**Table 6. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 4 | | 28 | V |
| $I_S$ | Supply current | Off-state standby<br>$IN_A$ = $IN_B$ = PWM = Multisense_EN= 0;<br>$SEL_{0,1}$ = 0; $T_j$ = 25 °C; $V_{CC}$ = 13 V | | | 1 | µA |
| | | Off-state standby;<br>$IN_A$ = $IN_B$ = PWM = Multisense_EN= 0;<br>$SEL_{0,1}$ = 0; $V_{CC}$ = 13 V; $T_j$ = 85 °C | | | 1 | µA |
| | | Off-state standby;<br>$IN_A$ = $IN_B$ = PWM = Multisense_EN= 0;<br>$SEL_{0,1}$ = 0; $V_{CC}$ = 13 V; $T_j$ = 125 °C | | | 10 | µA |
| | | Off-state (no standby)<br>$IN_A$ = $IN_B$ = PWM = Multisense_EN= 0;<br>$SEL_{0,1}$ = 5 V | | 4 | 8 | mA |
| | | On-state: $IN_A$ or $IN_B$ = 5V;<br>PWM = 0 V or PWM = 5 V;<br>$SEL_0$ = 0 or $SEL_0$ = 5 V;<br>$SEL_1$ = 0 or $SEL_1$ = 5 V | | 6 | 12 | mA |
| | | On-state: $IN_A$ = $IN_B$ = 5V;<br>PWM = 0 V or PWM = 5 V;<br>$SEL_0$ = 0 or $SEL_0$ = 5 V;<br>$SEL_1$ = 0 or $SEL_1$ = 5 V | | 9 | 18 | mA |
| $t_{D\_STBY}$ | Standby mode blanking time | $V_{CC}$ = 13 V; $IN_A$ = $IN_B$ = $SEL_1$ =<br>MultiSense_EN = PWM = 0 V;<br>$V_{SEL0}$ from 5 V to 0 V. | 60 | 300 | 550 | µs |
| $R_{ONHS}$ | Static high-side resistance | $I_{OUT}$ = 12 A; $T_j$ = 25 °C,<br>$V_{CC}$ = 13 V | | 8 | | mΩ |
| | | $I_{OUT}$ = 12 A;<br>$T_j$ = - 40 °C to 150 °C | | | 16 | mΩ |
| | | $V_{CC}$ = 4 V, $I_{OUT}$ = 12 A, Tj=25 °C | | 8 | | |
| $V_f$ | High-side free-wheeling diode forward voltage | $I_{OUT}$ = -12 A; $T_j$ = 150 °C | | 0.6 | 0.7 | V |
| $I_{L(off)}$ | Off-State Output current of one output | $IN_A$ = $IN_B$ = PWM = 0; $V_{OUT}$ = 0 V;<br>$V_{CC}$ = 13 V; $T_j$ = 25 °C | 0 | | 0.5 | µA |
| | | $IN_A$ = $IN_B$ = PWM = 0; $V_{OUT}$ = 0 V;<br>$V_{CC}$ = 13 V; $T_j$ = 125°C | 0 | | 5 | µA |
| $I_{L(off\_h)}$ | Off-state output current of one output with other HSD on | $IN_A$ = PWM = 0; $IN_B$ = 5 V; $V_{CC}$ = 13 V | 20 | | 60 | µA |

**Table 7. Logic inputs ($IN_A$, $IN_B$) ($V_{CC}$ = 7 V up to 28 V; -40 °C < $T_j$ < 150 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | | | | 0.9 | V |
| $V_{IH}$ | Input high level voltage | | 2.1 | | | V |
| $V_{IHYST}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | V |
| $I_{INL}$ | Input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $I_{INH}$ | Input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| **$SEL_0$, $SEL_1$ ($V_{CC}$ = 7 V up to 18 V; -40 °C < $T_j$ < 150 °C)** | | | | | | |
| $V_{SELL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SELL}$ | Low level input current | $V_{SEL}$ = 0.9 V | 1 | | | µA |
| $V_{SELH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SELH}$ | High level input current | $V_{SEL}$ = 2.1 V | | | 10 | µA |
| $V_{SEL(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SELCL}$ | Input clamp voltage | $I_{SEL}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{SEL}$ = -1 mA | | -0.7 | | V |
| **PWM ($V_{CC}$ = 7 V up to 28 V; -40 °C < $T_j$ < 150 °C)** | | | | | | |
| $V_{PWM}$ | Input low level voltage | | | | 0.9 | V |
| $I_{PWM}$ | Low level input current | $V_{PWM}$ = 0.9 V | 1 | | | µA |
| $V_{PWM}$ | Input high level voltage | | 2.1 | | | V |
| $I_{PWMH}$ | High level input current | $V_{PWM}$ = 2.1 V | | | 10 | µA |
| $V_{PWM(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{PMWCL}$ | Input clamp voltage | $I_{PWM}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{PWM}$ = -1 mA | | -0.7 | | V |
| **MultiSense_EN ($V_{CC}$ = 7 V up to 18 V; -40 °C < $T_j$ < 150 °C)** | | | | | | |
| $V_{SEnL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SEnL}$ | Low level input current | $V_{SEn}$ = 0.9 V | 1 | | | µA |
| $V_{SEnH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SEnH}$ | High level input current | $V_{SEn}$ = 2.1 V | | | 10 | µA |
| $V_{SEn(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SEnCL}$ | Input clump voltage | $I_{SEn}$ = 1 mA | 5.3 | | 7.5 | V |
| | | $I_{SEn}$ = -1 mA | | -0.7 | | V |

**Table 8. HSD switching ($V_{CC}$ = 13 V; RLOAD = 1.1 Ω)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*) | | 53 | | µs |
| $t_{d(off)}$ | Turn-off delay time | Input rise time < 1 µs; MultiSense_EN = 5 V (no standby); $SEL_{0,1}$ = 0; PWM = 0 (see *Figure 6*) | | 20 | | µs |

**Table 9. Gate driver for external MOS parameters ($V_{CC}$ = 13 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| f(1) | PWM frequency | | 0 | | 20 | kHz |
| $V_{gs\_lsd}$ | Gate_LSD voltage | PWM = 5 V; $IN_x$ = 0 V | | | 10 | V |
| | | $V_{CC}$ = 4 V, PWM = 5 V, $I_{Nx}$ = 0 V, Tj=25 °C | | 4 | | V |
| $t_{cross}$ | Low-side turn-on delay time | Input rise time < 1 µs (see *Figure 7*) | 40 | 160 | 300 | µs |
| $t_{gr\_ls}$ | Rise time | $V_{CC}$ = 13.5 V; $R_g$ = 0 Ω; $C_g$ = 4.7 nF (see *Figure 5*) | | 0.25 | 0.5 | µs |
| $t_{gf\_ls}$ | Fall time | $V_{CC}$ = 13.5 V; $R_g$ = 0 Ω; $C_g$ = 4.7 nF (see *Figure 5*) | | 0.35 | 0.5 | µs |

1. Parameter guaranteed by design.

**Table 10. Protections and diagnostics (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{USD}$ | Undervoltage shutdown | $V_{CC}$ falling | | | 4 | V |
| $V_{USDreset}$ | Undervoltage shutdown reset | $V_{CC}$ rising | | | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.3 | | V |
| $I_{LIM\_HSD}$ | High-side current limitation | | 51 | 77 | 110 | A |
| | | $V_{CC}$ = 4 V, Tj=25 °C (1) | | 66 | | A |
| $V_{CL\_HSD}$ | High-side driver clamp voltage ($V_{CC}$ to $OUT_A$ = 0 or $OUT_B$ = 0) | $I_{OUT}$ = 100 mA; $t_{clamp}$ = 1 ms; $I_{clamp}$ = 100 mA | 38 | 46 | | V |
| $V_{CL\_LSD}$(1) | Low-side clamp voltage ($OUT_A$ = $V_{CC}$ or $OUT_B$ = $V_{CC}$ to GND) | $I_{OUT}$ = 100 mA; $t_{clamp}$ = 1 ms; $I_{clamp}$ = 100 mA | 38 | 46 | 52 | V |
| $t_{DEL\_OVL\_LSD}$ | Low-side drain-current overload blanking time | | 1 | | 5 | µs |

**Table 10. Protections and diagnostics (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{REF\_OVL\_LSD}$ | Low-side drain-current overload reference current | | 40 | 50 | 60 | µA |
| $V_{REF\_OVL\_LSD\_MIN}$ | Low-side drain-current overload threshold voltage minimum | | 0.32 | 0.4 | 0.8 | V |
| $V_{REF\_OVL\_LSD\_MAX}$ | Low-side drain-current overload threshold voltage maximum | | 1.6 | 2 | 2.4 | V |
| $T_{TSD\_HSD}$ | High-side thermal shutdown temperature | $IN_x$ = 2.1 V | 150 | 175 | 200 | °C |
| $T_{TR\_HSD}$ | High-side thermal reset temperature | | 135 | | | °C |
| $T_{HYST\_HSD}$ | High-side thermal hysteresis ($T_{SD\_HSD}$ - $T_{R\_HSD}$) | | | 7 | | °C |
| $\Delta T_{j\_SD}$ (1) | Dynamic temperature | | | 60 | | °C |
| $I_{L(off3)}$ | OFF-state output sink current with $V_{OUT}$ = $V_{CC}$ | $IN_A$ = $IN_B$ = 0; PWM = 0; $V_{OUT}$ = $V_{CC}$ | 0 | 1.1 | 2.5 | mA |
| $V_{CL}$ | Clamp signal ($V_{CC}$ to GND) | $I_{OUT}$ = 100 mA; $t_{clamp}$ = 1 ms; $I_{clamp}$ = 100 mA | 38 | 46 | 52 | V |
| $V_{OL}$ | OFF-state open-load voltage detection threshold | $IN_A$ = $IN_B$ = 0; PWM = 0; $V_{SEL0}$ = 5 V for CHA; $V_{SEL0}$ = 0 V and within $t_{D\_STBY}$ for CHB | 2 | 3 | 4 | V |
| $I_{L(off2)}$ | OFF-state output sink current | $IN_A$ = $IN_B$ = 0; $V_{OUT}$ = 2 V; PWM = 2 V; $V_{SEL0}$ = 5 V for CHA; $V_{SEL0}$ = 0 V and within $t_{D\_STBY}$ for CHB | -150 | | -5 | µA |
| $t_{DSTKON}$ | OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 4*) | INA = 5 V to 0 V; $IN_B$ = 0; PWM = 0; $V_{SEL0}$ = 5 V; $I_{OUT}$ = 0 A; $V_{OUTA}$ = 4 V | 40 | 160 | 300 | µs |
| $V_{GS\_CP}$ | CP output voltage | $V_{CP}$ - $V_{BAT}$ = $V_{GS\_CP}$ | 8 | 12 | 15 | V |
| | | $V_{BAT}$ = -16 V; $V_{CP}$ - $V_{BAT}$ = $V_{GS\_CP}$ | | 0.6 | | V |
| $t_{D\_VOL}$ | OFF-state diagnostic delay time from rising edge of $V_{OUT}$ (see *Figure 10*) | $IN_A$ = $IN_B$ = 0 V; PWM = 0; $V_{OUTx}$ = 0 V to 4 V; $V_{SEL1}$ = 0 V for CHA; $V_{SEL0,1}$ = 0 V; SENSE_EN = 5 V for CHB | | 5 | 30 | µs |
| $t_{LATCH\_RST\_HS}$ | Input reset time for high-side fault unlatch | $V_{INx}$ = 5 V to 0 V; HSDx faulting (see *Figure 8*) | 3 | 10 | 20 | µs |

**Table 10. Protections and diagnostics (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{LATCH\_RST\_LS}$ | Input reset time for low-side fault unlatch | $V_{INx}$ = 0 V to 5 V; LSDx faulting (see *Figure 9*) | 3 | 10 | 20 | µs |
| $t_{stby\_ovl\_lsd}$ | Low-side drain current overload delay time form stby exit | 50% of $V_{SENSEH}$ | | 20 | | µs |

1. Parameter guaranteed by design and characterization; not subject to production test.

**Table 11. MultiSense (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE\_CL}$ | MultiSense clamp voltage | $V_{SEn}$ = 0 V; $I_{SENSE}$ = -1 mA | | 7 | | V |
| | | $V_{SEn}$ = 0 V; $I_{SENSE}$ = 1 mA | -17 | | -12 | V |
| $K_{OL}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.25 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40 °C to 150 °C | 6300 | 10500 | 14700 | |
| $K_0$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 2 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40 °C to 150 °C | 8400 | 10900 | 13400 | |
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 6 A; $V_{SENSE}$ = 0.5; $T_j$ = -40 °C to 150 °C | 8700 | 11000 | 13200 | |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 12 A; $V_{SENSE}$ = 4 V; $T_j$ = -40 °C to 150 °C | 9000 | 11000 | 13000 | |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 24 A; $V_{SENSE}$ = 4 V; $T_j$ = -40 °C to 150 °C | 9200 | 11000 | 12200 | |
| $dK_{OL}/K_{OL}$ (1) | Analog sense current drift | $I_{OUT}$ = 0.25 A; $V_{SENSE}$ = 0.5 V; $T_j$ = -40 °C to 150 °C | -25 | | 25 | % |
| $dK_0/K_0$ (1) | Analog sense current drift | $I_{OUT}$ = 2 A; $V_{SENSE}$ = 0.5 V; $V_{SENSE\_EN}$ = 0 V; $T_j$ = -40 °C to 150 °C | -5 | | 5 | % |
| $dK_1/K_1$ (1) | Analog sense current drift | $I_{OUT}$ = 6 A; $V_{SENSE}$ = 0.5 V; $V_{SENSE\_EN}$ = 0 V; $T_j$ = -40 °C to 150 °C | -5 | | 5 | % |
| $dK_2/K_2$ (1) | Analog sense current drift | $I_{OUT}$ = 12 A; $V_{SENSE}$ = 4 V; $T_j$ = -40 °C to 150°C | -5 | | 5 | % |
| $dK_3/K_3$ (1) | Analog sense current drift | $I_{OUT}$ = 24 A; $V_{SENSE}$ = 4 V; $T_j$ = -40 °C to 150°C | -5 | | 5 | % |
| $V_{SENSE\_SAT}$ | Max analog sense output voltage | $V_{CC}$ = 7 V; $R_{SENSE}$ = 10 kΩ; $I_{OUT}$ = 24 A; $V_{SEL0}$ = 5 V; $T_j$ = 150 °C | 5 | | | V |
| $I_{SENSE\_SAT}$ (2) | MultiSense saturation current | $V_{CC}$ = 7 V; $V_{INA}$ = 5 V; $V_{INB}$ = 0 V; $V_{SEL0}$ = 5 V; $T_j$ = 150°C | 4 | | | mA |
| $I_{OUT\_SAT}$ (2) | Output saturation current | $V_{CC}$ = 7 V; $V_{SENSE}$ = 4 V; $V_{INA}$ = 5 V; $V_{INB}$ = 0 V; $V_{SEL0}$ = 5 V; $T_j$ = 150°C | 48 | | | A |

**Table 11. MultiSense (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OUT\_MSD}$ (2) | Output Voltage for MultiSense shutdown | $V_{INA}$ = 5 V; $V_{INB}$ = 0 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 0 V; $R_{SENSE}$ = 2.7 kΩ; $I_{OUT}$ = 24 A | | 5 | | V |
| $I_{SENSE0}$ | MultiSense leakage current | $V_{MultiSense}$ = $V_{SENSE\_EN}$ = PWM = 0 V; $IN_A$ = $IN_B$ =0 V; $SEL_0$ = $SEL_1$ = 0; $T_j$ = -40 °C to 150°C (standby) | 0 | | 0.5 | µA |
| | | SEn = 5 V; $IN_A$ = $IN_B$ = 5 V; PWM = 0 V; SideX diagnostic selected; $I_{OUTx}$ = 0 A<br>E.g.<br>– SideA: SEL0 = 5 V; SEL1 = 0 V; $I_{OUTA}$ = 0 A; $I_{OUTB}$ = 12 A<br>– SideB: SEL0 = 0 V; SEL1 = 0 V; $I_{OUTA}$ = 12 A; $I_{OUTB}$ = 0 V | 0 | | 12 | µA |
| | | SEn = 5 V; PWM = 0 V; SideX diagnostic selected; HSx OFF<br>E.g.<br>– SideA: SEL0 = 5 V; SEL1 = 0 V; $IN_A$ = 0 V; $IN_B$ = 5 V; $I_{OUTB}$ = 12 A<br>– SideB: SEL0 = 0 V; SEL1 = 0 V; $IN_A$ = 5 V; $IN_B$ = 0 V; $I_{OUTA}$ = 12 A | 0 | | 10 | µA |
| $V_{SENSEH}$ | MultiSense output voltage in fault condition | $V_{CC}$ = 13 V; $R_{SENSE}$ = 1 kΩ;<br>– E.g: $Ch_0$ in open-load; $V_{IN}$ = 0 V; $I_{OUT}$ = 0 A; $V_{OUT}$ = 4 V | 5 | | 7 | V |
| $I_{SENSEH}$ | MultiSense current in fault condition | 9 V < $V_{CC}$ < 18 V; $V_{SENSE}$ = 5 V; MultiSense in fault condition | 10 | 20 | 30 | mA |
| **Chip temperature analog feedback** | | | | | | |
| $V_{SENSE\_TC}$ | MultiSense output voltage proportional to chip temperature | $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = -40 °C | 2.325 | 2.41 | 2.495 | V |
| | | $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = 25 °C | 1.985 | 2.07 | 2.155 | V |
| | | $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = 125 °C | 1.435 | 1.52 | 1.605 | V |
| $dV_{SENSE\_TC}/dT$ (2) | Temperature coefficient | $T_j$ = -40 °C to 150 °C | | -5.5 | | mV/K |
| Transfer function | | $V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC}/dT * (T - T_0)$ | | | | |
| **$V_{CC}$ supply voltage analog feedback** | | | | | | |

**Table 11. MultiSense (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE\_VCC}$ | MultiSense output voltage proportional to $V_{CC}$ supply voltage | $V_{CC}$ = 13 V; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | 3.16 | 3.23 | 3.3 | V |
| Transfer function | | $V_{SENSE\_VCC}$ = $V_{CC}$/4 | | | | |
| **MultiSense timings (Multiplexer transition times)(2)** | | | | | | |
| $t_{D\_CStoTC}$ | MultiSense transition delay from current sense to $T_C$ sense | $V_{INA}$ = 5 V; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 5 V to 0 V; $V_{SEL1}$ = 0 V to 5 V; $I_{OUTA}$ = 2.5 A; $R_{SENSE}$ = 1 kΩ; $V_{SENSE\_TC}$ = 90% of $V_{SENSE\_TC\_FINAL}$ | | | 60 | µs |
| $t_{D\_TCtoCS}$ | MultiSense transition delay from $T_C$ sense to current sense | $V_{INA}$ = 5 V; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 0 V to 5 V; $V_{SEL1}$ = 5 V to 0 V; $I_{OUTA}$ = 2.5 A; $R_{SENSE}$ = 1 kΩ; $I_{SENSE}$ = 90% of $I_{SENSE\_MAX}$ | | | 20 | µs |
| $t_{D\_CStoVCC}$ | MultiSense transition delay from current sense to $V_{CC}$ sense | $V_{INA}$ = 5 V; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 0 V to 5 V; $I_{OUTA}$ = 2.5 A; $R_{SENSE}$ = 1 kΩ; $V_{SENSE\_VCC}$ = 90% of $V_{SENSE\_VCC\_FINAL}$ | | | 60 | µs |
| $t_{D\_VCCtoCS}$ | MultiSense transition delay from $V_{CC}$ sense to current sense | $V_{INA}$ = 5 V; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V to 0 V; $I_{OUTA}$ = 2.5 A; $R_{SENSE}$ = 1 kΩ; $I_{SENSE}$ = 90% of $I_{SENSE\_MAX}$ | | | 20 | µs |
| $t_{D\_TCtoVCC}$ | MultiSense transition delay from $T_C$ sense to $V_{CC}$ sense | $V_{CC}$ = 13 V; $T_j$ = 125 °C; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 0 V to 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $V_{SENSE\_VCC}$ = 90% of $V_{SENSE\_VCC\_FINAL}$ | | | 20 | µs |
| $t_{D\_VCCtoTC}$ | MultiSense transition delay from $V_{CC}$ sense to $T_C$ sense | $V_{CC}$ = 13 V; $T_j$ = 125 °C; $V_{SENSE\_EN}$ = 5 V; $V_{SEL0}$ = 5 V to 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $V_{SENSE\_TC}$ = 90% of $V_{SENSE\_TC\_FINAL}$ | | | 20 | µs |
| **MultiSense timings (CurrentSense mode)** | | | | | | |
| $t_{DSENSE1H}$ | Current sense settling time from rising edge of $V_{SENSE\_EN}$ | $V_{INA}$ = 5 V; $V_{INB}$ = 0 V; $V_{SENSE\_EN}$ = 0 V to 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 2.6 Ω; $V_{PWM}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 0 V | | | 60 | µs |

**Table 11. MultiSense (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{DSENSE1L}$ | Current sense disable delay time from falling edge of $V_{SENSE\_EN}$ | $V_{INA}$ = 5 V; $V_{INB}$ = 0 V; $V_{SENSE\_EN}$ = 5 V to 0 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 2.6 Ω; $V_{PWM}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 0 V | | | 20 | µs |
| $t_{DSENSE2H}$ | $V_{SENSE\_TC}$ settling time from rising edge of $V_{SENSE\_EN}$ | $V_{SENSE\_EN}$ = 0 V to 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{DSENSE2L}$ | $V_{SENSE\_TC}$ settling time from rising edge of $V_{SENSE\_EN}$ | $V_{SENSE\_EN}$ = 5 V to 0 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| **MultiSense timings ($V_{CC}$ voltage sensor mode)** | | | | | | |
| $t_{DSENSE3H}$ | $V_{SENSE\_VCC}$ settling time from rising edge of $V_{SENSE\_EN}$ | $V_{SENSE\_EN}$ = 0 V to 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{DSENSE3L}$ | $V_{SENSE\_VCC}$ settling time from rising edge of $V_{SENSE\_EN}$ | $V_{SENSE\_EN}$ = 5 V to 0 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |

1. Analog sense current drift is deviation of factor K for a given device over (-40°C to 150°C and 9 V < $V_{CC}$ < 18 V) with respect to its value measured at $T_j$ = 25 °C, $V_{CC}$ = 13 V.
2. Parameter guaranteed by design and characterization; not subject to production test.

**Figure 4. $T_{DSTKON}$**

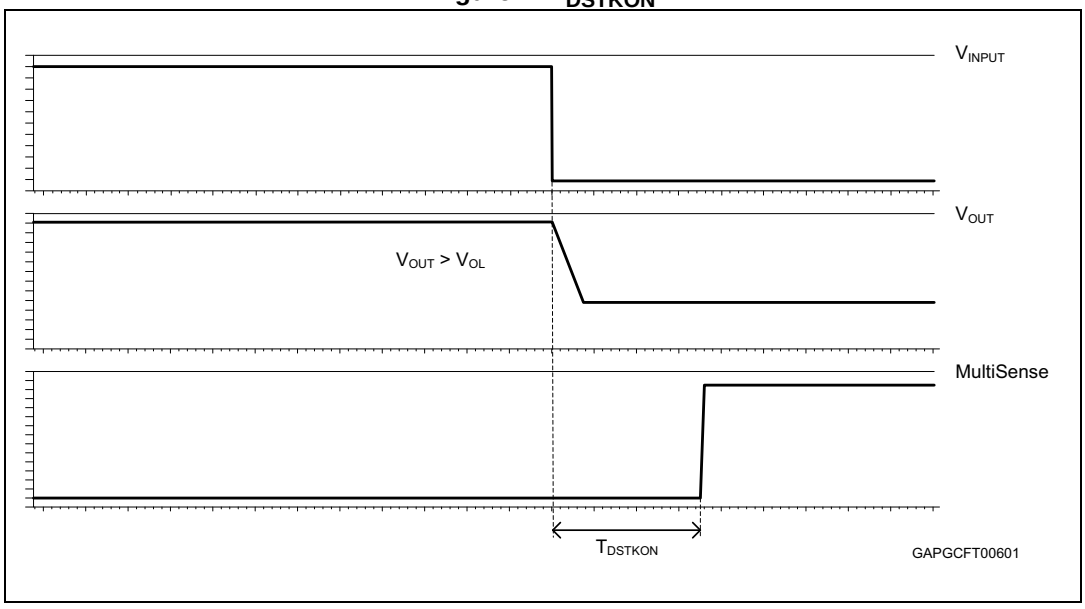


**Figure 5. Definition of the low-side switching times**

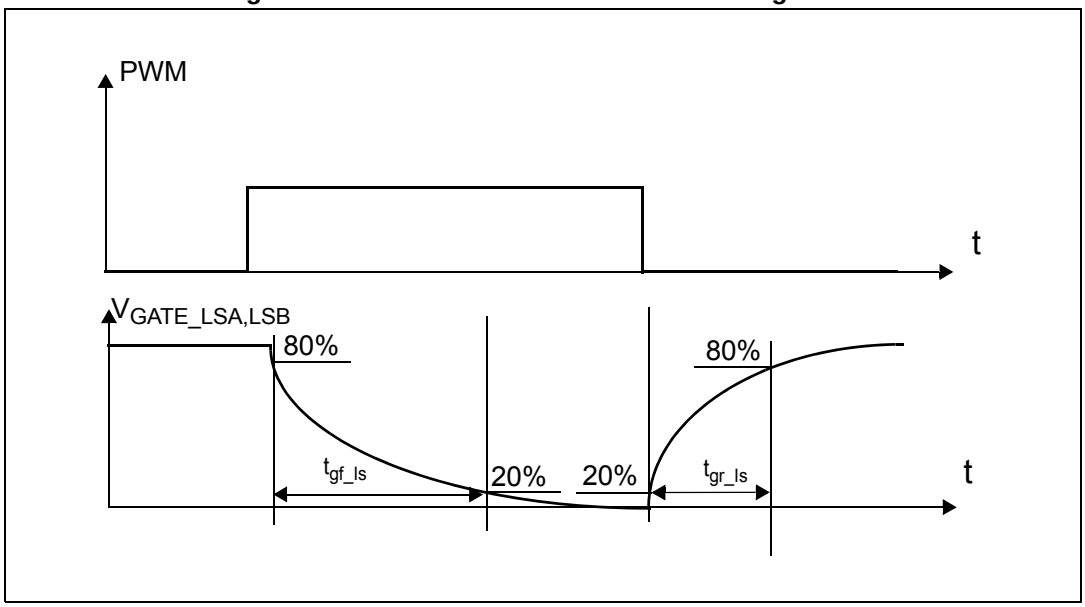



**Figure 6. Definition of the high-side switching times**

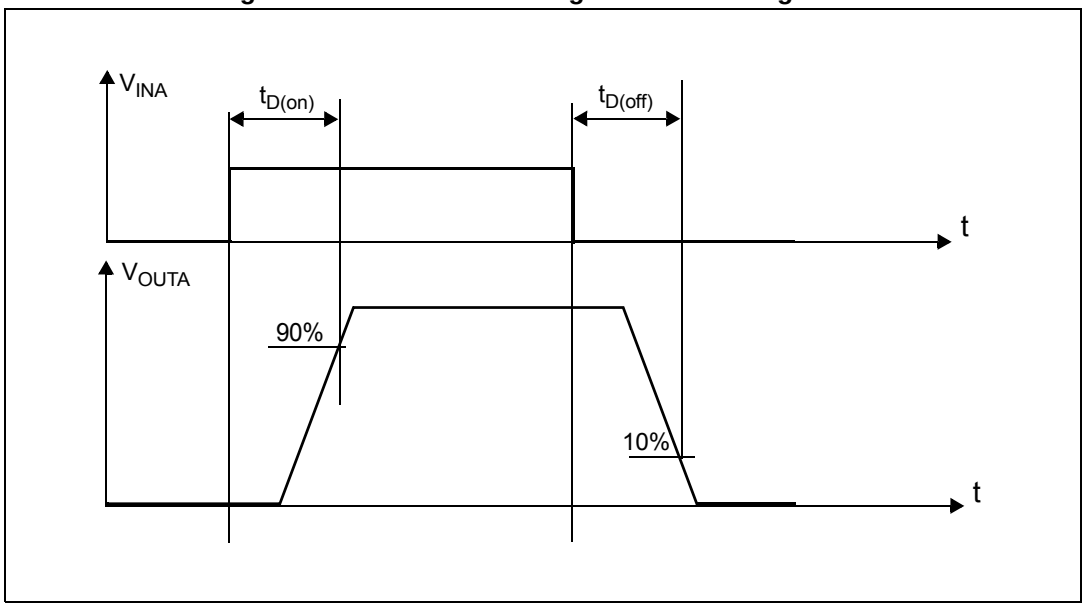


**Figure 7. Low-side turn-on delay time**

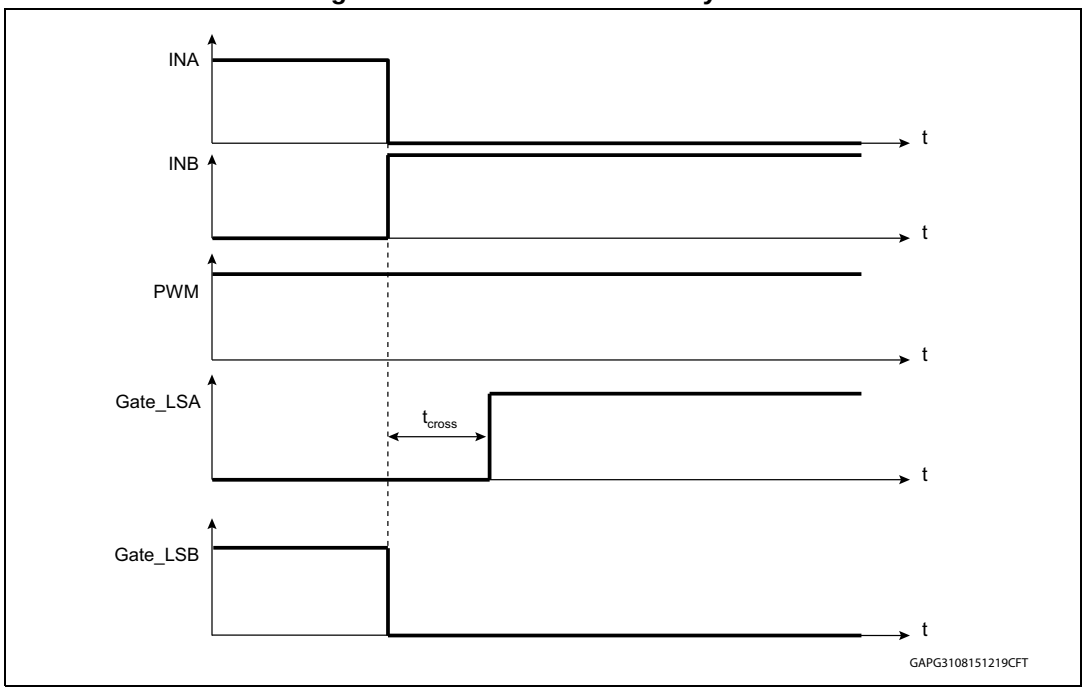
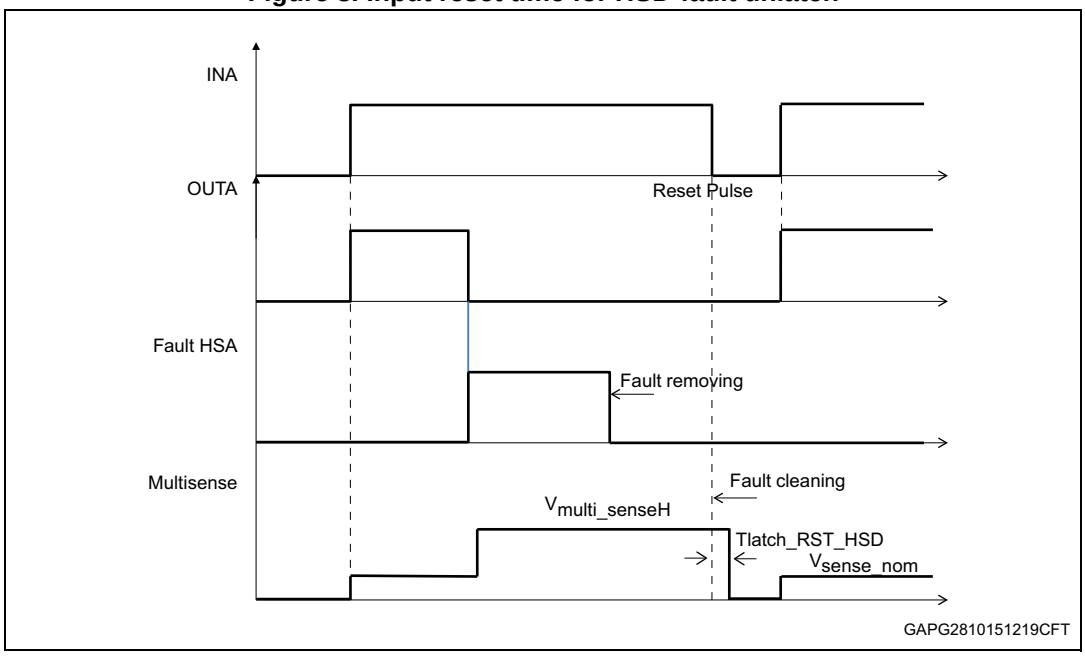
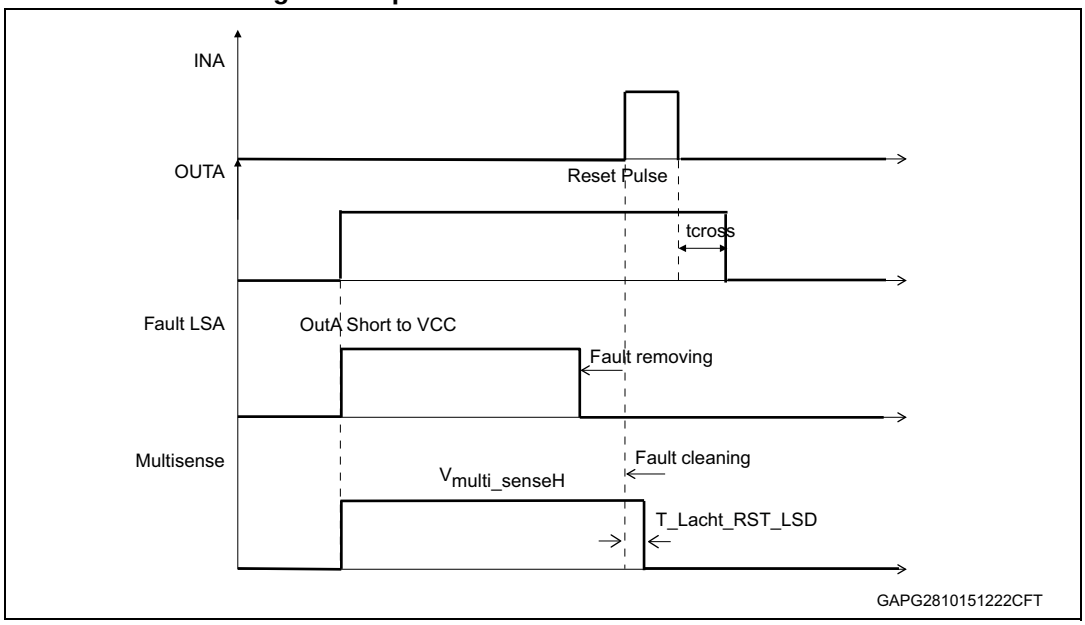



**Figure 8. Input reset time for HSD-fault unlatch**



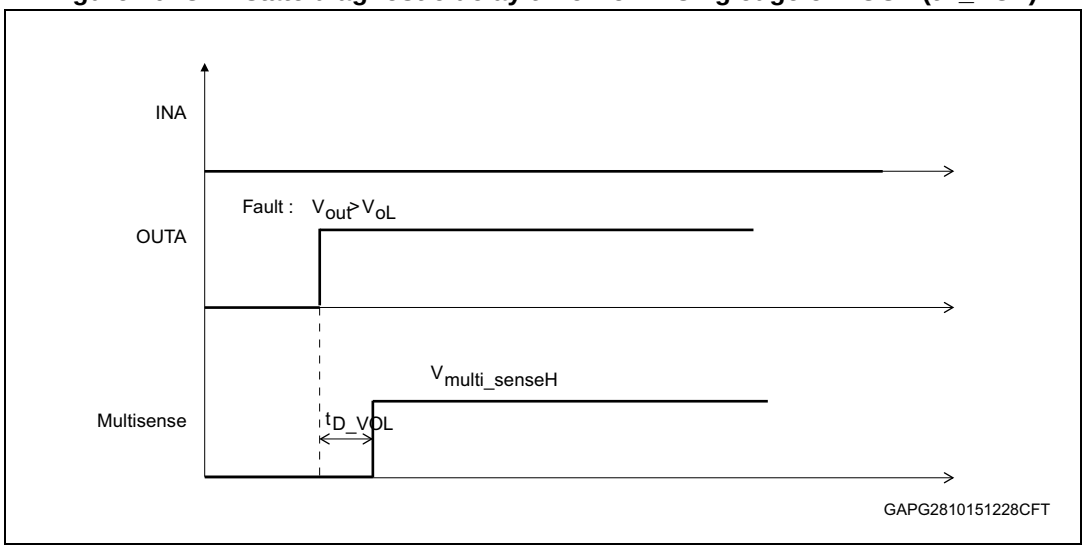

*Note: Multisense_EN=1*

**Figure 9. Input reset time for LSD-fault unlatch**




*Note: Multisense_EN=1*

**Figure 10. OFF-state diagnostic delay time from rising edge of VOUT (tD_VOL)**




*Note: Multisense_EN=1*

**Table 12. Operative condition - truth table**

| INA | INB | PWM | SEL0 | SEL1 | MultiSense_EN | MultiSense | HSA | LSA | HSB | LSB |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | High-Z | OFF | ON | OFF | ON |
| | | 1 | 1 | 0 | 1 | High-Z | OFF | ON | OFF | ON |
| 0 | 1 | 0 | 0 | 0 | 1 | Current Monitoring HSB | OFF | OFF | ON | OFF |
| | | 1 | 0 | 0 | 1 | Current Monitoring HSB | OFF | ON | ON | OFF |
| 0 | 1 | 0 | 1 | 0 | 1 | High-Z | OFF | OFF | ON | OFF |
| | | 1 | 1 | 0 | 1 | High-Z | OFF | ON | ON | OFF |
| 1 | 0 | 0 | 0 | 0 | 1 | High-Z | ON | OFF | OFF | OFF |
| | | 1 | 0 | 0 | 1 | High-Z | ON | OFF | OFF | ON |
| 1 | 0 | 0 | 1 | 0 | 1 | Current Monitoring HSA | ON | OFF | OFF | OFF |
| | | 1 | 1 | 0 | 1 | Current Monitoring HSA | ON | OFF | OFF | ON |
| 1 | 1 | X(1) | 0 | 0 | 1 | Current Monitoring HSB | ON | OFF | ON | OFF |
| | | | 1 | 0 | 1 | Current Monitoring HSA | ON | OFF | ON | OFF |
| 0 | 0 | 0 | 1 | 0 | 1 | Off-state diagnostic OUTA | OFF | OFF | OFF | OFF |
| 0 | 0 | 0 | 0 | 0 | 1 | Off-state diagnostic OUTB | OFF | OFF | OFF | OFF |
| X | X | X | 0 | 1 | 1 | $T_{CHIP}$ Monitoring | — | — | — | — |
| X | X | X | 1 | 1 | 1 | $V_{CC}$ Monitoring | — | — | — | — |
| X | X | X | X | X | 0 | High-Z(2) | — | — | — | — |

1. X: the level of the pin can be 0 or 1.
2. When $IN_A$ = $IN_B$ = PWM = SEL0 = SEL1 = MultiSense_EN = 0 device enters standby after $T_{DSTBY}$.

**Table 13. On-state fault conditions- truth table**

| Digital input pins(1) | | | | MultiSense | Comment |
|---|---|---|---|---|---|
| INA | INB | PWM | SEL0 | | |
| 0 | 0 | 1 | 0 | $V_{SENSE\_H}$ | VDS LSB protection triggered; LSB latched off |
| 0 | 0 | 1 | 1 | $V_{SENSE\_H}$ | VDS LSA protection triggered; LSA latched off |
| 0 | 1 | X | 0 | $V_{SENSE\_H}$ | HSB protection triggered; HSB latched off |
| 0 | 1 | 1 | 1 | $V_{SENSE\_H}$ | VDS LSA protection triggered; LSA latched off |
| 1 | 0 | 1 | 0 | $V_{SENSE\_H}$ | VDS LSB protection triggered; LSB latched off |
| 1 | 0 | X | 1 | $V_{SENSE\_H}$ | HSA protection triggered; HSA latched off |
| 1 | 1 | X | 0 | $V_{SENSE\_H}$ | HSB protection triggered; HSB latched off |
| 1 | 1 | X | 1 | $V_{SENSE\_H}$ | HSA protection triggered; HSA latched off |

1. MultiSense_EN = 1 and SEL1 = 0 are mandatory for fault detection. Other logic combinations on digital input pins not reported on the above table do not allow to detect a latched-off channel.

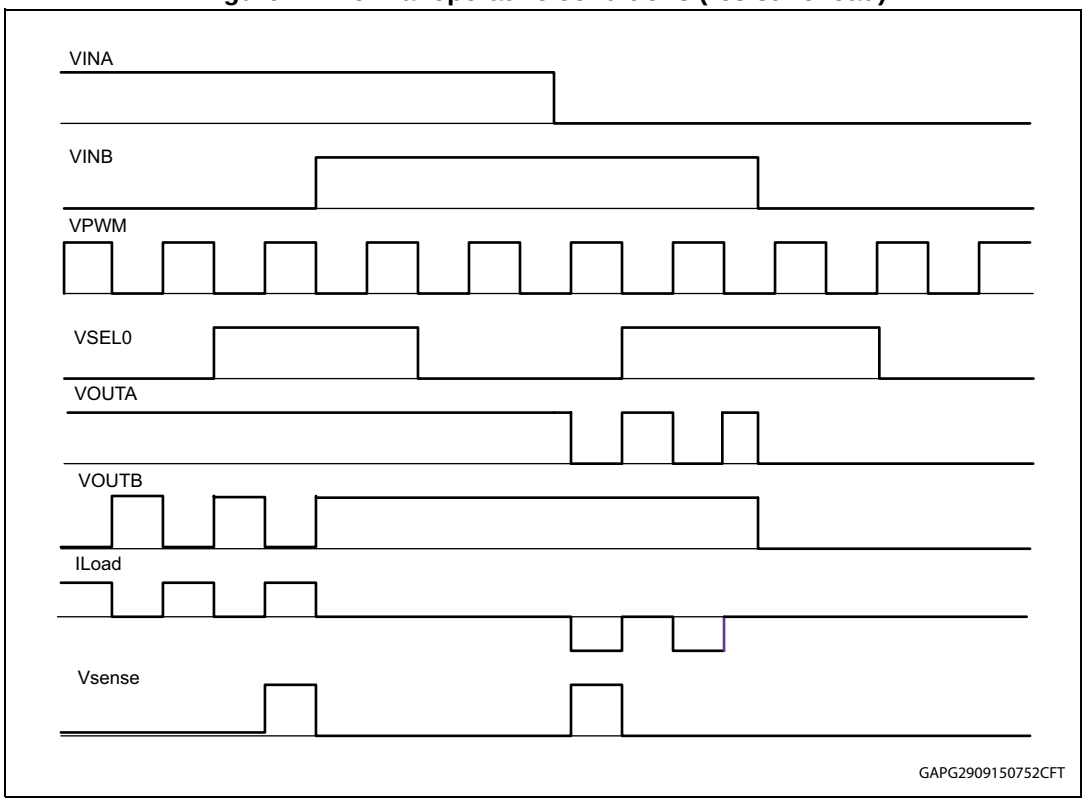
**Table 14. Off-state — truth table**

| INA | INB | SEL0 | SEL1 | PWM | OUTA | OUTB | MultiSense_EN | MultiSense | Description |
|---|---|---|---|---|---|---|---|---|---|
| **Off-state diagnostic** | | | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | $V_{OUTA} > V_{OL}$ | X | 1 | $V_{SENSEH}$ | **Case 1: $OUT_A$ shorted to $V_{CC}$** if no pull-up is applied.<br>**Case 2: NO open-load** in full bridge configuration with an external pull-up on OUTB<br>**Case 3: open-load** in half bridge configuration with an external pull-up on $OUT_A$ (motor connected between Out and Ground) |
| | | | | | $V_{OUTA} < V_{OL}$ | X | 1 | Hi-Z | **Case 1: open-load** in full Bridge configuration with an external pull-up on $OUT_B$<br>**Case 2: NO open-load** in half Bridge configuration with external pull-up on $OUT_A$ (motor connected between Out and Ground) |
| | | 0 | 0 | | X | $V_{OUTB} > V_{OL}$ | 1 | $V_{SENSEH}$ | **Case 1: $OUT_B$ shorted to $V_{CC}$** if no pull-up is applied<br>**Case 2: NO open-load** in full bridge configuration with external pull-up on $OUT_A$<br>**Case 3: open-load** in half bridge configuration with external pull-up on $OUT_B$ (motor connected between Out and Ground) |
| | | | | | X | $V_{OUTB} < V_{OL}$ | 1 | Hi-Z | **Case1: open-load** in full Bridge configuration with an external pull-up on $OUT_A$<br>**Case 2. NO open-load** in half Bridge configuration with external pull-up on $OUT_B$ (motor connected between Out and Ground) |

*Note: To power on the device from standby, it is recommended to: toggle INA or INB or SEL0 or SEL1 from 0 to 1 first to come out from STBY mode; toggle PWM from 0 to 1 with a delay of 20 microsecond this avoids any overstress on the device in case of existing short-to-battery.*

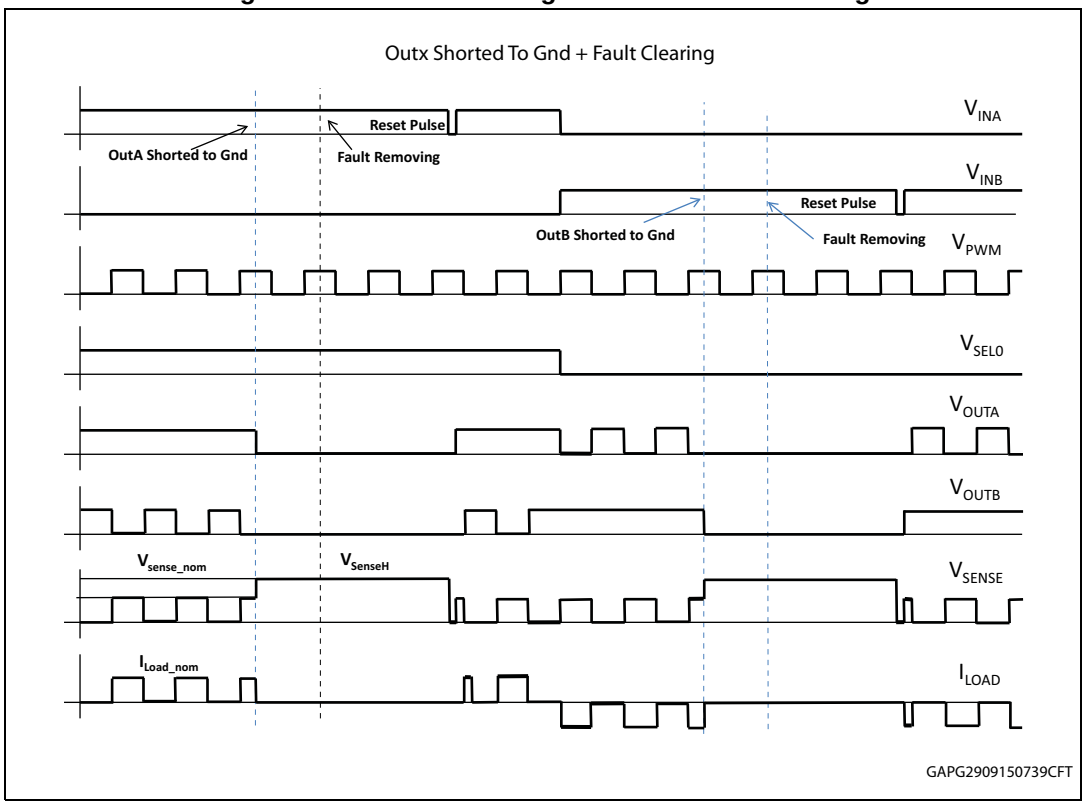
## 2.4 Waveforms

**Figure 11. Normal operative conditions (resistive load)**



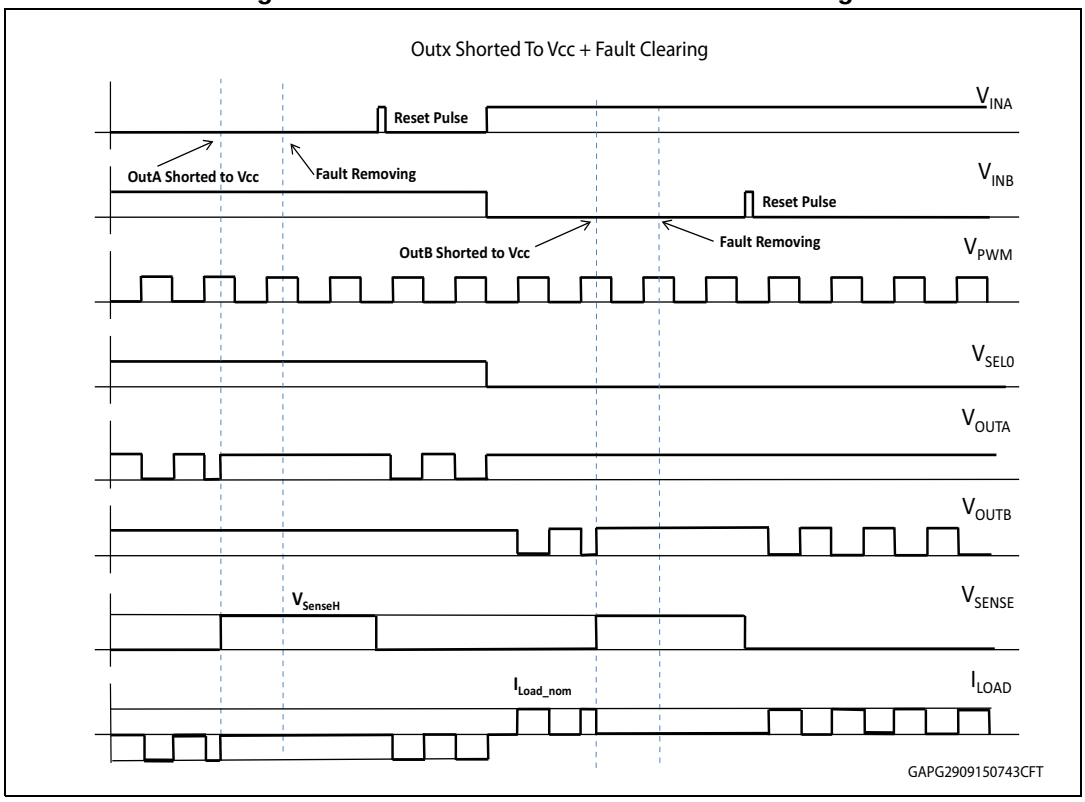

*Note: MultiSense_EN=1*

**Figure 12. Out shorted to ground and short clearing**




*Note: MultiSense_EN=1*

**Figure 13. OUT shorted to Vcc and short clearing**




*Note: MultiSense_EN=1*

**Figure 14. Gate driver low side rise time normalized vs $C_g$ = 4.7nF**

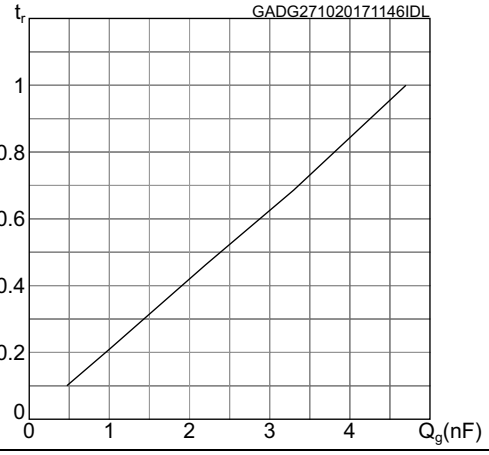
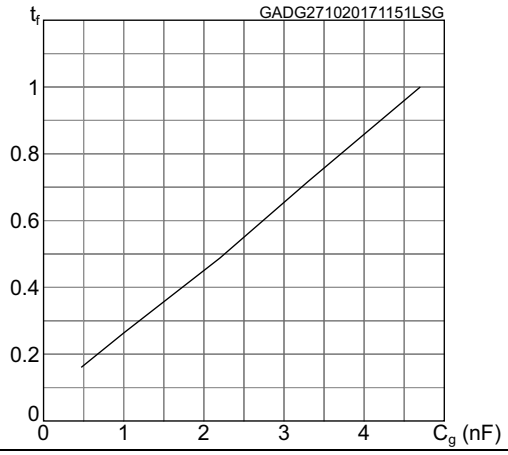



**Figure 15. Gate driver low side fall time normalized vs $C_g$ = 4.7nF**



# 3 Protections

## 3.1 Power limitation (high-side driver)

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing $\Delta$ Tj through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as $\Delta$ Tj exceeds the safety level of $\Delta$ Tj_SD. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue. When Power Limitation is reached, The device enters in latch mode and generates the Fault Flag on Multisense = VsenseH when the faulty leg diagnostic is selected (please refer to *Table 13*).

## 3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), the device enters in latch mode and generates the Fault Flag on Multisense = VsenseH (please refer to *Table 13*). The concerned high side can be switched ON again as soon as: $T_j$ drops below TTR_HSD, INX is set low for a duration > TLATCH_RST_HS and set high again.

## 3.3 High-side current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. In case of short circuit, overload or during load power-up, the output current is clamped to a safety level, ILIMH, by operating the output power MOSFET in the active region

## 3.4 External PowerMOS low side VDS monitoring

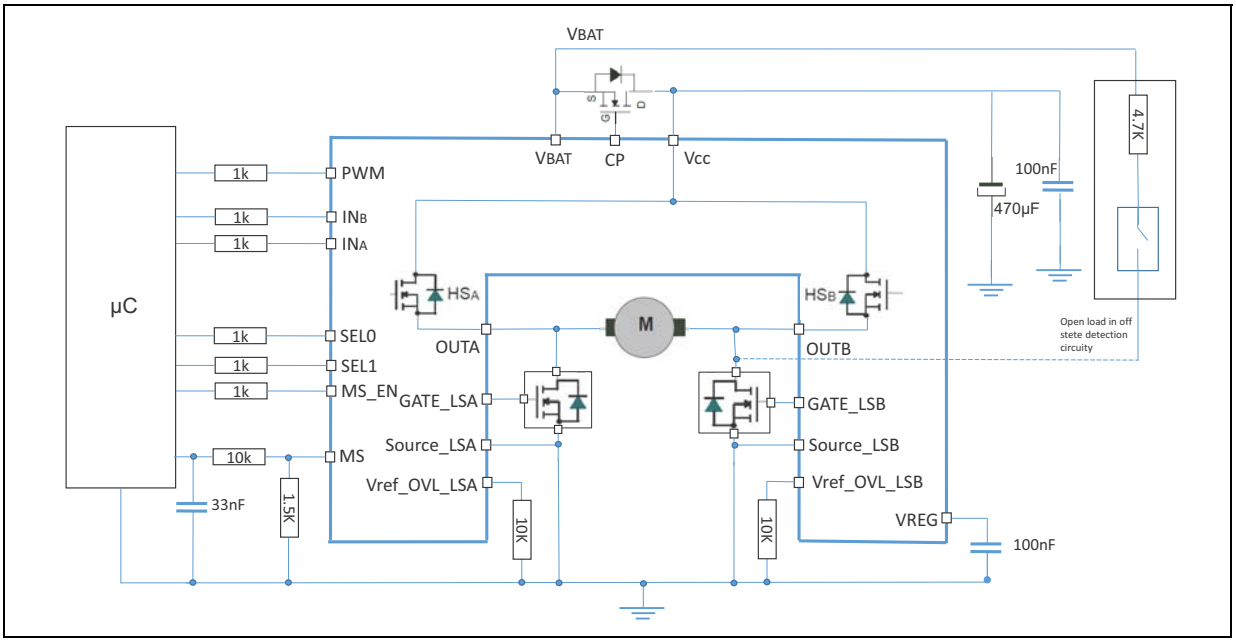
The VDS_monitoring function has the ability to sense the OUTPUT Mosfet source voltage and compare it to a predetermined threshold. This threshold is programmable, using an internal reference current IREF_OVL_LSD = 50 µA (typ.) and an external resistor connected at VREF_OVL_LS external pin.

This protection will be activated when the low side Power Mos is switched ON and its gate is fully charged: to guarantee this condition the function will detect a short to battery event only when PWM = H and after a blanking time tfil_OVL_LS= 2.2 µs (typ.) starting from PWM rising edge. This feature is present for each LSD leg.

In case of fault conditions caused by Power Limitation or overtemperature or open load/short to VCC in OFF state, the fault is indicated by the MultiSense pin being internally switched to a "current limited" voltage source pulled to level $V_{SENSEH}$.

# 4 Typical application schematic

**Figure 16. Typical application schematic**




*Note: To protect the device against Battery disconnection with energized inductive load when the bridge driver goes into 3-state, suggested C(Vcc) is:*

$$c(V_{cc}) = \frac{Emotor}{0.5DVcc,max^2}$$

*where:*

*Emotor = 33.5 mJ;*

*DVcc,max = Vcc_AMR - Vcc_max;*

*Vcc_AMR = 38 V;*

*Vcc_max = 26 V (Vcc at jump start);*

*C(Vcc) = 470 µF*

# 5 MultiSense operation

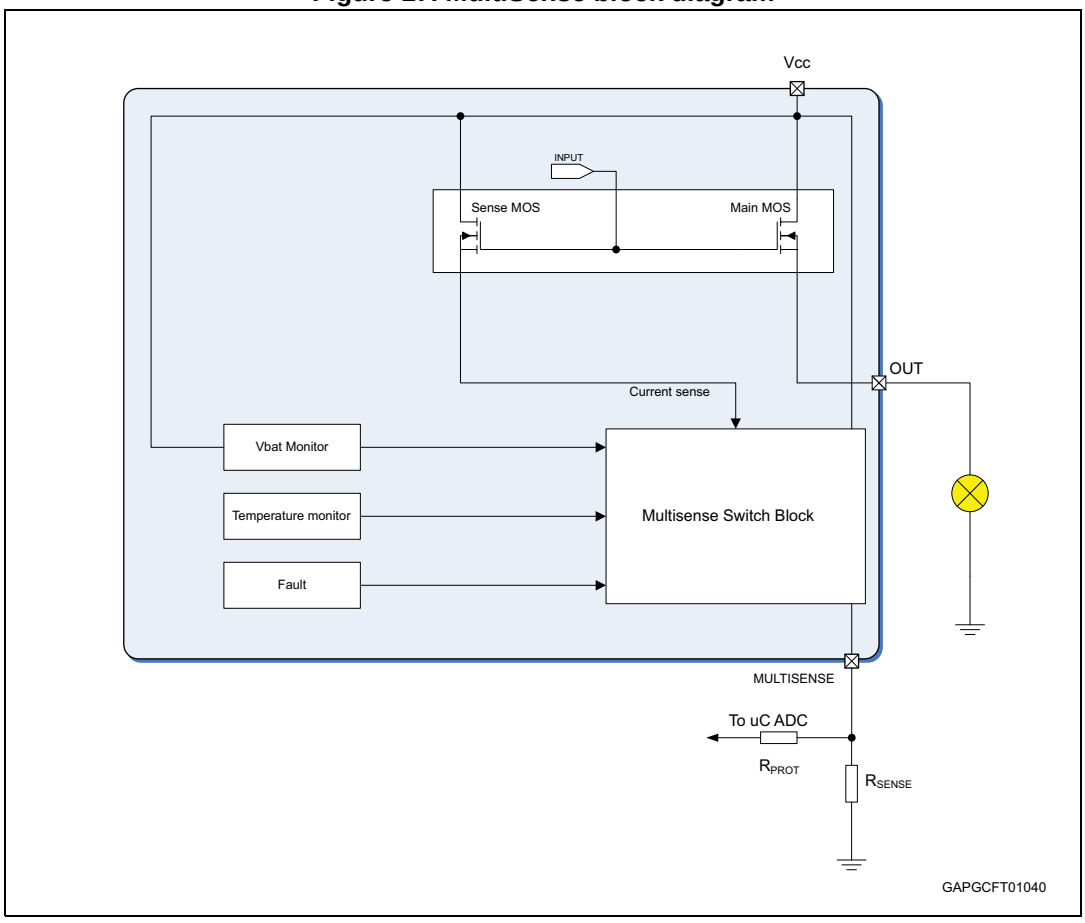
## 5.1 MultiSense analog monitoring

Diagnostic information on device and load status are provided by an analog output pin (MultiSense) delivering the following signals:

- Current monitor: current mirror of HSDx output current
- VCC monitor: voltage propotional to VCC
- TCASE: voltage propotional to chip temperature

Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *Table 12*.

**Figure 17. MultiSense block diagram**




## 5.2 Multisense diagnostics flag in fault conditions

Multisense pin delivers fixed voltage (VSENSEH) with a certain current capability in case of:

- fault condition on activated high-side triggered by Power Limitation
- fault condition on activated high-side triggered by overtemperature protection
- fault condition on VDS of Low side exceeded threshold

# 6 VREG and Driver_LS Block

VREG pin is the output of an internal low drop voltage regulator. VREG block is designed to power the driver of external power Mosfet (Driver_LS) and it allows a proper MOS transition.

- VREG out voltage will be VREG=10V if Vbattery > 10V, while VREG = Vbattery if Vbattery < 10V.

An external capacitor $C_{REG}$ = 100 nF connected to the pin VREG is needed to proper polarize the circuit (see *Figure 16*).

# 7 Reverse battery protection

CP pin provides the necessary gate drive for an external n-channel PowerMOS used for reverse polarity protection. The external N-channel Power MOSFET used for the reverse battery protection should have the following characteristics:

- BVdss > 20 V (for a reverse battery of -16 V);
- RDS(on) < 1/3 of H-bridge total RDS(on)
- Standard Logic Gate Driving

# 8 Open-load detection in off-state

The Open Load (OL) detection in off-state operates when output is deactivated (means INA = INB = PWM=0, or INB together with PWM=0). Open load detection is performed by reading the MultiSense output. External (switched) pull-up resistor has to be used and dimensioned to pull output voltage above the maximum open load detection voltage (VOL MAX) when load is not connected and as well stays below the minimum level (VOL MIN) when load is connected.

When the open load is detected, VsenseH is indicated on Multisense pin, possible conditions are specified in *Table 14*.

If pull up resistor is applied over switched circuitry, it allows to detect short to VCC from open-load (see *Figure 16*).

The RPU value has to be:

$$R_{pull\_up} < \frac{V_{BATTmin} - V_{OLmax}}{2 \times I_{L(off2)min\ [@VOLmax]}}$$

# 9 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the VCC pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 15*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through VCC and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

**Table 15. IISO 7637-2 - electrical transient conduction along supply line**

| Test pulse 2011(E) | Test pulse severity level with status II functional performance status | | Minimum number of pulses or test time | Burst cycle/pulse repetition time | | Pulse duration and pulse generator internal impedance |
|---|---|---|---|---|---|---|
| | Level | $U_S$(1) | | min. | max. | |
| 1 | III | -112 V | 500 pulses | 0.5 s | | 2 ms, 10 Ω |
| 2a | III | +55 | 500 pulses | 0.2 s | 5 s | 50 µs, 2 Ω |
| 3a | IV | -220 V | 1h | 90 ms | 100 ms | 0.1 µs, 50 Ω |
| 3b | IV | +150 V | 1h | 90 ms | 100 ms | 0.1 µs, 50 Ω |
| 4(2) | IV | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| **Load dump according to ISO 16750-2:2010** | | | | | | |
| Test B(3) | | 40 V | 5 pulse | 1 min | | 400 ms, 2 Ω |

1. US is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E)
2. Test pulse from ISO 7637-2:2004(E)
3. With 40 V external suppressor referred to ground (-40 °C < $T_J$ < 150 °C)

# 10 Package and PCB thermal data

## 10.1 PowerSSO-36 thermal data

**Figure 18. PowerSSO-36 PCB board**

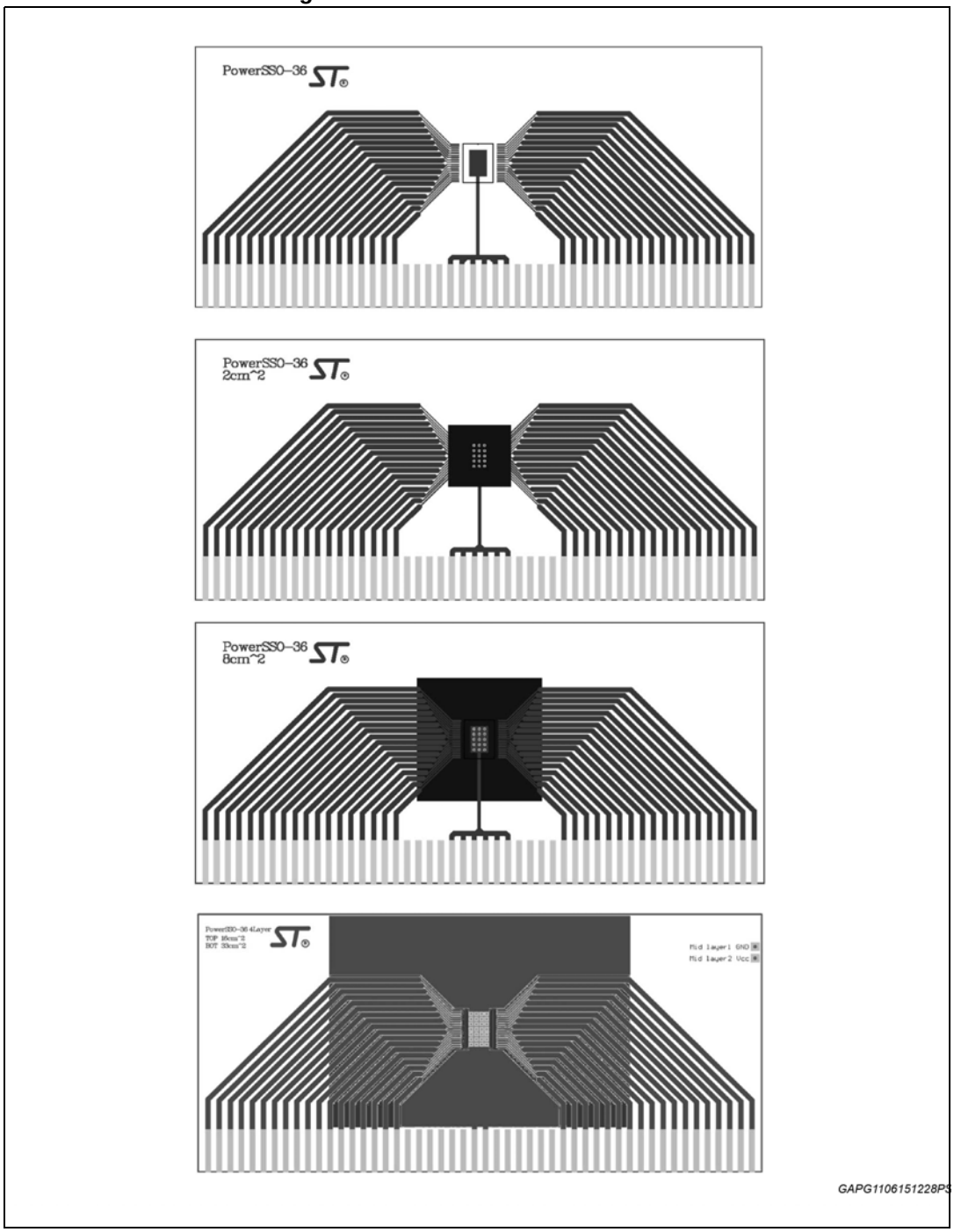
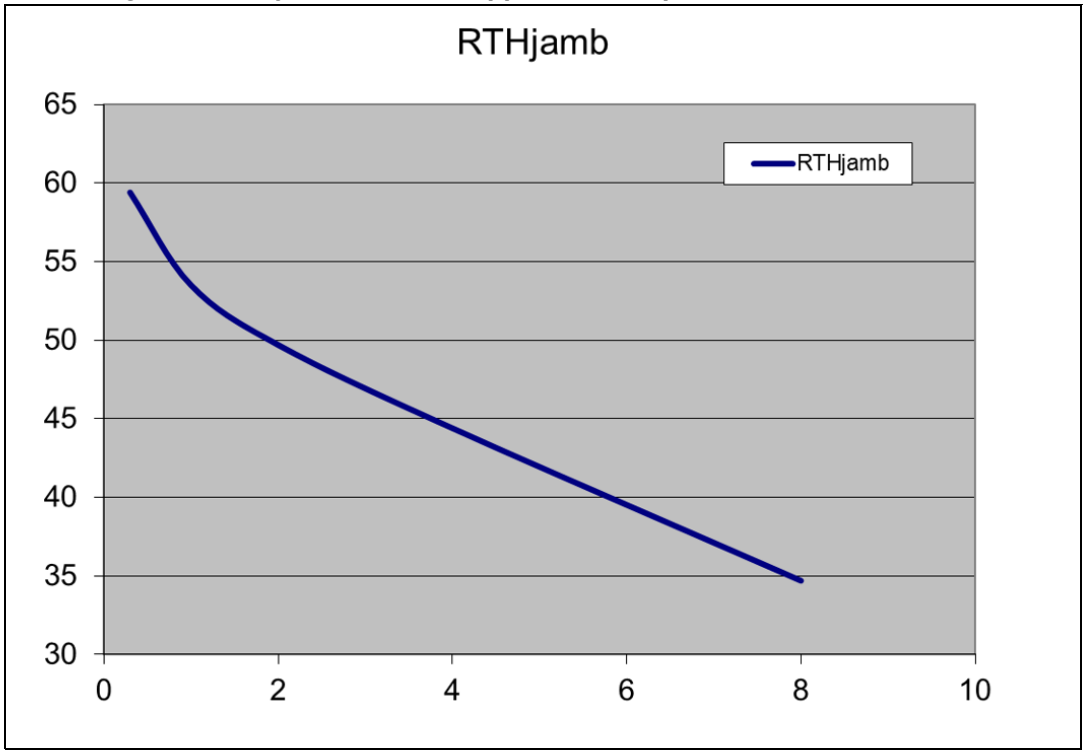


**Table 16. PCB properties**

| Dimension | Value |
|---|---|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 129 mm x 86 mm |
| Board material | FR4 |
| Cu thickness (outer layers) | 0.070 mm |
| Cu thickness (inner layers) | 0.035 mm |
| Thermal via separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Cu thickness on vias | 0.025 mm |
| Footprint dimension | 4.1 mm x 6.5 mm |

**Figure 19. Rthj-amb vs PCB copper area in open box free air condition**

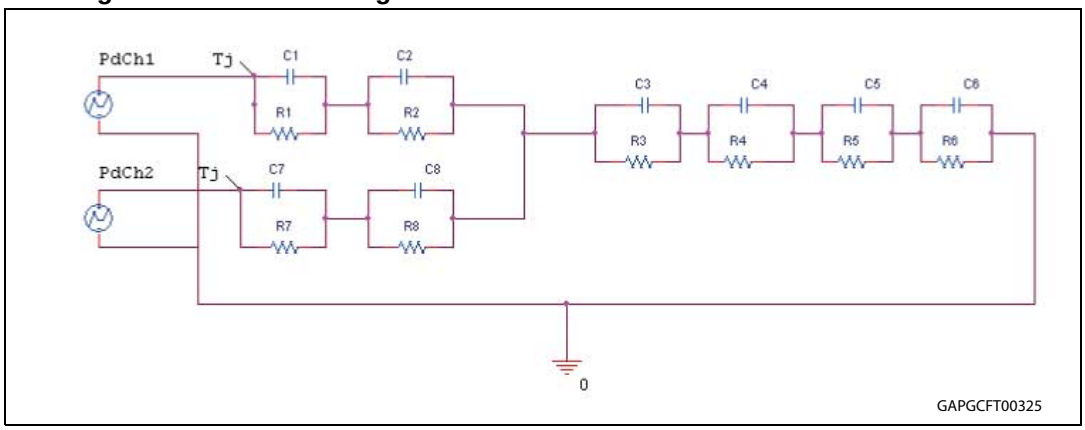



**Equation 1: pulse calculation formula**

$ZTH\delta = RTH \cdot \delta + ZTHtp (1 - \delta)$

where $\delta = tP/T$

**Figure 20. Thermal fitting model of a double-channel HSD in PowerSSO-36**




*Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.*

**Figure 21. Thermal impedance junction ambient single pulse**

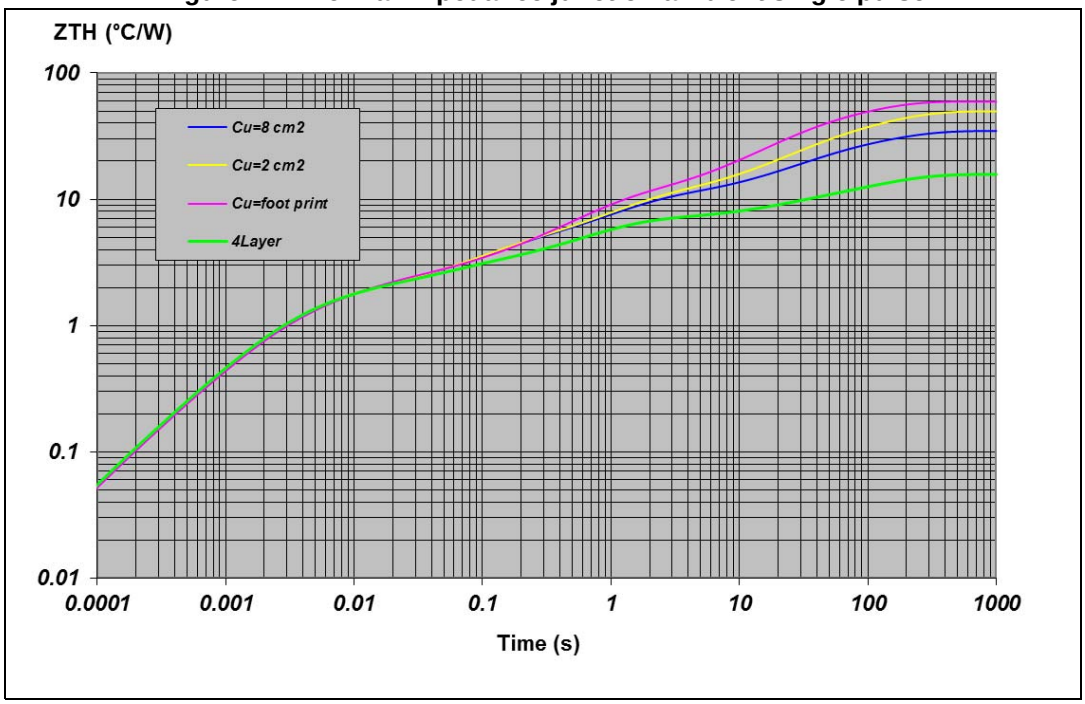



**Table 17. Thermal parameters**

| Area / island | FP | 2 | 8 | 4L |
|---|---|---|---|---|
| R1 (°C/W) | 0.75 | | | |
| R2 (°C/W) | 1 | | | |
| R3 (°C/W) | 2 | 2 | 2 | 1 |
| R4 (°C/W) | 7 | 6 | 6 | 4 |
| R5 (°C/W) | 20 | 14 | 10 | 2 |

Table 17. Thermal parameters (continued)

| Area / island | FP | 2 | 8 | 4L |
|---|---|---|---|---|
| R6 (°C/W) | 30 | 26 | 15 | 7 |
| R7 (°C/W) | 0.75 | | | |
| R8 (°C/W) | 1 | | | |
| C1 (W•s/°C) | 0.0027 | | | |
| C2 (W•s/°C) | 0.006 | | | |
| C3 (W•s/°C) | 0.05 | 0.05 | 0.05 | 0.05 |
| C4 (W•s/°C) | 0.15 | 0.2 | 0.2 | 0.2 |
| C5 (W•s/°C) | 1 | 2 | 3 | 10 |
| C6 (W•s/°C) | 3 | 5 | 9 | 18 |
| C7 (W•s/°C) | 0.0027 | | | |
| C8 (W•s/°C) | 0.006 | | | |

# 11 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

## 11.1 PowerSSO-36 package information

**Figure 22. PowerSSO-36 package dimensions**

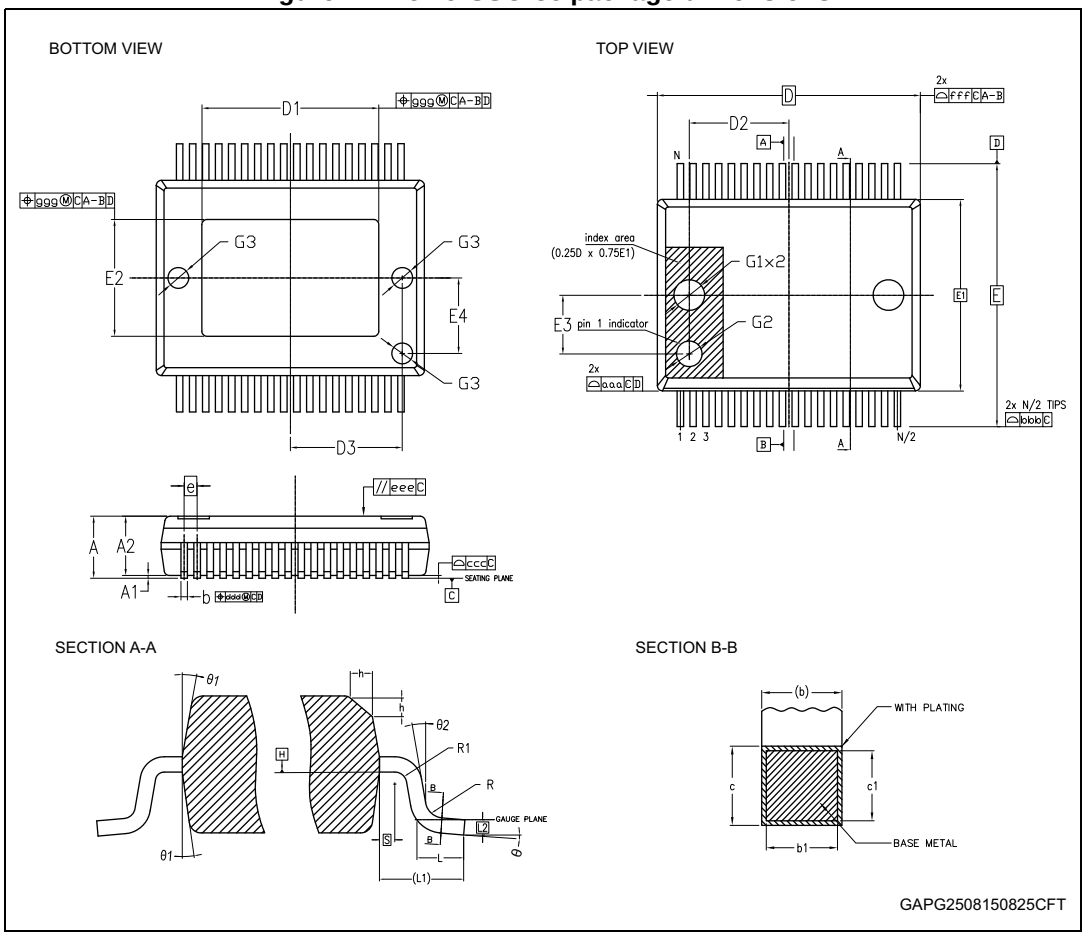



**Table 18. PowerSSO-36 (exposed pad) package mechanical data**

| Ref | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| Θ | 0° | - | 8° |
| Θ1 | 5° | - | 10° |
| Θ2 | 0° | - | - |

Table 18. PowerSSO-36 (exposed pad) package mechanical data (continued)

| Ref | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.15 | - | 2.45 |
| A1 | 0.0 | - | 0.1 |
| A2 | 2.15 | - | 2.35 |
| b | 0.18 | - | 0.32 |
| b1 | 0.13 | 0.25 | 0.3 |
| c | 0.23 | - | 0.32 |
| c1 | 0.2 | 0.2 | 0.3 |
| D(1) | 10.30 BSC | | |
| D1 | 6.9 | - | 7.5 |
| D2 | - | 3.65 | - |
| D3 | - | 4.3 | - |
| e | 0.50 BSC | | |
| E | 10.30 BSC | | |
| E1(1) | 7.50 BSC | | |
| E2 | 4.3 | - | 5.2 |
| E3 | - | 2.3 | - |
| E4 | - | 2.9 | - |
| G1 | - | 1.2 | - |
| G2 | - | 1 | - |
| G3 | - | 0.8 | - |
| h | 0.3 | - | 0.4 |
| L | 0.55 | 0.7 | 0.85 |
| L1 | 1.40 REF | | |
| L2 | 0.25 BSC | | |
| N | 36 | | |
| R | 0.3 | - | - |
| R1 | 0.2 | - | - |
| S | 0.25 | - | - |
| **Tolerance of form and position** | | | |
| aaa | 0.2 | | |
| bbb | 0.2 | | |
| ccc | 0.1 | | |
| ddd | 0.2 | | |

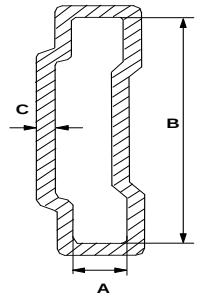
Table 18. PowerSSO-36 (exposed pad) package mechanical data (continued)

| Ref | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| eee | | 0.1 | |
| ffff | | 0.2 | |
| ggg | | 0.15 | |

1. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is ‘0.25 mm’ per side D and ‘0.15 mm’ per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

## 11.2 PowerSSO-36 packing information

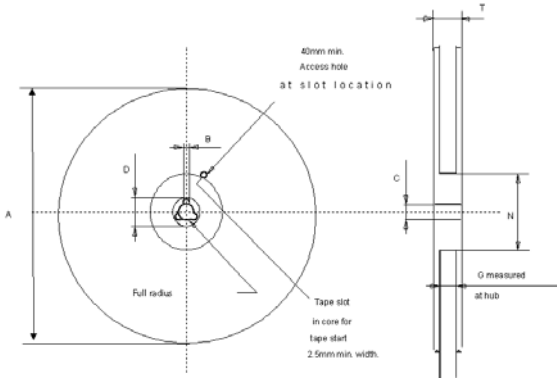
Figure 23. PowerSSO-36 tube shipment (no suffix)




| | |
|---|---|
| **Base Qty** | 49 |
| **Bulk Qty** | 1225 |
| **Tube length (±0.5)** | 532 |
| **A** | 3.5 |
| **B** | 13.8 |
| **C (±0.1)** | 0.6 |

All dimensions are in mm.

**Figure 24. PowerSSO-36 tape and reel shipment (suffix “TR”)**



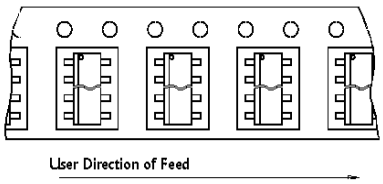

**Reel dimensions**

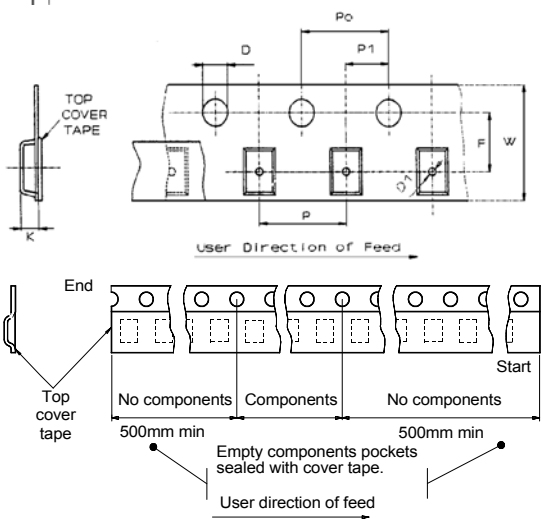
| | |
|---|---|
| **Base Qty** | 1000 |
| **Bulk Qty** | 1000 |
| **A (max)** | 330 |
| **B (min)** | 1.5 |
| **C (±0.2)** | 13 |
| **F** | 20.2 |
| **G (+2 / -0)** | 24.4 |
| **N (min)** | 100 |
| **T (max)** | 30.4 |

**Tape dimensions**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

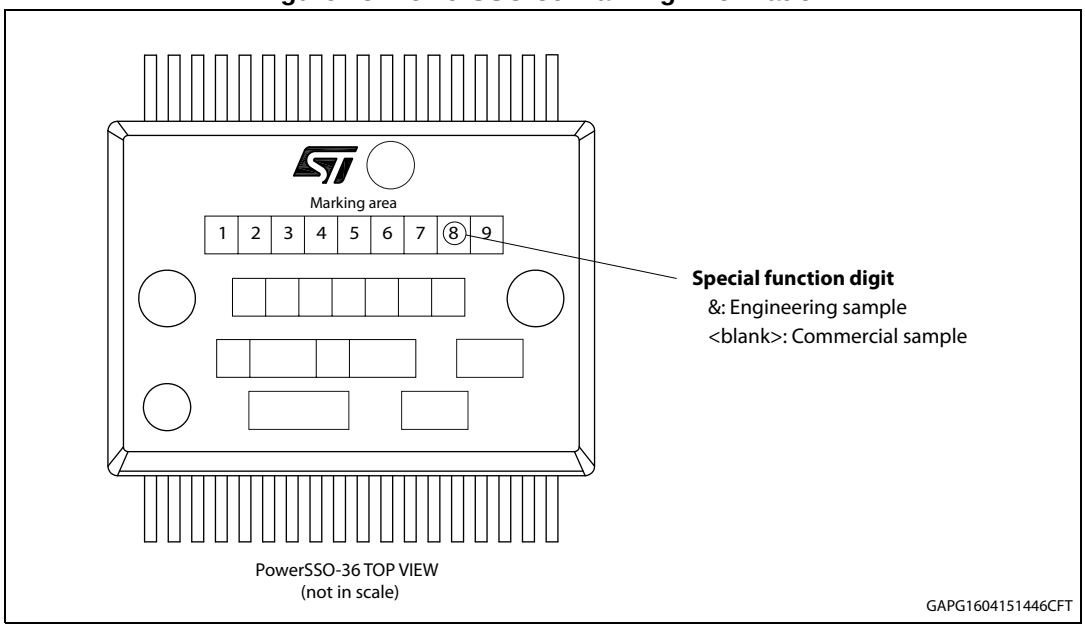
| | | |
|---|---|---|
| **Tape width** | **W** | 24 |
| **Tape Hole Spacing** | **P0 (±0.1)** | 4 |
| **Component Spacing** | **P** | 12 |
| **Hole Diameter** | **D (±0.05)** | 1.55 |
| **Hole Diameter** | **D1 (min)** | 1.5 |
| **Hole Position** | **F (±0.1)** | 11.5 |
| **Compartment Depth** | **K (max)** | 2.85 |
| **Hole Spacing** | **P1 (±0.1)** | 2 |



## 11.3 PowerSSO-36 marking information

**Figure 25. PowerSSO-36 marking information**




*Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

*Note: Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.*

# 12 Order codes

**Table 19. Device summary**

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| PowerSSO-36 | VNHD7008AY | VNHD7008AYTR |

# 13 Revision history

**Table 20. Document revision history**

| Date | Revision | Description of changes |
|---|---|---|
| 11-Feb-2016 | 1 | Initial release. |
| 14-Jul-2017 | 2 | Updated table in Section: *Features.*<br>Updated values in *Table 3: Absolute maximum ratings* and added note.<br>Updated Max. value in *Table 4: Thermal data*.<br>Updated *Table 5: Power section*.<br>Updated *Table 8: Low-side driver parameters (VCC = 13 V)*.<br>Updated *Table 9: Protections and diagnostics (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*.<br>Updated *Table 10: MultiSense (7 V < VCC < 18 V; -40 °C < Tj < 150 °C)*.<br>Added *Figure 6: Input reset time for HSD-fault unlatch*.<br>Added *Section 3: Protections Section 4: Typical application schematic Section 5: MultiSense operation, Section 6: Reverse battery protection, Section 7: Open-load detection in off-state, Section 8: Immunity against transient electrical disturbances, Section 9: Package and PCB thermal data.* |
| 03-Nov-2017 | 3 | Updated *Figure 1*, *Table 2: Pin definitions and functions*.<br>Added *Table 3: Suggested connection for unused and not connected pins.*<br>Updated *Table 4: Absolute maximum ratings*, *Table 6: Power section*, *Table 9: Gate driver for external MOS parameters (VCC = 13 V), Table 10: Protections and diagnostics (7 V < VCC < 18 V; -40 °C < Tj < 150 °C), Table 11: MultiSense (7 V < VCC < 18 V; -40 °C < Tj < 150 °C).*<br>Added *Figure 5: Definition of the low-side switching times* and *Figure 6: Definition of the high-side switching times*.<br>Updated *Table 13: On-state fault conditions- truth table.*<br>Added *Figure 14: Gate driver low side rise time normalized vs Cg = 4.7nF* and *Figure 15: Gate driver low side fall time normalized vs Cg = 4.7nF, Section 5.2: Multisense diagnostics flag in fault conditions* and *Section 6: VREG* and *Driver_LS Block, Figure 21: Thermal impedance junction ambient single pulse* and *Table 17: Thermal parameters*.<br>Minor text changes. |
| 11-Dec-2017 | 4 | Document status promoted from target to production data.<br>Updated features in cover page.<br>Minor text changes. |

**Table 20. Document revision history (continued)**

| Date | Revision | Description of changes |
|---|---|---|
| 29-Jan-2018 | 5 | Typo error. |
| 19-Jul-2018 | 6 | Updated *Table 4: Absolute maximum ratings* (add $V_{BAT}$ and $V_{CP}$ values).<br>Updated *Table 10: Protections and diagnostics (7 V < $V_{CC}$ < 18 V; -40 °C < $T_j$ < 150 °C)* (changed Min. value in $t_{DEL\_OVL\_LSD}$; added Min. and Max. value in $V_{GS\_CP}$ ).<br>Updated *Figure 19: Rthj-amb vs PCB copper area in open box free air condition*.<br>Updated *Figure 21: Thermal impedance junction ambient single pulse*.<br>Updated *Table 17: Thermal parameters*. |