TWR-K21D50M Tower Module

User's Manual

Rev. 1.0

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1 TWR-K21D50M

The TWR-K21D50M microcontroller module is designed to work either in standalone mode or as part of the Freescale Tower System, a modular development platform that enables rapid prototyping and tool re-use through reconfigurable hardware. Take your design to the next level and begin constructing your Tower System today by visiting www.freescale.com/tower for additional Tower System microcontroller modules and compatible peripherals. For TWR-K21D50M-specific information and updates, visit www.freescale.com/TWR-K21D50M

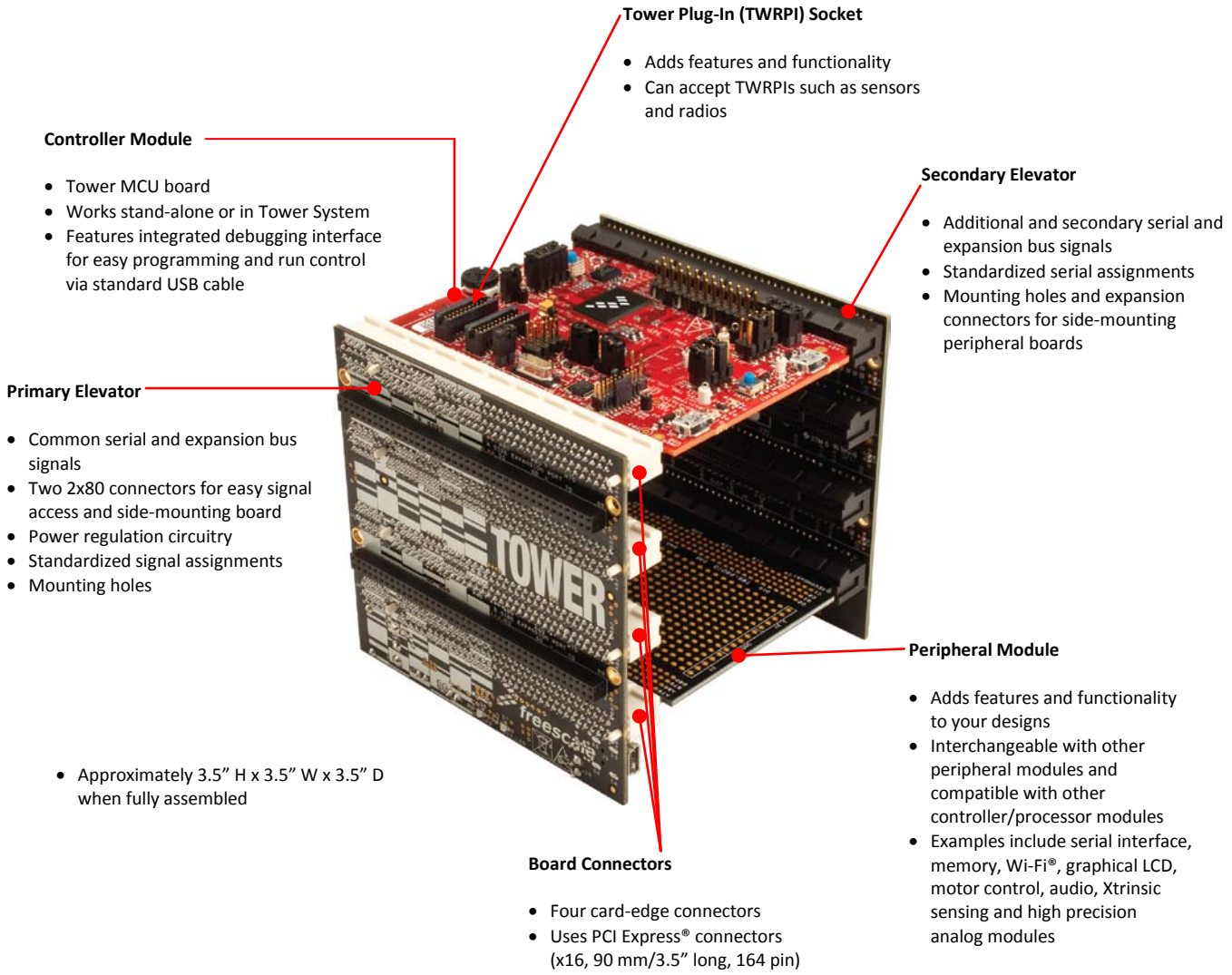

Figure 1. Freescale Tower System Overview

2 Contents

The TWR-K21D50M contents include:

- TWR-K21D50M board assembly
- 3 ft A to micro-B USB cable for debug interface and power or MK21DN512VMB5 USB interface
- CR2025 coin cell battery for VBAT power supply
- Quick Start Guide

3 TWR-K21D50M Features

- Tower-compatible microcontroller module
- MK21DN512VMB5 MCU (50 MHz, 512 KB Flash, 64 KB RAM, low power, 121 MAPBGA package)
- Dual-role USB interface with Micro-AB USB connector
- General-purpose Tower Plug-in (TWRPI) socket
- On-board debug circuit: MC9S08JM60 open source JTAG (OSJTAG) with virtual serial port
- Three-axis accelerometer (MMA8451Q)
- Four (4) user-controllable LEDs
- Two (2) user pushbutton switches for GPIO interrupts
- One (1) user pushbutton switch for MCU reset
- Potentiometer
- Independent, battery-operated power supply for Real Time Clock (RTC) and tamper detection modules

NOTE: The TWR-K21D50M contains some components that are reserved for future revisions of this board and are not functional with the MK21DN512VMB5 MCU.

4 Get to Know the TWR-K21D50M

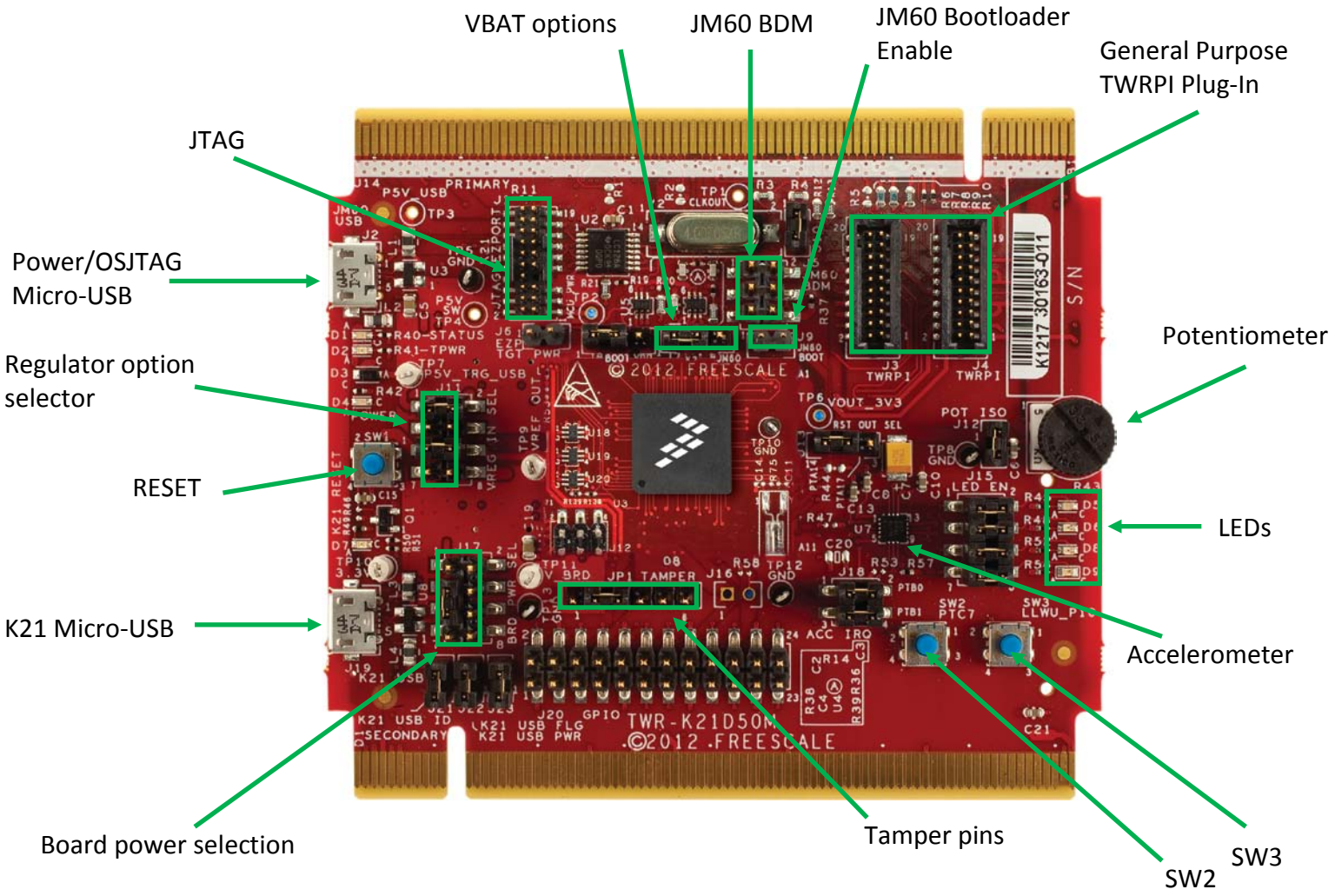

Figure 2. Front side of TWR-K21D50M module

(TWRPI devices not shown)

Battery Receptacle

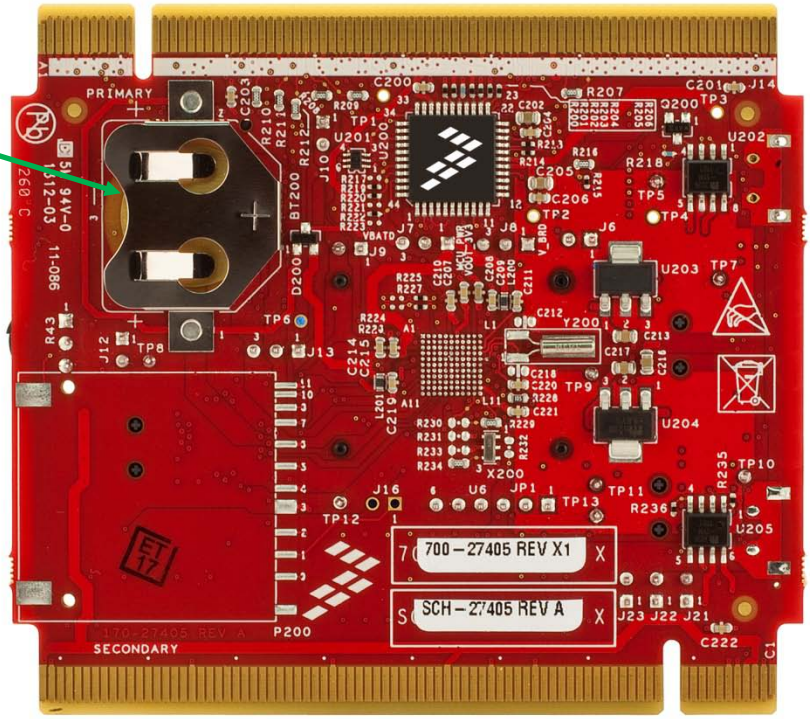

Figure 3. Back side of TWR-K21D50M

5 Reference Documents

The documents listed below should be referenced for more information on the Kinetis K Series, Tower System, and MCU Modules. These can be found in the documentation section of http://www.freescale.com/TWR-K21D50M or http://www.freescale.com/kinetis

- TWR-K21D50M-SCH: Schematics
- TWR-K21D50M-PWA: Design Package
- K21P81M50SF4RM: Reference Manual
- Tower Configuration Tool
- Tower Mechanical Drawing

6 Hardware description

The TWR-K21D50M is a Tower MCU Module featuring the K21DN512VMB5—a Kinetis K Series microcontroller in a 121 MAPBGA package with a USB 2.0 full-speed on-the-go (OTG) controller, system security and tamper detection, and a secure real-time clock with an independent battery supply. It is intended for use in the Freescale Tower System but can also operate stand-alone. An on-board OSJTAG debug circuit provides a JTAG interface and a power supply input through a single micro-USB connector.

The block diagram of the TWR-K21D50M board is presented in the following figure:

6.1 Block Diagram

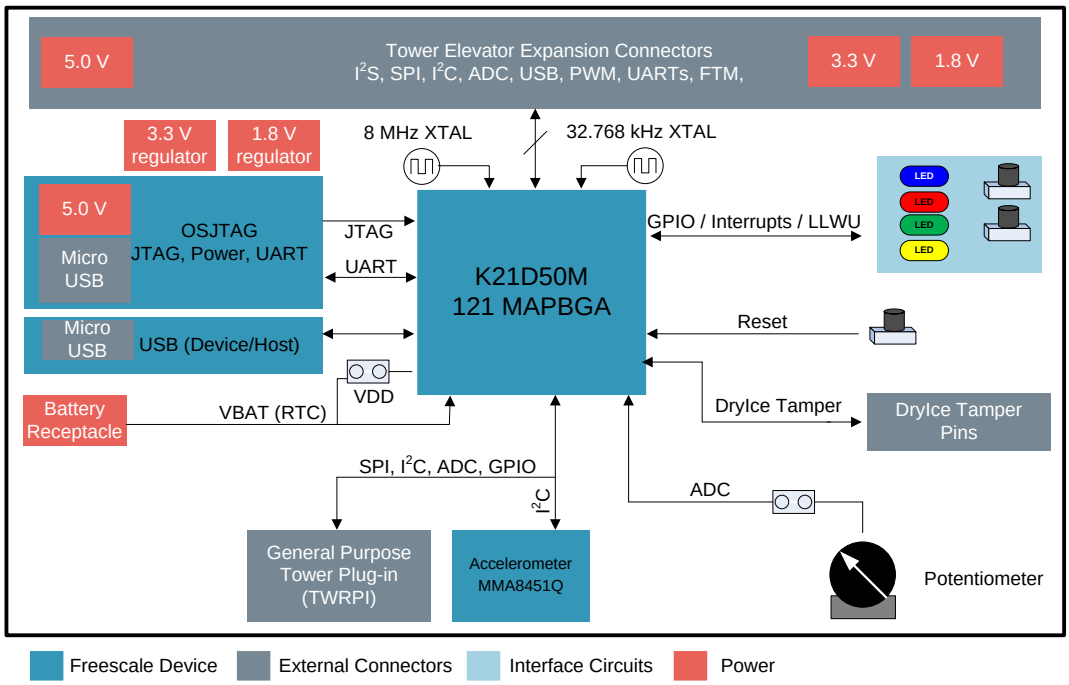

Figure 4. Block Diagram of TWR-K21D50M

6.2 Microcontroller

The TWR-K21D50M features the K21DN512VMB5 MCU. This 50 MHz microcontroller is part of the Kinetis K2x family and is implemented in a 121 MAPBGA package. The following table notes some of the features of the K21DN512VMB5 MCU.

Table 1. Features of MK21DN512VMB5

Feature	Description
Ultra low power	– 11 low-power modes with power and clock gating for optimal peripheral activity and recovery times. – Full memory and analog operation down to 1.71 V for extended battery life – Low-leakage wake-up unit with up to six internal modules and sixteen pins as wake-up sources in low-leakage stop (LLS) and very low-leakage stop (VLLS) modes – Low-power timer for continual system operation in reduced power states
Flash and SRAM	– 512-KB flash featuring fast access times, high reliability, and four levels of security protection – 64 KB of SRAM – No user or system intervention to complete programming and erase functions, and full operation down to 1.71 V
Mixed-signal capability	– High-speed 16-bit ADC with configurable resolution – Single or differential output modes for improved noise rejection – 500-ns conversion time achievable with programmable delay block triggering – Two high-speed comparators providing fast and accurate motor over-current protection by driving PWMs to a safe state – Optional analog voltage reference provides an accurate reference to analog blocks and replaces external voltage references to reduce system cost
Performance	– 50-MHz ARM Cortex-M4 core with DSP instruction set, single cycle MAC, and single instruction multiple data (SIMD) extensions – Up to four channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput – Crossbar switch enables concurrent multi-master bus accesses, increasing bus bandwidth – Independent flash banks allow concurrent code execution and firmware updating with no performance degradation or complex coding routines

Timing and Control	– Three FlexTimers with a total of 12 channels – Hardware dead-time insertion and quadrature decoding for motor control – Carrier modulator timer for infrared waveform generation in remote control applications – Four-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler, or trigger source for ADC conversion and programmable delay block
Connectivity and Communications	– Full-Speed USB Device/Host/On-The-Go with device charge detect capability – Optimized charging current/time for portable USB devices, enabling longer battery life – USB low-voltage regulator that supplies up to 120 mA off chip at 3.3 volts to power external components from 5-volt input – Four UARTs: o one UART that supports RS232 with flow control, RS485, ISO7816, IrDA, and CEA709.1-B (LON) o three UARTs that support RS232 with flow control and RS485 – One Inter-IC Sound (I^2S) serial interface for audio system interfacing – Two DSPI modules and two I^2C modules
Reliability, Safety and Security	– Hardware encryption co-processor for secure data transfer and storage. Faster-than-software implementations with minimal CPU loading. Supports a wide variety of algorithms - DES, 3DES, AES, MD5, SHA-1, SHA-256 – System security and tamper detection with secure real-time clock (RTC) and independent battery supply. Secure key storage with internal/external tamper detection for unsecured flash, temperature, clock, and supply voltage variations and physical attack detection – Memory protection unit provides memory protection for all masters on the crossbar switch, increasing software reliability – Cyclic redundancy check (CRC) engine validates memory contents and communication data, increasing system reliability – Independently-clocked COP guards against clock skew or code runaway for fail-safe applications such as the IEC 60730 safety standard for household appliances – External watchdog monitor drives output pin to safe state for external components in the event that a watchdog timeout occurs – Included in Freescale's product longevity program, with assured supply for a minimum of 10 years after launch

6.3 Clocking

Kinetis K Series MCUs start up from an internal digitally controlled oscillator (DCO). Software can enable the main external oscillator (EXTAL0/XTAL0) if desired. The external oscillator/resonator can range from 32.768 KHz up to 32 MHz. An 8-MHz crystal is the default external source for the MCG oscillator inputs (XTAL/EXTAL).
A 32.768-kHz crystal is connected to the RTC oscillator inputs by default.

By populating isolation resistors, other external clock sources for the K21DN512VMB5 include the CLKIN0 signal, which can be provided through the TWR-ELEV module or pin 20 of TWRPI connector J3.

6.4 System Power

When installed into a Tower System, the TWR-K21D50M can be powered from either an on-board source or from another source in the assembled Tower System.

In stand-alone operation, the main power source (5.0 V) for the TWR-K21D50M module is derived from either the OSJTAG USB micro-B connector (J2) or the K21DN512VMB5 USB micro-AB connector (J19). Two low-dropout regulators provide 3.3 V and 1.8 V supplies from the 5.0 V input voltage. Additionally, the 3.3 V regulator built into the K21DN512VMB5 MCU can be selected to power the 3.3 V bus. All of the user-selectable options can be configured using two headers, J11 and J17. Refer to sheet 5 of the TWR-K21D50M schematics for more details.

DryIce and RTC VBAT

The DryIce tamper detection module and the Real Time Clock (RTC) module on the K21DN512VMB5 have two modes of operation: system power-up and system power-down. During system power-down, the tamper detection module and the RTC are powered from the backup power supply (VBAT) and electrically isolated from the rest of the MCU. The TWR-K21D50M provides a battery receptacle for a coin cell battery that can be used as the VBAT supply. This receptacle can accept common 3-V lithium coin cell batteries that are 20 mm in diameter.

6.5 Debug Interface

There are two debug interface options provided: the on-board OSJTAG circuit and an external ARM JTAG connector. The ARM-JTAG connector (J1) is a standard 2x10-pin connector that provides an external debugger cable access to the JTAG interface of the K21DN512VMB5. Alternatively, the on-board OSJTAG debug interface can be used to access the debug interface of the K21DN512VMB5.

6.6 OSJTAG

An on-board MC9S08JM60 based Open Source JTAG (OSJTAG) circuit provides a JTAG debug interface to the K21DN512VMB5. A standard USB A male to micro-B male cable (provided) can be used for debugging via the USB connector (J2). The OSJTAG interface also provides a USB to serial bridge. Drivers for the OSJTAG interface are provided in the P&E Micro OSBDM/OSJTAG Tower Toolkit. These drivers and more utilities can be found online at http://www.pemicro.com/osbdm.

Cortex Debug Connector

The Cortex Debug connector is a 20-pin (0.05") connector providing access to the SWD, JTAG, cJTAG, and EzPort signals available on the K21 device. The pinout and K21 pin connections to the debug connector (J1) are shown in Table 2.

Table 2. Cortex Debug connector

Pin	Function	TWR-K21D50M Connection
1	VTref	3.3 V MCU supply (MCU_PWR)
2	TMS / SWDIO	PTA3/UART0_RTS_b/FTM0_CH0/**JTAG_TMS/SWD_DIO**
3	GND	GND
4	TCK / SWCLK	PTA0/UART0_CTS_b/FTM0_CH5/**JTAG_CLK/SWD_CLK/EZP_CLK**
5	GND	GND
6	TDO / SWO	PTA2/UART0_TX/FTM0_CH7/**JTAG_TDO/TRACE_SWO/EZP_DO**
7	Key	—
8	TDI	PTA1/UART0_RX/FTM0_CH6/**JTAG_TDI/EZP_DI**
9	GNDDetect	PTA4/FTM0_CH1/MS/NMI_b/**EZP_CS_b**
10	nRESET	**RESET_b**
11	Target Power	5 V supply (via jumper J6)
12	TRACECLK	PTE0/mADC0_SE10/SPI1_PCS1/UART1_TX/**TRACE_CLKOUT**/I2C1_SDA/RTC_CLKOUT
13	Target Power	5 V supply (via jumper J6)
14	TRACEDATA[0]	PTE4/LLWU_P2/SPI1_PCS0/UART3_TX/**TRACE_D0**
15	GND	GND
16	TRACEDATA[1]	PTE3/ADC0_DM2/mADC0_DM1/SPI1_SIN/UART1_RTS_b/**TRACE_D1**/SPI1_SOUT
17	GND	GND
18	TRACEDATA[2]	PTE2/LLWU_P1/ADC0_DP2/mADC0_DP1/SPI1_SCK/UART1_CTS_b/**TRACE_D2**
19	GND	GND
20	TRACEDATA[3]	PTE1/LLWU_P0/mADC0_SE11/SPI1_SOUT/UART1_RX/**TRACE_D3**/I2C1_SCL/SPI1_SIN

6.7 Accelerometer

An MMA8451Q digital accelerometer is connected to the K21DN512VMB5 MCU through an I^2C interface (I2C1) and GPIO/IRQ signals (PTB0 and PTB1).

6.8 Potentiometer, Pushbuttons, LEDs

The TWR-K21D50M also features:

- a potentiometer connected to an ADC input signal (ADC0_SE12).
- two pushbutton switches (SW2 and SW3 connected to PTC7 and PTC6, respectively)
- four user-controllable LEDs connected to GPIO signals (optionally isolated using jumpers):
    - Green LED (D5) to PTD4
    - Yellow LED (D6) to PTD5
    - Red LED (D8) to PTD6
    - Blue LED (D9) to PTD7

6.9 General Purpose Tower Plug-in (TWRPI) Socket

The TWR-K21D50M features a socket (J3 and J4) that can accept a variety of different Tower Plug-in modules featuring sensors, RF transceivers, and other peripherals. The General Purpose TWRPI socket provides access to I^2C, SPI, IRQs, GPIOs, timers, analog conversion signals, TWRPI ID signals, reset, and voltage supplies. The pinout for the TWRPI Socket is defined in Table 3.

Table 3. General Purpose TWRPI socket pinout

J4	
Pin	Description
1	5 V VCC
2	3.3 V VCC
3	GND
4	3.3 V VDDA
5	VSS (Analog GND)
6	VSS (Analog GND)
7	VSS (Analog GND)
8	ADC: Analog 0
9	ADC: Analog 1
10	VSS (Analog GND)
11	VSS (Analog GND)
12	ADC: Analog 2
13	VSS (Analog GND)
14	VSS (Analog GND)
15	GND
16	GND
17	ADC: TWRPI ID 0
18	ADC: TWRPI ID 1
19	GND
20	Reset

J3	
Pin	Description
1	GND
2	GND
3	I2C: SCL
4	I2C: SDA
5	GND
6	GND
7	GND
8	GND
9	SPI: MISO
10	SPI: MOSI
11	SPI: SS
12	SPI: CLK
13	GND
14	GND
15	GPIO: GPIO0/IRQ
16	GPIO: GPIO1/IRQ
17	UART: UART_RX or GPIO: GPIO2
18	UART: UART_TX or GPIO: GPIO3
19	UART: UART_CTS or GPIO: GPIO4/Timer
20	UART: UART_RTS or GPIO: GPIO5/Timer

6.10 USB

The K21DN512VMB5 features a full-speed/low-speed USB module with OTG/Host/Device capability and built-in transceiver. The TWR-K21D50M routes the USB D+ and D- signals from the K21DN512VMB5 MCU directly to the on-board micro-USB connector (J19).

A power supply switch with an enable input signal and over-current flag output signal is used to supply power to the USB connector when the K21DN512VMB5 is operating in host mode. PTC8 is connected to the flag output signal and PTC9 is used to drive the enable signal. Both PTC8 and PTC9 port pins can be isolated with jumpers (J23 and J22, respectively) if needed.

7 TWR-K21D50M Jumper Options and Headers

The following is a list of all of the jumper options on the TWR-K21D50M. The default installed jumper settings are indicated by white text on a black background.

Table 4. TWR-K21D50M Jumper Options

Option	Jumper	Setting	Description
MCU power connection	J8	**1-2**	Connect on-board 3.3 V or 1.8 V supply (V_BRD) to MCU VDD
		2-3	Connect K21 USB regulator output to MCU VDD
VBAT power source	J7	**1-2**	Connect VBAT to on-board 3.3 V or 1.8 V supply
		2-3	Connect VBAT to the higher voltage between MCU supply (MCU_PWR) or coin cell supply (VBATD)
JTAG board power selection	J6	ON	Connect OSJTAG 5V output (P5V_TRG_USB) to JTAG port (supports powering board from JTAG pod supporting 5V supply output)
		OFF	Disconnect OSJTAG 5V output (P5V_TRG_USB) from JTAG port
OSJTAG bootloader selection	J9	ON	OSJTAG bootloader mode (OSJTAG firmware reprogramming)
		OFF	Debugger mode
V_BRD power source (Board Power Selector)	J17	1-2	Connect K21 USB regulator output (VOUT_3V3) to on-board supply (V_BRD)
		3-5	Connect 3.3 V on-board regulator output (P3V3) to on-board supply (V_BRD)
		5-7	Connect 1.8 V on-board regulator output (P1V8) to on-board supply (V_BRD)
VREG IN Selector	J11	**1-2**	OSJTAG 5V output (P5V_TRG_USB) connected to on-board regulator input (VREG_IN)
		5-6	VBUS signal on micro-USB connector J19 connects to K21_VREGIN to allow stand-alone USB operation
		6-8	VBUS signal from Tower Elevator connector connects to K21_VREGIN to allow USB operation with complete Tower System
USB ID connection	J21	**ON**	Connect PTD7 to USB ID pin
		OFF	Disconnect PTD7 from USB ID pin

Option	Jumper	Setting	Description
USB power enable	J22	**ON**	Connect PTC9 to USB power enable on power switch MIC2026
		OFF	Disconnect PTC9 from USB power enable on power switch MIC2026
USB over-current flag	J23	**ON**	Connect PTC8 to over-current flag on power switch MIC2026
		OFF	Disconnect PTC8 from over-current flag on power switch MIC2026
General Purpose TWRPI V_BRD power enable	J10	**ON**	Connect on-board 1.8 V or 3.3 V supply (V_BRD) to TWRPI 3-V power (GPT_VBRD)
		OFF	Disconnect on-board 1.8 V or 3.3 V supply (V_BRD) from TWRPI 3-V power (GPT_VBRD)
Accelerometer IRQ connection	J18	**1-2**	Connect PTB0 to INT1 pin of accelerometer
		3-4	Connect PTB1 to INT2 pin of accelerometer
		OFF	Disconnect PTB0 and/or PTB1 from INT1 and/or INT2 of accelerometer
Potentiometer connection	J12	**ON**	Connect potentiometer to ADC0_SE12
		OFF	Disconnect potentiometer from ADC0_SE12
LED connections	J15	**1-2**	Connect PTD4 to green LED (D5)
		3-4	Connect PTD5 to yellow LED (D6)
		5-6	Connect PTD6 to red LED (D8)
		7-8	Connect PTD7 to blue LED (D9)
		OFF	Disconnect PTD[4:7] from associated LED
GPIO RESET_OUT_B Connection	J13	**1-2**	Connect PTA14 to RESET_OUT_B signal
		2-3	Connect PTA17 to RESET_OUT_B signal
		OFF	Leave RESET_OUT_B signal disconnected

8 Useful links

- www.freescale.com
  - freescale.com/Kinetis
  - freescale.com/TWR-K21D50M
  - freescale.com/codewarrior (CodeWarrior v10.2 or later)
- www.iar.com/freescale
- www.pemicro.com
  - http://www.pemicro.com/osbdm
  - OSBDM/OSJTAG Virtual Serial Toolkit
- www.segger.com
  - http://www.segger.com/jlink-flash-download.html

Revision History

Revision	Date	Description
1.0	July, 2012	Initial release.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

TWR-K21D50M-UM
Rev. 1.0
08/2012