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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)[c]	Q_g (Typ.)
- 100	0.138 at V_{GS} = - 10 V	- 16.3	24 nC
	0.141 at V_{GS} = - 7.5 V	- 16.1	
	0.142 at V_{GS} = - 6 V	- 16.1	

FEATURES

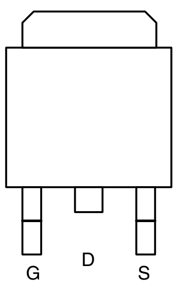
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT

APPLICATIONS

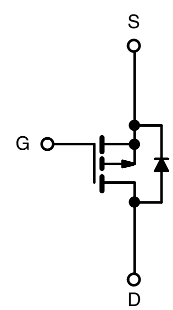
- DC/DC Converters
- Motor Control

TO-263



Top View

Ordering Information:
SUM25P10-138-E3 (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 16.7	A
	T_C = 125 °C		- 9.6	
Pulsed Drain Current (t = 100 µs)		I_{DM}	- 40	
Avalanche Current	L = 0.1 mH	I_{AS}	- 25	
Single Pulse Avalanche Energy[a]		E_{AS}	31.25	mJ
Power Dissipation	T_C = 25 °C	P_D	88.2[b]	W
	T_A = 25 °C		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient Free Air	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.7	

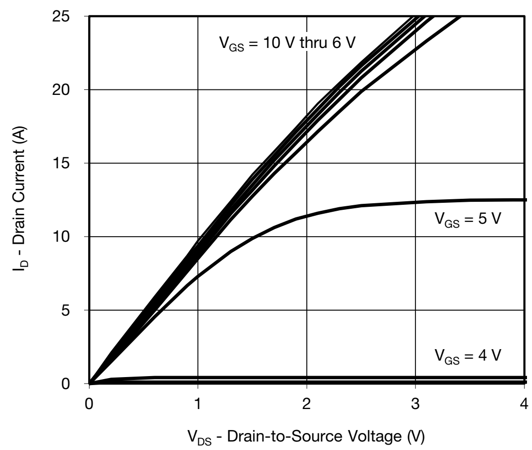
Notes:
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. T_C = 25 °C

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	- 2		- 4	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 105		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = - 250 µA		6.6		mV/°C
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 100 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 125 °C			- 50	
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 150 °C			- 200	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = - 5 V, V_{GS} = - 10 V	- 20			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 6 A		0.115	0.138	Ω
		V_{GS} = - 7.5 V, I_D = - 6 A		0.117	0.141	
		V_{GS} = - 6 V, I_D = - 6 A		0.118	0.142	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 6 A		18		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 50 V, f = 1 MHz		2110		pF
Output Capacitance	C_{oss}			105		
Reverse Transfer Capacitance	C_{rss}			58		
Total Gate Charge[c]	Q_g	V_{DS} = - 50 V, V_{GS} = - 10 V, I_D = - 6.7 A		40	60	nC
		V_{DS} = - 50 V, V_{GS} = - 6 V, I_D = - 6.7 A		24	36	
Gate-Source Charge[c]	Q_{gs}			12.5		
Gate-Drain Charge[c]	Q_{gd}			6.7		
Gate Resistance	R_g	f = 1 MHz	2	8	16	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 10 Ω $I_D \cong$ - 5 A, V_{GEN} = - 10 V, R_g = 1 Ω		7	14	ns
Rise Time[c]	t_r			12	20	
Turn-Off Delay Time[c]	$t_{d(off)}$			46	70	
Fall Time[c]	t_f			40	60	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 10 Ω $I_D \cong$ - 5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		12	20	
Rise Time[c]	t_r			105	160	
Turn-Off Delay Time[c]	$t_{d(off)}$			36	54	
Fall Time[c]	t_f			34	51	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				- 16.3	A
Pulsed Current (t = 100 µs)	I_{SM}				- 40	A
Forward Voltage[a]	V_{SD}	I_F = - 5 A, V_{GS} = 0 V		- 0.85	- 1.5	V
Reverse Recovery Time	t_{rr}	I_F = - 5 A, dI/dt = 100 A/µs		70	105	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			- 7	- 14	A
Reverse Recovery Charge	Q_{rr}			220	330	nC

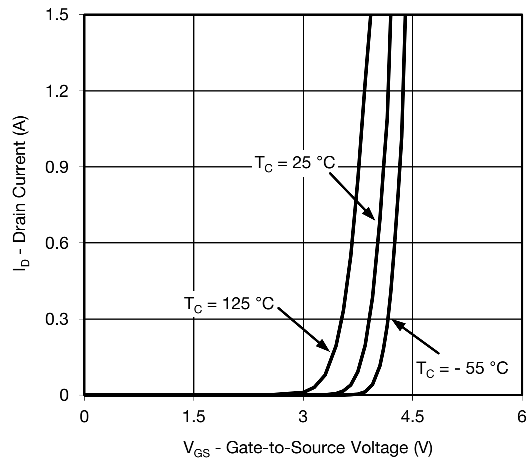
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

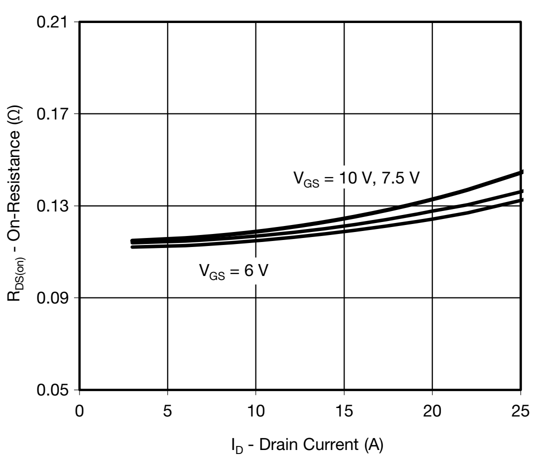
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



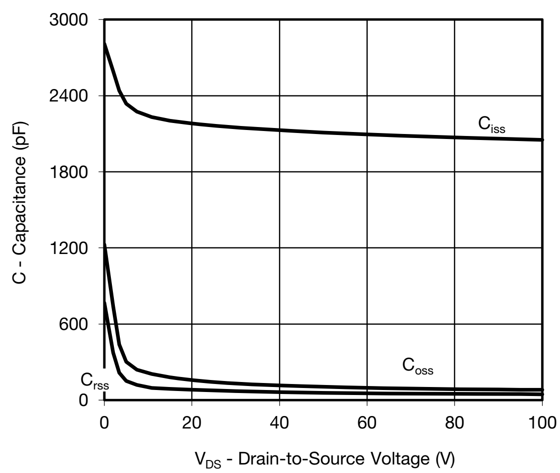
Output Characteristics



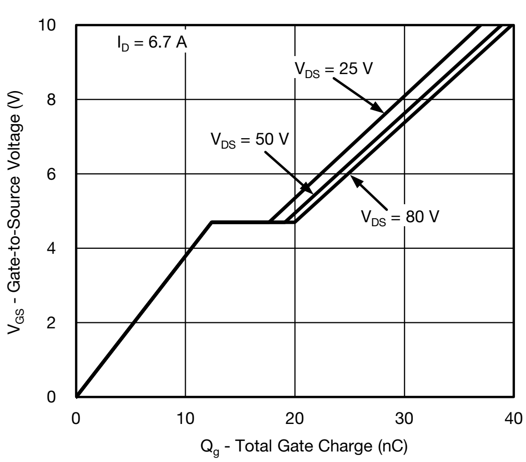
Transfer Characteristics



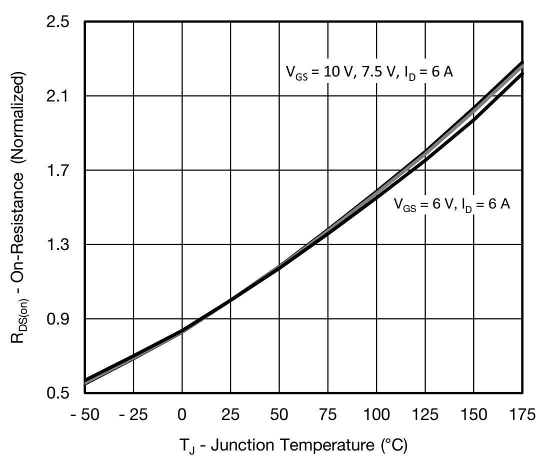
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

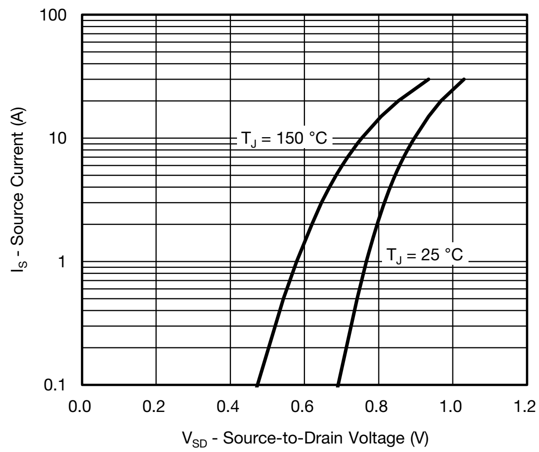


Gate Charge

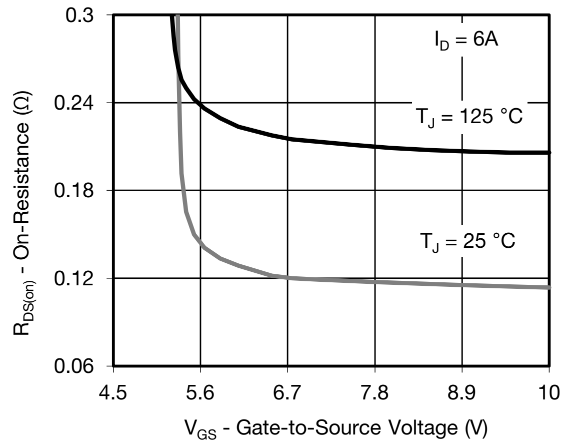


On-Resistance vs. Junction Temperature

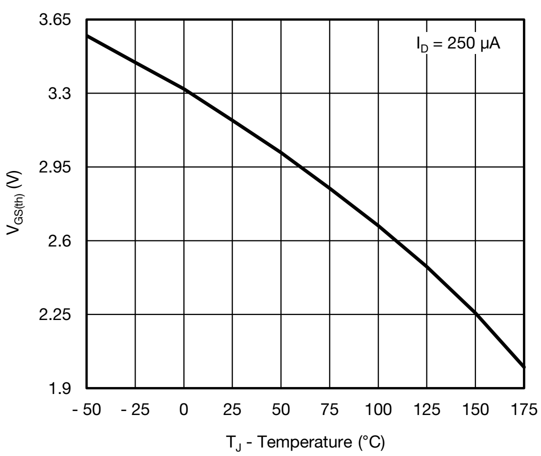
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



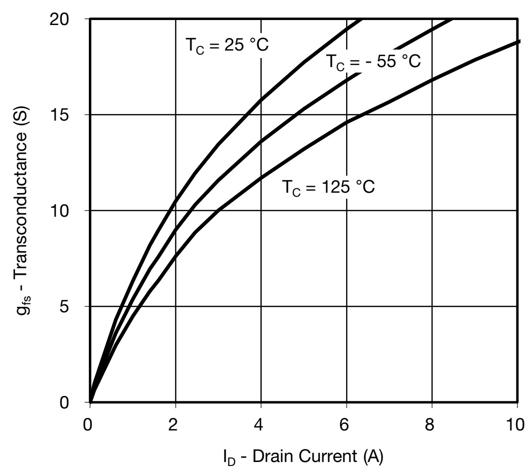
Source-Drain Diode Forward Voltage



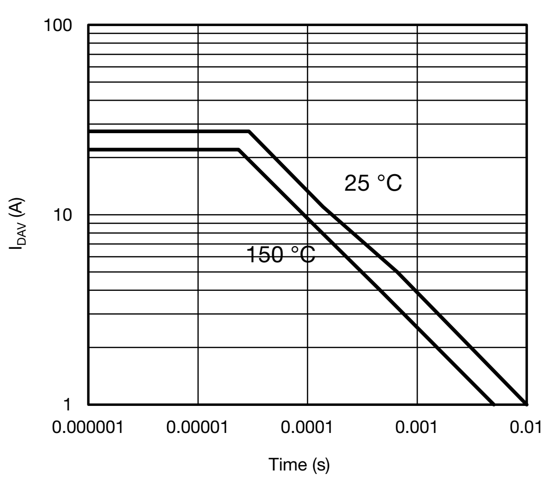
On-Resistance vs. Gate-to-Source Voltage



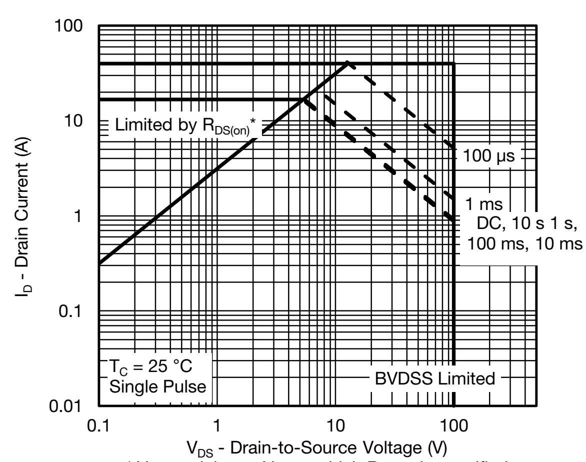
Threshold Voltage



Transconductance



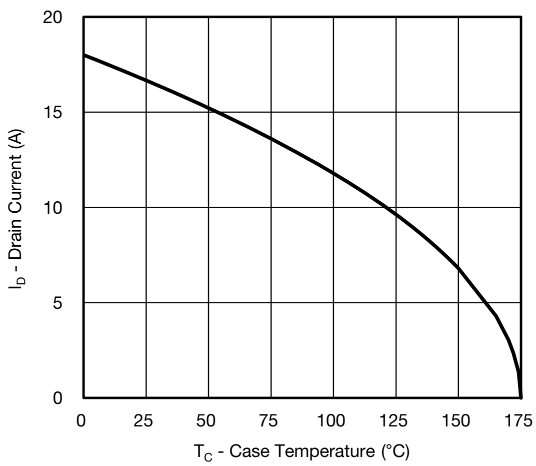
Single Pulse Avalanche Capability



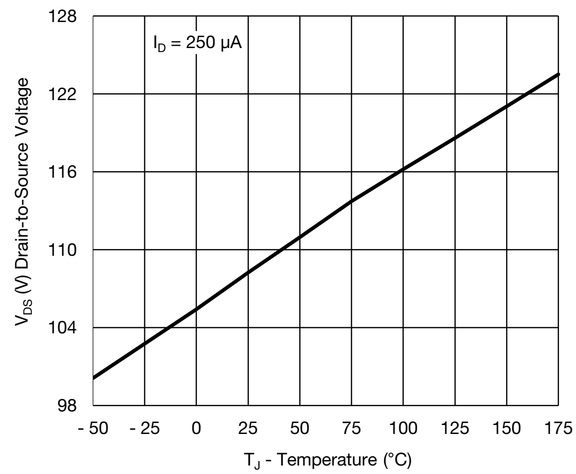
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

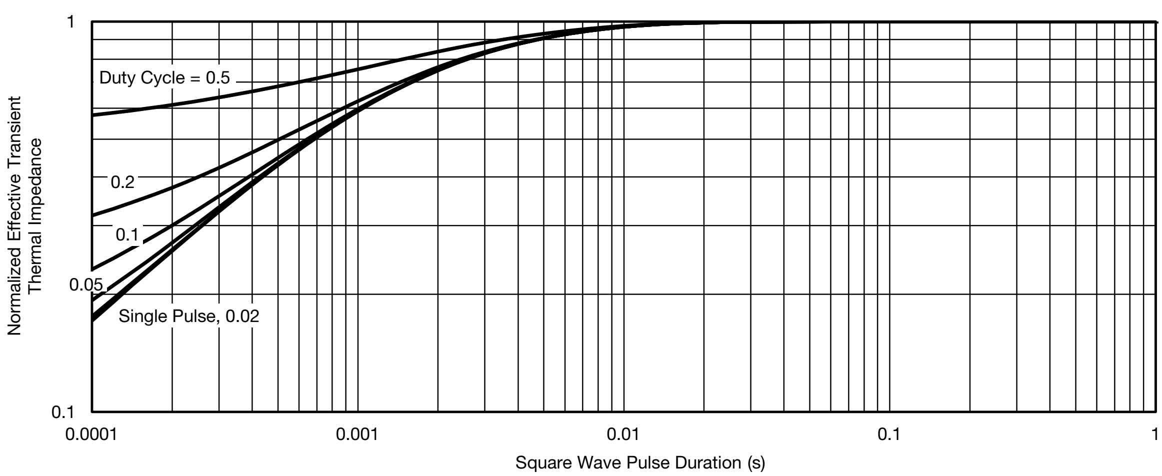


Current Derating*



Drain Source Breakdown vs. Junction Temperature

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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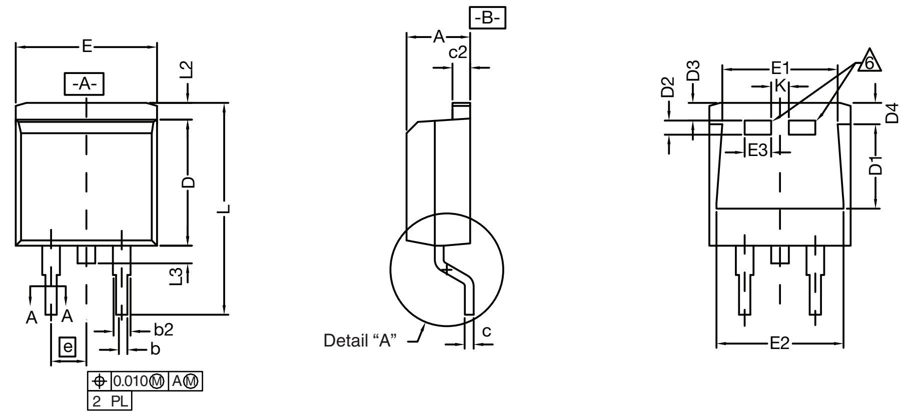
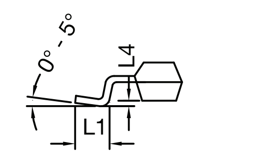
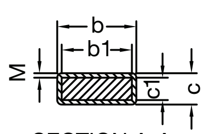
TO-263 (D^2PAK): 3-LEAD





DETAIL A (ROTATED 90°)



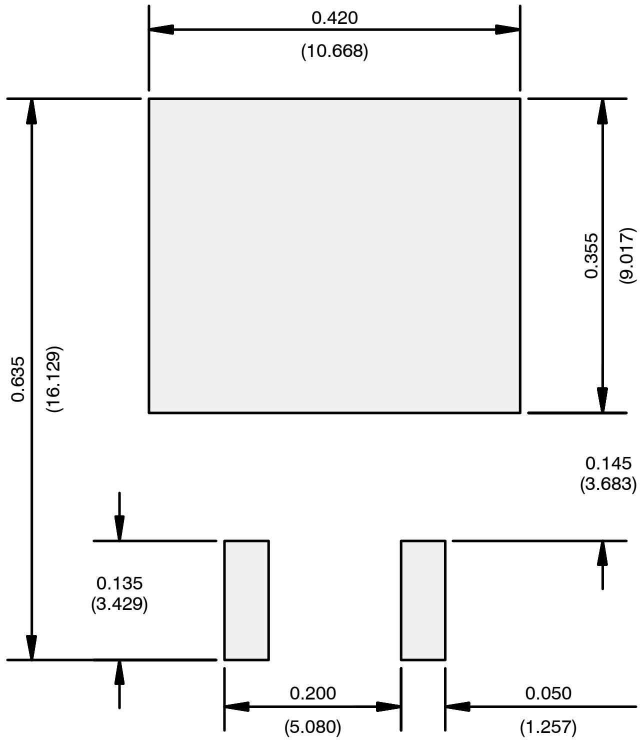
SECTION A-A

DIM.		INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

ECN: T13-0707-Rev. K, 30-Sep-13
DWG: 5843

Notes
1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D^{2}PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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