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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China







MICROCHIP

MX555ABD100M000

Ultra-Low Jitter 100MHz HCSL XO

ClockWorks® FUSION

General Description

The MX555ABD100M000 is an ultra-low phase jitter XO with HCSL output optimized for high line rate applications.

Applications

- PCI-Express
- Storage

Absolute Maximum Ratings

Supply Voltage (VIN)	+4.6V
Lead Temperature (soldering, 10s)	260°C
Storage Temperature (T _c)	125°C
ESD Rating (HBM)	2kV

Features

- 100MHz HCSL
- PCIe Gen1/Gen2/Gen3/Gen4* compliant
- Typical phase noise:
 - 97fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

*Internal test

Operating Ratings

Supply Voltage (VIN)	+ 2.375 V to $+3.63$ V
Ambient Temperature (TA)	40°C to +85°C

Electrical Characteristics

VDD = $2.5V \pm 5\%$ or $3.3V \pm 10\%$, -40° C to $+85^{\circ}$ C, outputs terminated with 50 Ohms to VSS.¹

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			100		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		166 97		fsRMS
Tstart	Start-Up Time				10	ms
TR/TF	Rise/Fall time	20%-80%	150	300	450	ps
	Duty Cycle		48	50	52	%
VOH	Output High Voltage	HCSL output levels	660	700	850	mV
VOL	Output Low Voltage	HCSL output levels	-150	0	27	mV
VOVS	Max Output Including Overshoot				VOH + 0.3	V
VUDS	Min Output Including Undershoot		VOL - 0.3			V
VRB	Ringback Voltage		0.2			V
VOX	Absolute Crossing Point		250	350	550	mV
Vswing	Peak to Peak Output Voltage Swing		640	700	950	mV

Notes:

- 1. Guaranteed after thermal equilibrium.
- 2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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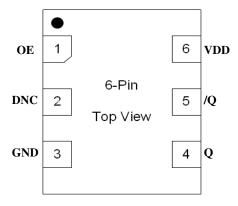
March 16, 2017 MX555AB1-1510 Revision 1.0 tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ABD100M000	MX555A	BD1000	Tube	6-Pin 5mm x 3.2mm LGA
MX555ABD100M000 TR	MX555A	BD1000	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	HCSL	Clock Output Frequency = 100MHz
6	VDD	PWR		Power Supply

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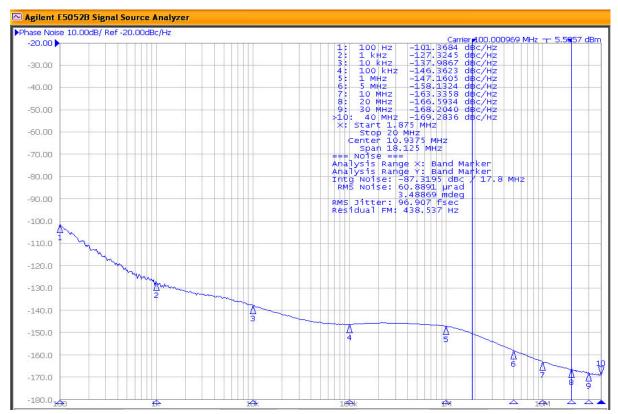


Figure 1. HCSL Output 100MHz 1.875MHz-20MHz 97fs

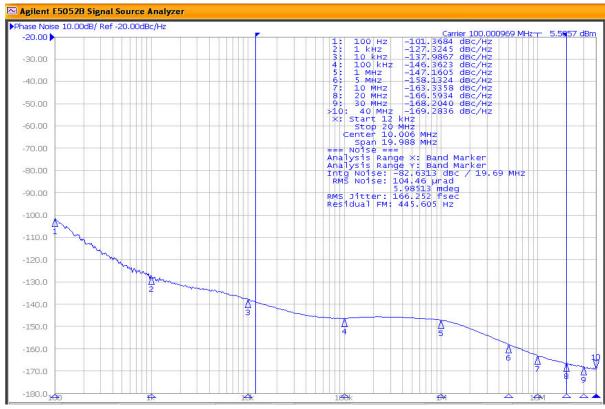
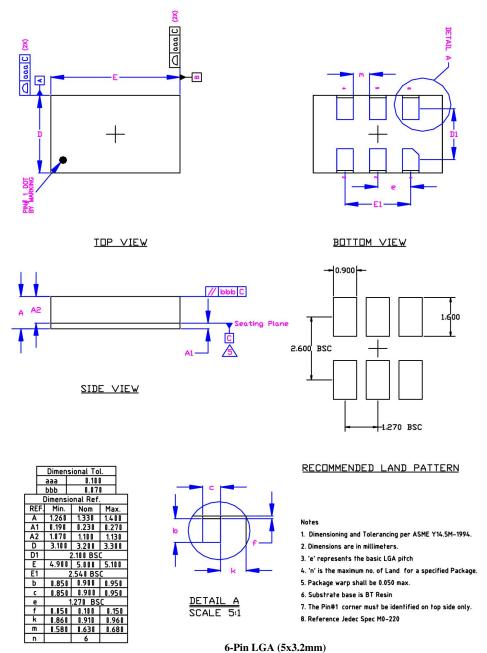


Figure 2. HCSL Output 100MHz 12kHz-20MHz 166fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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