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User's Manual

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The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

SH-2 SH7047 Group

Hardware Manual

Renesas 32-Bit RISC Microcomputer SuperH™ RISC engine Family/ SH7000 Series

SH7047F HD64F7047
SH7049 HD6437049

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Rev.2.00 2004.09

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are they are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

Precaution on Handling HCAN2

Restrictions apply to the use of the HCAN2. Carefully read section 15.8, Usage Notes, beforehand.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
    - CPU and System-Control Modules
    - On-Chip Peripheral Modules

      The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

    i) Feature
    ii) Input/Output Pin
    iii) Register Description
    iv) Operation
    v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. Electrical Characteristics
8. Appendix
    - List of registers, product code lineup, and package dimensions
    - Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

9. Index

Preface

The SH7047 group single-chip RISC (Reduced Instruction Set Computer) microprocessor includes a Renesas -original RISC CPU as its core, and the peripheral functions required to configure a system.

Target users: This manual was written for users who will be using the SH7047 group Micro-Computer Unit (MCU) in the design of application systems. Users of this manual are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the SH7047 group MCU to the above users.
Refer to the SH-1, SH-2, SH-DSP Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- Product names
  The following products are covered in this manual.

Product Classifications and Abbreviations

Basic Classification	On-Chip ROM Classification		Product Code
SH7047 (100-pin version)	SH7047F	Flash memory version (ROM: 256 kbytes)	HD64F7047
	SH7049	Mask ROM version (ROM: 128 kbytes)	HD6437049

In this manual, the product abbreviations are used to distinguish products. For example, 100-pin products are collectively referred to as the SH7047, an abbreviation of the basic type's classification code. There are two versions of each: a flash memory version and a mask ROM version. When a description is limited to the flash memory version alone, the character F is added at the end of the abbreviation, such as SH7047F. When a description is limited to the mask ROM version alone, an abbreviation that is determined by the ROM size is used; SH7049 is used to indicate the mask ROM version.

- The typical product

  The HD64F7047 is taken as the typical product for the descriptions in this manual. Accordingly, when using an HD6437049, simply replace the HD64F7047 in those references where no differences between products are pointed out with HD6437049. Where differences are indicated, be aware that each specification apply to the products as indicated.
- In order to understand the overall functions of the chip

  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions

  Read the SH-1, SH-2, SH-DSP Software Manual.
- In order to understand the details of a register when the user knows its name

  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bit names, and initial values of the registers are summarized in Appendix A, Internal I/O Register.

Rules:	Register name:	The following notation is used for cases when the same or a similar function, e.g. serial communication, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB (most significant bit) is on the left and the LSB (least significant bit) is on the right.

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SH7047 Group manuals:

Document Title	Document No.
SH7047 Group Hardware Manual	This manual
SH-1, SH-2, SH-DSP Software Manual	REJ09B0171

Users manuals for development tools:

Document Title	Document No.
SuperH RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	ADE-702-372
SuperH RISC engine Simulator/Debugger User's Manual	ADE-702-186
High-performance Embedded Workshop User's Manual	ADE-702-201

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