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International
IOR Rectifier

iP1201PbF

iPOWIR™ TECHNOLOGY

Dual Output Full Function 2 Phase Synchronous Buck Power Block

Integrated Power Semiconductors, PWM Control & Passives

Features

- 3.14V to 5.5V input voltage
- 0.8V to 3.3V output voltage
- 2 Phase Synchronous Buck Power Block
- 180° out of phase operation
- Single or Dual output capability
- Dual 15A maximum load capability
- Single 2 phase 30A maximum load capability
- 200-400kHz per channel nominal switching frequency
- Over Current Hiccup or Over Current Latch
- External Synchronization capability
- Overvoltage protection
- Independent soft start per output
- Over Temperature protection
- Internal features minimize layout sensitivity *
- Very small outline 15.5mm x 9.25mm x 2.6mm

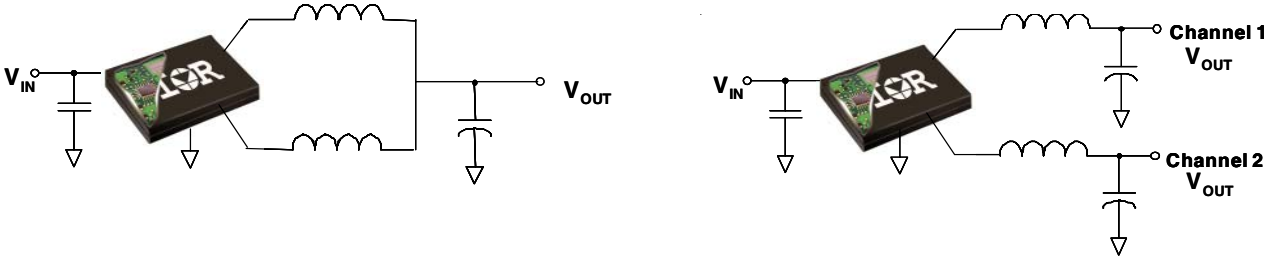
iP1201PbF Power Block

Description

The iP1201PbF is a fully optimized solution for medium current synchronous buck applications requiring up to 15A or 30A. The iP1201PbF is optimized for 2 phase single output applications up to 30A or dual output, each up to 15A with interleaved input. It includes full function PWM control, with optimized power semiconductor chip-sets and associated passives, achieving high power density. Very few external components are required to create a complete synchronous buck power supply.

iPOWIR technology offers designers an innovative space-saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP1201PbF Configurations



Single Output Dual Output

* Although, all of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR block, proper layout techniques should be applied for the design of the power supply board. There are no concerns about unwanted shutdowns common to switching power supplies, if operated as specified. The iPOWIR block will function normally, but not optimally without any additional input decoupling capacitors. Input decoupling capacitors should be added at Vin pin for stable and reliable long term operation. See layout guidelines in datasheet for more detailed information.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{IN}	V_{IN}	-0.3	-	5.8	V	
Feedback	VFB1/VFB2	-0.3	-	6		
Output Overvoltage Sense	$VFB1_S/VFB2_S$	-0.3	-	6		
PGOOD		-0.3	-	6		
ENABLE		-0.3	-	5.8		
Soft Start	SS1/SS2	-0.3	-	6		
Vp-ref		-0.3	-	6		
HICCUP	HICCUP	-0.3	-	6		
SYNC		-0.3	-	6		
Output RMS Current Per Channel	$Iout_{VSW}$	-	-	15	A	2 Independent outputs. See Fig. 3
Block Temperature	T_{BLK}	-40	-	125	°C	Capable of start up over full temperature range. See Note 1.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Voltage Range	V_{IN}	3.14	-	5.5		
Output RMS Current Per Channel	$Iout_{VSW}$	-	-	15	A	2 Independent outputs T_{PCB} = T_{CASE} = 90°C. See Fig. 3
		-	-	11.5	A	2 Independent outputs T_{PCB} = 90°C, T_{CASE} = no airflow, no heatsink. See Fig. 3
Output Voltage Range	V_{OUT}	0.8	-	3.3	V	For V_{IN} = 5V
		0.8	-	2.5		For V_{IN} = 3.3V

Electrical Specifications @ V_{IN} = 5V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Power Loss	P_{LOSS}	-	6.7	8.4	W	f_{SW} = 300kHz, V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 15A
Over Current Shutdown	I_{OC}	-	20	-	A	V_{IN} = 5V, V_{OUT} = 1.5V, f_{SW} = 300KHz, HICCUP pin pulled Low
HICCUP duty cycle	D_{HICCUP}	-	5	-	%	HICCUP pin pulled high, output short circuited.
Soft Start Time	t_{SS}	-	5	-	ms	V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS1} = C_{SS2} = 0.1µF
Reference Voltage	V_{REF}	-	0.80	-	V	I_{OUT} = 2A
V_{OUT} Accuracy	V_{OUT_ACC1}	-3	-	3	%	T_{BLK} = -40°C to 125°C, See Note 1. V_{IN} = 5V, V_{OUT} = 1.5V
	V_{OUT_ACC2}	-2.5	-	2.5		T_{BLK} = 0°C to 125°C, See Note 1. V_{IN} = 5V, V_{OUT} = 1.5V
Error Ampifier 1 & 2 input offset voltage	V_{OS1}, V_{OS2}	-4	-	4	mV	V_{IN} = 5V, V_{OUT} = 1.5V
FB1 / FB2 Input bias current	I_{B1}, I_{B2}	-	-0.1	-	µA	
Error Amplifier source/sink Current	I_{ERR}	-	60	-	µA	
Error Amplifier Transconductance	g_{m1}, g_{m2}	-	2000	-	µmho	
Output Overvoltage Shutdown Threshold	OVP	-	1.15 x V_{OUT}	-	V	See OVP note in Design Guidelines
OVP Fault Propagation Delay	t_{OVP}	-	25	-	µs	Output forced to 1.125Vref
PGOOD Trip Threshold	V_{Th_PGOOD}	-	0.85 x V_{OUT}	-	V	FB1 or FB2 ramping down
PGOOD Output Low Voltage	V_{Lo_PGOOD}	-	0.25	-	V	I_{SINK} = 2mA

Electrical Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Frequency	f_{SW}	170	-	230	kHz	R_T = 48.7kΩ (See Fig.11 for
		255	-	345	kHz	R_T = 30.9kΩ R_T selection)
		340	-	460	kHz	R_T = 21.5kΩ
Oscillator Ramp Voltage	V_{ramp}	-	1.25	-	V	
Sync Frequency Range	f_{SYNC}	480	-	800	kHz	Free running frequency set 20% below sync frequency
Sync Pulse Duration	t_{SYNC}	-	200	-	ns	
Sync, Hiccup High Level Threshold Voltage		2	-	-	V	
Sync, Hiccup Low Level Threshold Voltage		-	-	0.8	V	
V_{IN} Quiescent Current	$I_{IN\_Leakage}$	-	1.0	-	mA	V_{IN} = 5V, ENABLE high
Thermal Shutdown	$Temp_{shdn}$	-	140	-	°C	
Max Duty Cycle	D_{MAX}	90	-	-	%	f_{SW}= 200kHz
Enable Input Logic High	V_{EN-Hi}	2	-	-	V	V_{IN} = V_{MIN} to V_{MAX}
Enable Input Logic Low	V_{EN-Lo}	-	-	0.4	V	V_{IN} = V_{MIN} to V_{MAX}
V_{IN} Undervoltage Lockout Threshold Voltage	V_{IN_UVLO}	-	2.7	-	V	V_{IN} = 5V, ENABLE Pulled Low
Output Disable Soft Start Low Threshold Voltage	V_{SS_Dis}	-	-	0.25	V	SS1 / SS2 Pins Pulled Low

Note 1: Guaranteed to meet specifications from T_{BLK} = 0°C to 90°C. Specifications outside of this temperature range are guaranteed by design, and not production tested.

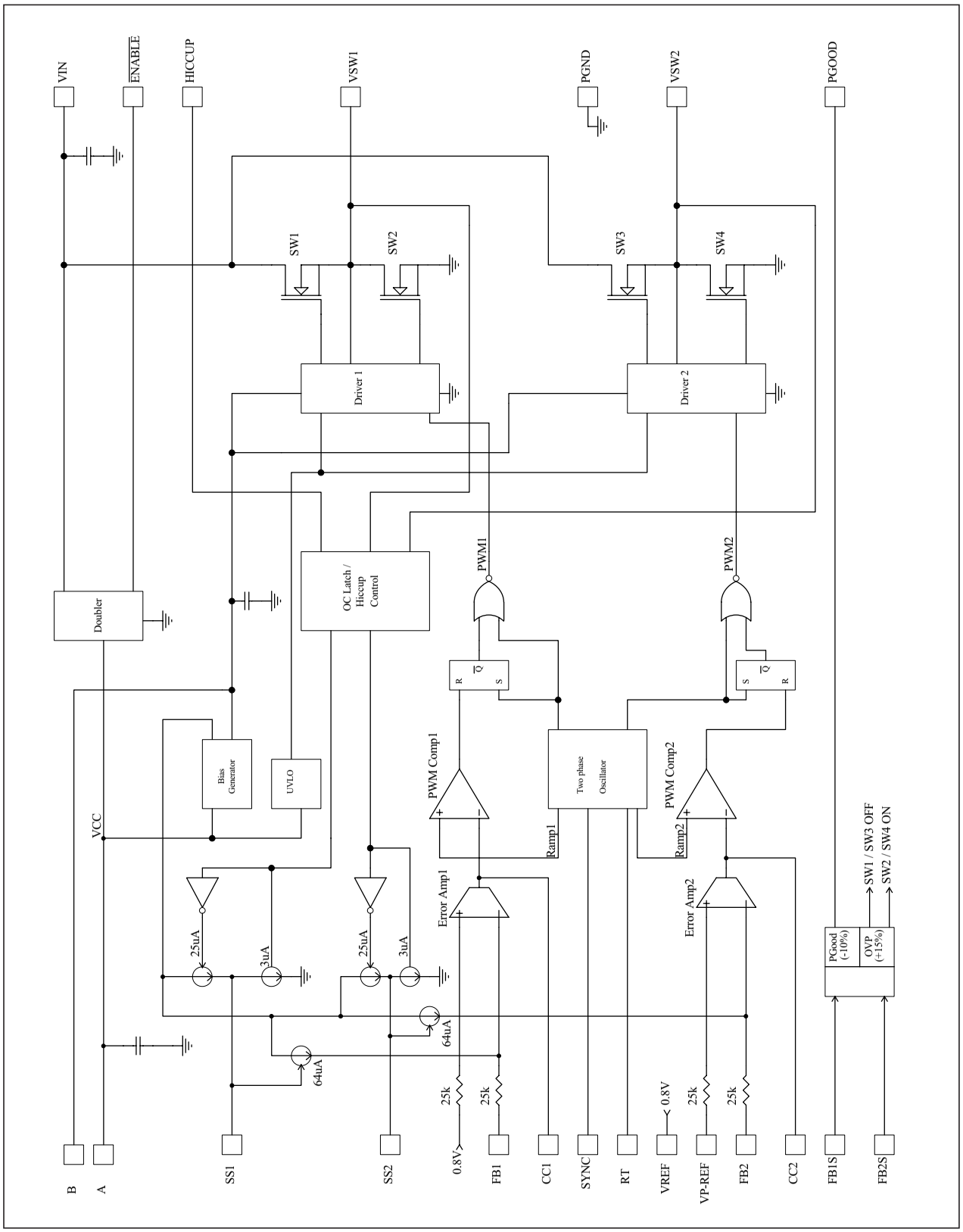


Fig. 1: iP1201PbF Internal Block Diagram

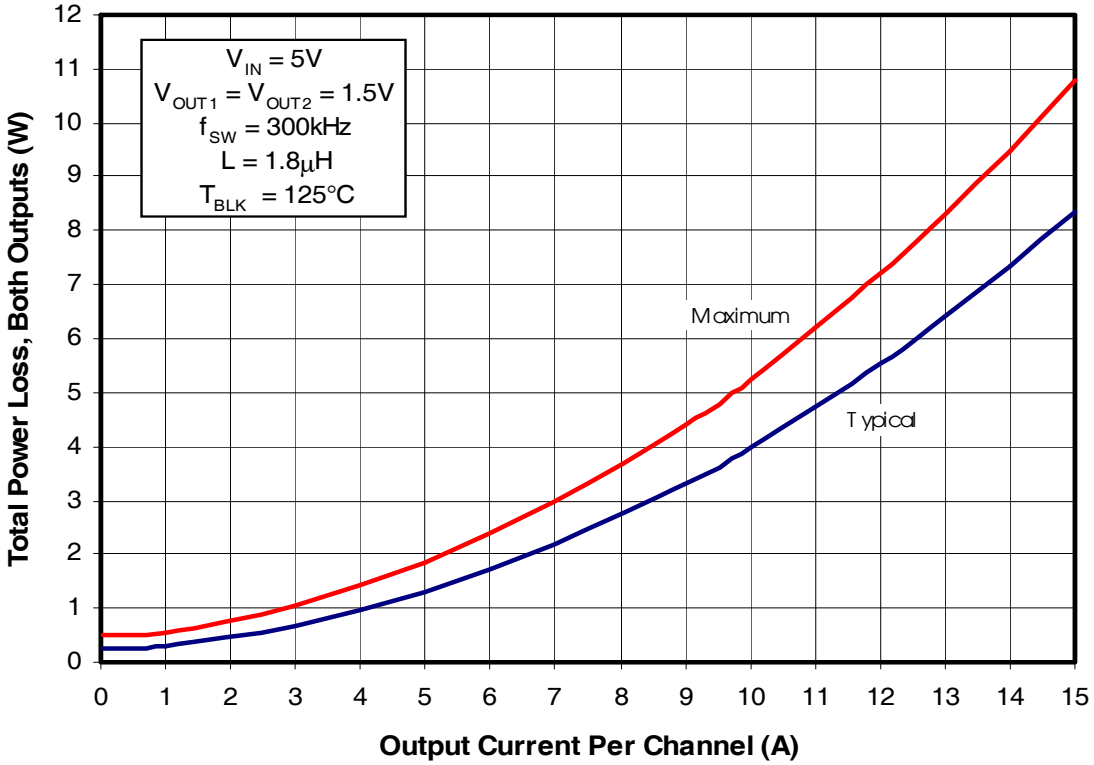


Fig. 2: Power Loss vs. Current

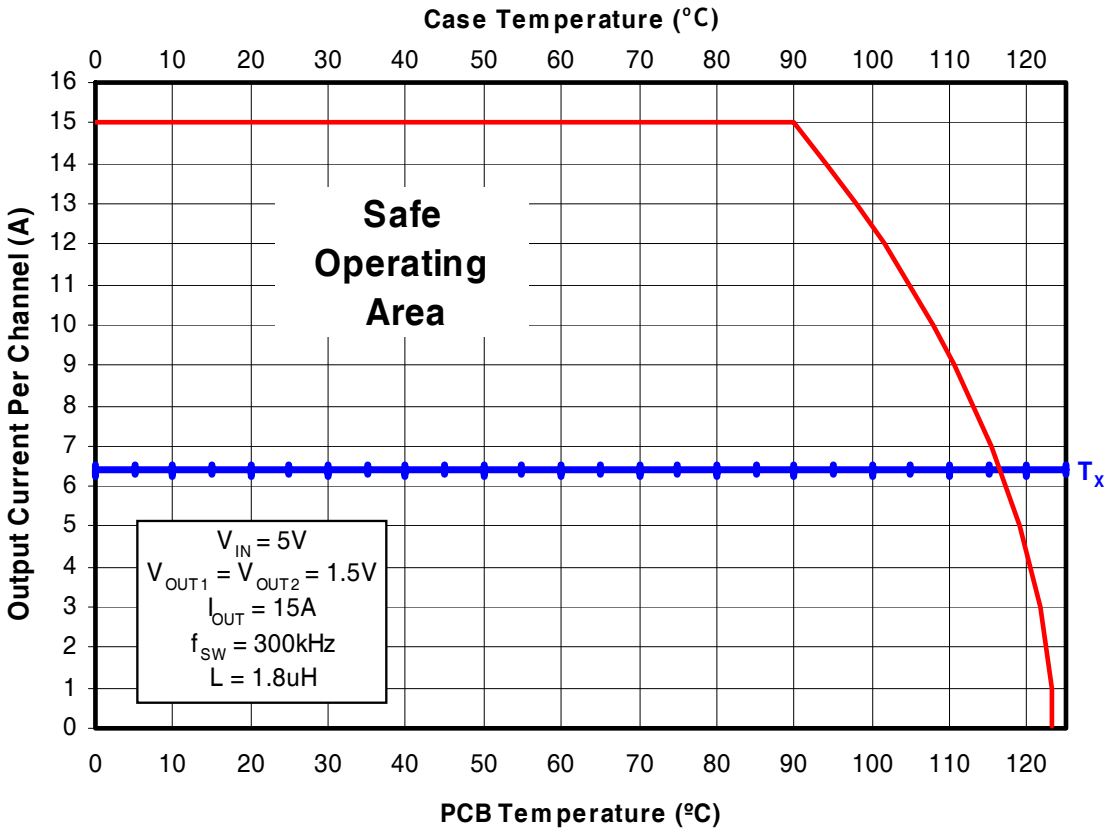


Fig. 3: Safe Operating Area (SOA) vs. T_{PCB} & T_{CASE}

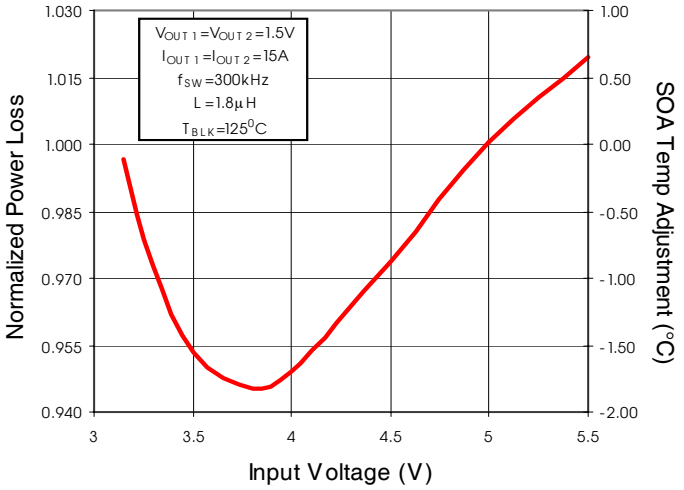


Fig. 4: Normalized Power Loss vs. V_{IN}

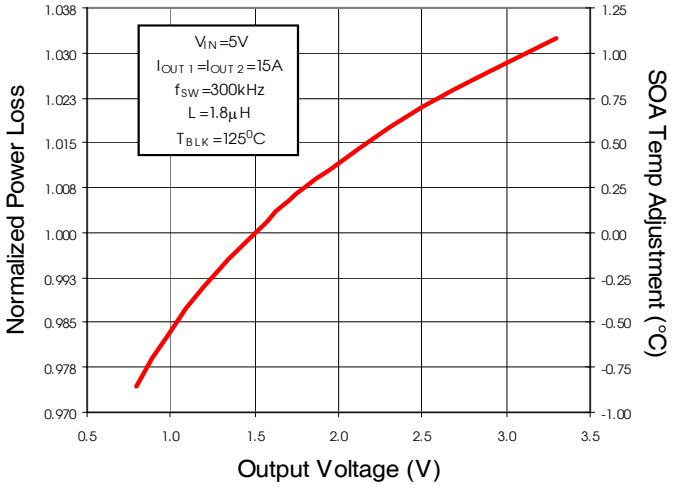


Fig. 5: Normalized Power Loss vs. V_{OUT}

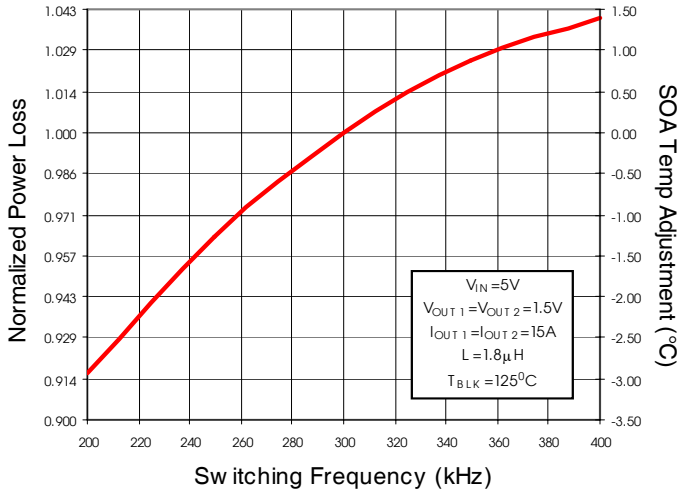


Fig. 6: Normalized Power Loss vs. Frequency

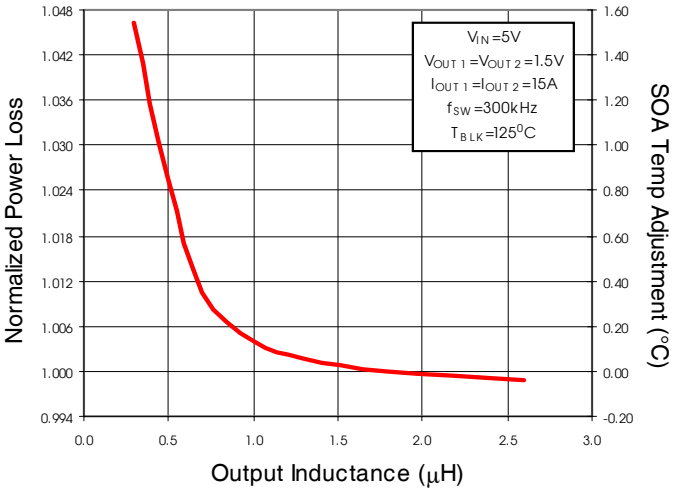


Fig. 7: Normalized Power Loss vs. Inductance

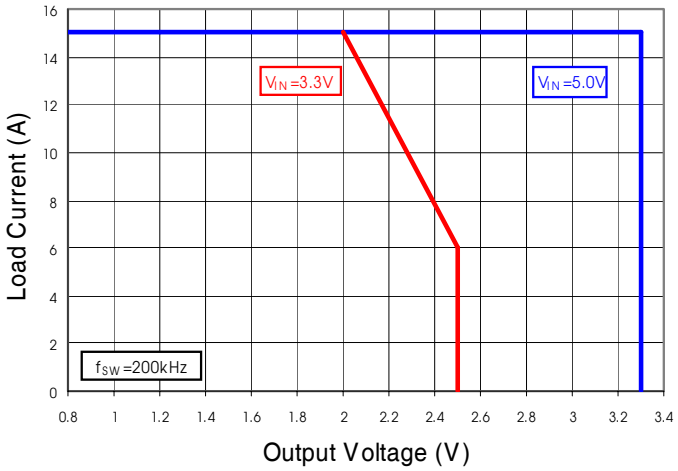


Fig. 8: Recommended Operating Area 200kHz

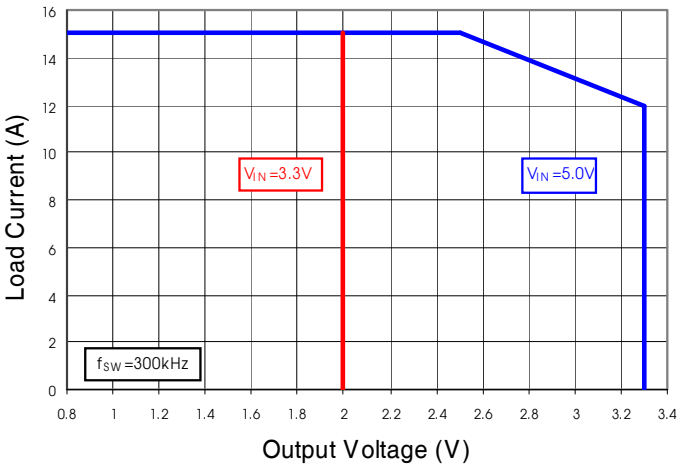


Fig. 9: Recommended Operating Area 300kHz

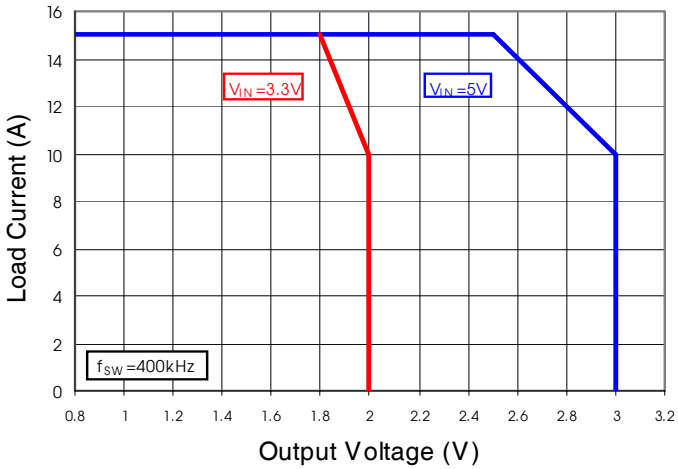


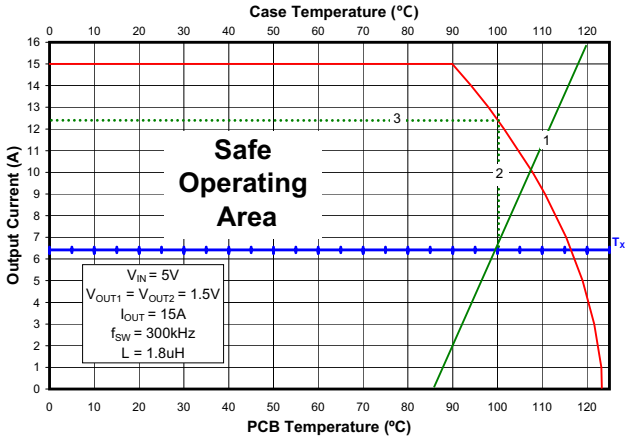
Fig. 10: Recommended Operating Area 400kHz

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case.

Procedure

1) Draw a line from Case Temp axis at T_{CASE} to the PCB Temp axis at T_{PCB}.
2) Draw a vertical line from the T_X axis intercept to the SOA curve. (see AN-1047 for further explanation of T_X)
3) Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y axis. The point at which the horizontal line meets the y-axis is the SOA current.
4) If no top sided heatsinking is available, assume T_{CASE} temperature of 125°C for worst case performance.



Adjusting the Power Loss and SOA curves for different operating conditions

To make adjustments to the power loss curves in Fig. 2, multiply the normalized value obtained from the curves in Figs. 4, 5, 6 or 7 by the value indicated on the power loss curve in Fig. 2. Remember that the power loss in Fig 2. is the power loss for 2 outputs operating with the same output voltage. If differing output voltages are used the initial power loss for each channel needs to be divided by 2. Then if multiple adjustments are required, multiply all of the normalized values together, then multiply that product by the value indicated on the power loss curve in Fig. 2. The resulting product is the final power loss based on all factors. See example no. 1.

To make adjustments to the SOA curve in Fig. 3, determine your maximum PCB Temp & Case Temp at the maximum operating current of each iP1201PbF. Then, add the correction temperature from the normalized curves in Figs. 4, 5, 6 or 7 to the T_X axis intercept (see procedure no. 2 above) in Fig. 3. When multiple adjustments are required, add all of the temperatures together, then add the sum to the T_X axis intercept in Fig. 3. See example no. 2.

Note: First check Fig. 8, Fig. 9 or Fig. 10 for maximum current capability

Operating Conditions for the following examples:

Output1

Output Current = 10A	Input Voltage = 3.3V	Inductor = 1.75µH
Output Voltage = 1.5V	Sw Freq= 200kHz	

Output2

Output Current = 13A	Input Voltage =3.3V	Inductor = 1.75µH
Output Voltage = 1.0V	Sw Freq= 200kHz	

Example 1) Adjusting for Maximum Power Loss:

Output1 (Fig. 2) Maximum power loss = 5.3W /2 = 2.65W
(Fig. 4) Normalized power loss for input voltage ≈ 0.97
(Fig. 5) Normalized power loss for output voltage ≈ 1.0
(Fig. 6) Normalized power loss for frequency ≈ 0.918
(Fig. 7) Normalized power loss for inductor value ≈ 1.0

Adjusted Power Loss = 2.65W x 0.97 x 1.0 x 0.918 x 1.0 ≈ 2.36W

Output2 (Fig. 2) Maximum power loss = 8.25W /2 = 4.13W
(Fig. 4) Normalized power loss for input voltage ≈ 0.97
(Fig. 5) Normalized power loss for output voltage ≈ 0.98
(Fig. 6) Normalized power loss for frequency ≈ 0.918
(Fig. 7) Normalized power loss for inductor value ≈ 1.0

Adjusted Power Loss = 4.13W x 0.97 x 0.98 x 0.918 x 1.0 ≈ 3.60W

Total device power loss = 2.36W + 3.60W = 5.96W

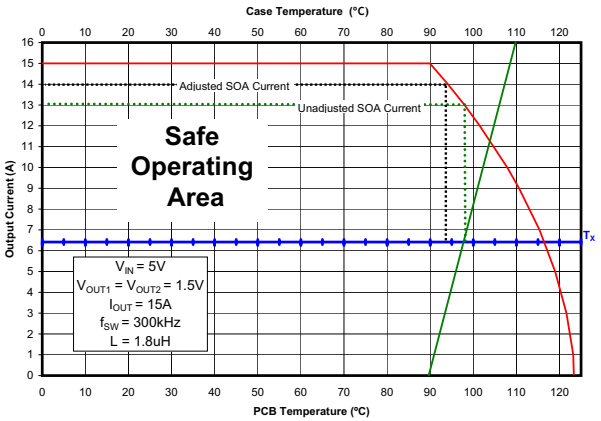
Example 2) Adjusting for SOA Temperature:

Assuming T_{CASE} = 110°C & T_{PCB} = 90°C for both outputs

Output1 (Fig. 4) Normalized SOA Temperature for input voltage ≈ -1.0°C
(Fig. 5) Normalized SOA Temperature for output voltage ≈ 0°C
(Fig. 6) Normalized SOA Temperature for frequency ≈ -2.9°C
(Fig. 7) Normalized SOA Temperature for inductor value ≈ 0°C

T_X axis intercept temp adjustment = -1.0°C + 0°C -2.9°C + 0°C ≈ -3.9°C

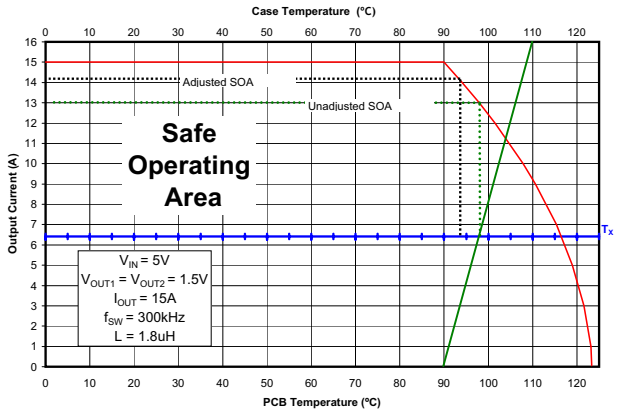
The following example shows how the SOA current is adjusted for a T_X change of -3.9°C and output 1 is **in SOA**



Output2 (Fig. 4) Normalized SOA Temperature for input voltage ≈ -1.0°C
(Fig. 5) Normalized SOA Temperature for output voltage ≈ -0.55°C
(Fig. 6) Normalized SOA Temperature for frequency ≈ -2.9°C
(Fig. 7) Normalized SOA Temperature for inductor value ≈ 0°C

T_X axis intercept temp adjustment = -1.0°C - 0.55°C - 2.9°C + 0°C ≈ -4.45°C

The following example shows how the SOA current is adjusted for a T_X change of -4.45°C and output 2 is **in SOA.**



Pin Name	Ball Designator	Pin Description
V_{IN}	A1 A2 A3 A4 A5 A14 A15 A16 A17 A18 B1 B2 B3 B4 B5 B14 B15 B16 B17 B18 C1 C2 C3 C4 C5 C14 C15 C16 C17 C18	Input voltage connection node
A*	G8 J13	Internally generated voltage. Connect to pin B when Vin < 3.5V. Leave floating for input voltages >3.5V. Externally, add a 2.2µF capacitor
B*	L12 L13	Internally generated voltage. Connect to pin A when Vin < 3.5V. Leave floating for input voltages >3.5V. Externally, add a 2.2µF capacitor
CC1	H8	Output of the first error amplifier, refer to Fig.1 block diagram
CC2	H13	Output of the second error amplifier
$\overline{\text{ENABLE}}$	A8 B8	Single pin for both outputs. Commands outputs ON or OFF. Pulled low, turns both outputs ON. Should be pulled high to disable outputs.
SS1	H6	Soft start pin for output1. External capacitor provides soft start. Pulled low disables output 1.
SS2	G11	Soft start pin for output2. External capacitor provides soft start. Pulled low disables output 2.
FB1	J6	Inverting input of error amplifier 1
FB1s	J8	Output 1 voltage sense pin
FB2	H11	Inverting input of error amplifier 2
FB2s	J11	Output 2 voltage sense pin
VSW1	D1 D2 D3 E1 E2 F1 F2 G1 G2 G3 H1 H2 H3 J1 J2 J3 K1 K2 L1 L2	Output 1 inductor connection node
VSW2	D16 D17 D18 E17 E18 F17 F18 G16 G17 G18 H16 H17 H18 J16 J17 J18 K17 K18 L17 L18	Output 2 inductor connection node
PGND	A6 A7 A9 A10 A12 A13 B6 B7 B9 B10 B12 B13 C6 C7 C9 C10 C12 C13 D6 D7 D9 D10 D12 D13 D14 E3 E4 E8 E11 E15 E16 F3 F4 F5 F6 F9 F10 F13 F14 F15 F16 G4 G5 G6 G9 G10 G13 G14 G15 H4 H5 H9 H10 H14 H15 J4 J5 J9 J10 J14 J15 K3 K16 L3 L5 L14 L16	Power Ground
Vref	L9	Amplifier 1 reference Voltage. Connect a 100pf cap from this pin to PGND.
VP-ref	L8	Amplifier 2 reference voltage. Connect to Vref for independent output configuration. Refer to function description section on how to connect for parallel configuration.
SYNC	K6	External Clock synchronization pin. Set free running frequency to 80% of the SYNC frequency. When not in use leave pin floating.
R_T	K13	Switching frequency setting pin. For R_T selection, refer to Fig.11 R_T vs Frequency curve.
PGOOD	L10	Power Good pin, needs external pull-up resistor. If not used pin can be left floating.
HICCUP	L6 L7	Logic level pin. Pulled high enables hiccup mode of operation. Pulled low enables overcurrent shutdown mode.
NC	L11	Unused pin. No electrical connection.

* Part will malfunction if pins A and B are shorted together for input voltages >3.5V

Table 1: Pin Description

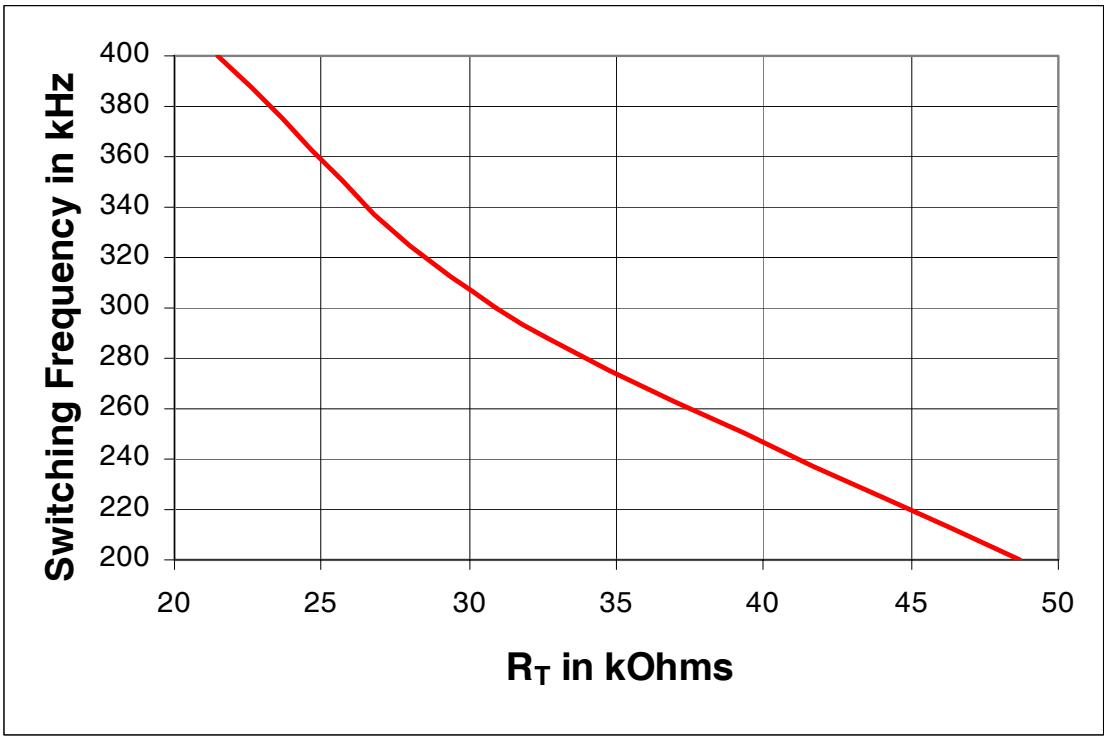


Fig. 11: Per Channel Switching Frequency vs R_T

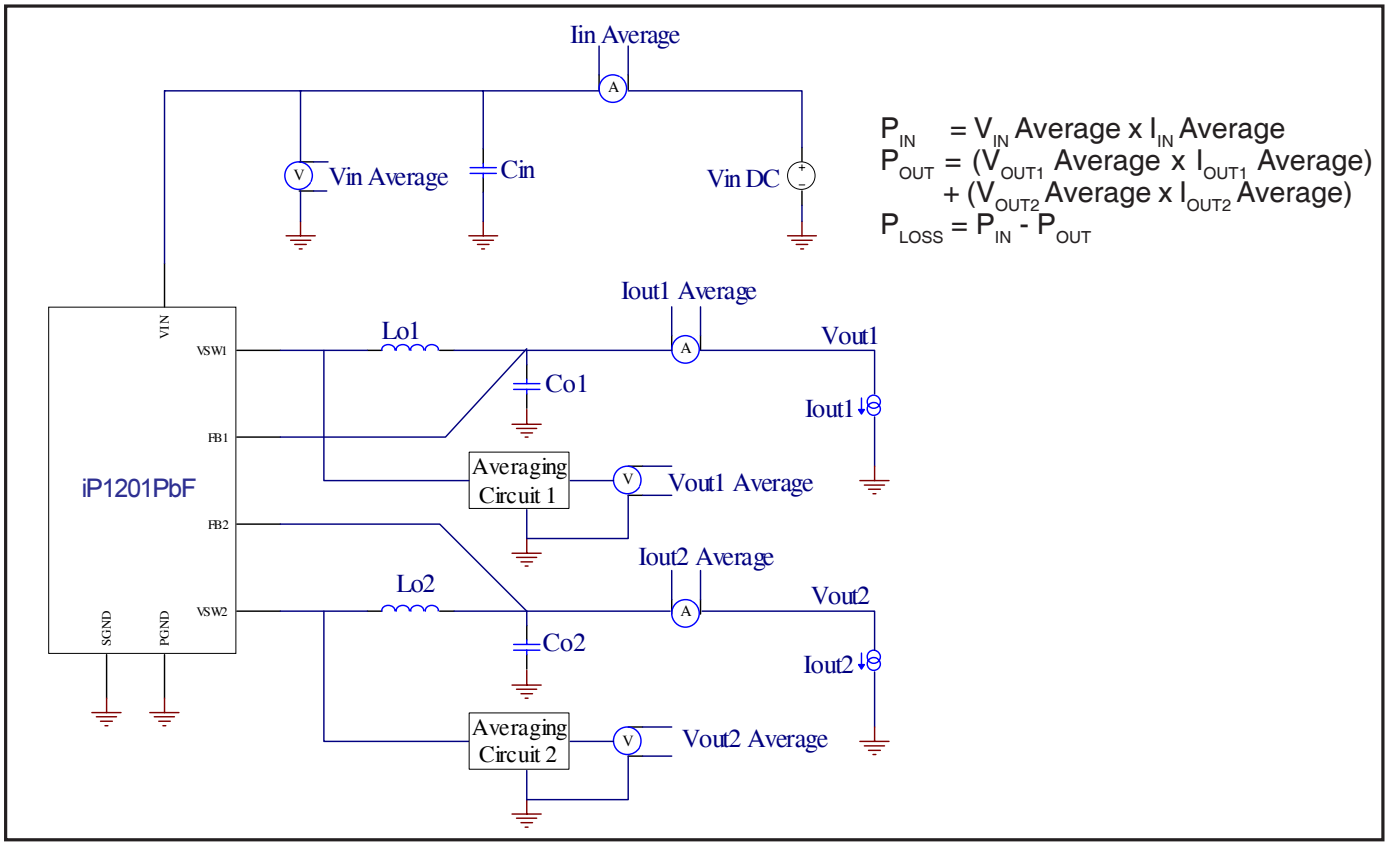
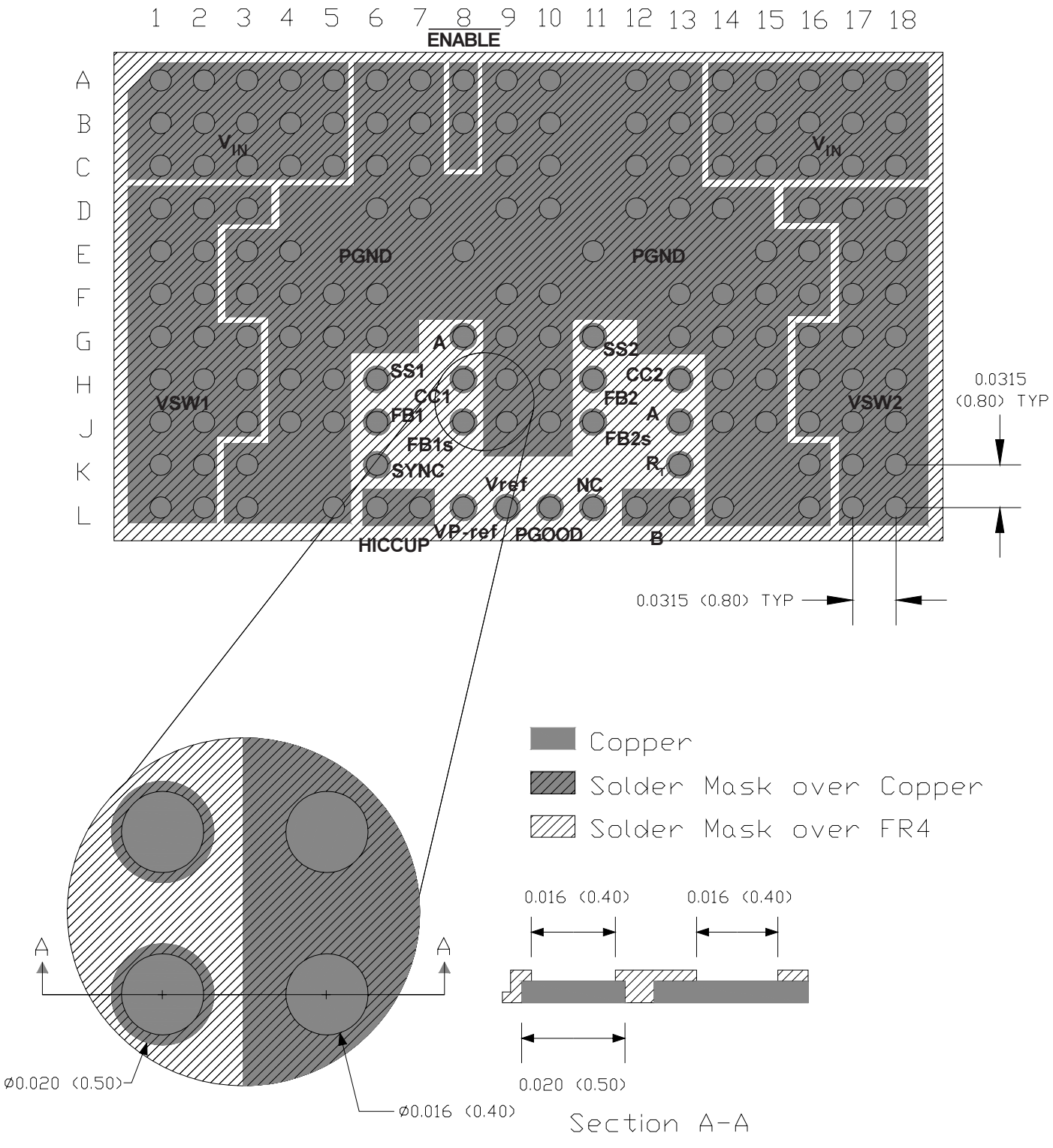


Fig. 12: Power Loss Test Circuit



All Dimensions in inches (millimeters)

Fig. 13: Recommended PCB Footprint (Top View)

iP1201PbF User's Design Guidelines

The iP1201PbF can be configured as a dual channel 15A or parallel single 30A power block consisting of optimized power semiconductors, PWM control and its associated passive components. It is based on a synchronous buck topology and offers an optimized solution where space, efficiency and noise caused by parasitics are of concern. The phase shifted, two output power block operates with fixed frequency voltage mode control and can be configured to operate as a dual output or paralleled single output with current sharing. The iP1201PbF components are integrated in a ball grid array (BGA) package.

V_{IN}

The input operating voltage range of the iP1201PbF is 3.14V to 5.5V. Both channels of the power block have a common input.

For applications where the input bus voltage is less than 3.5V, A and B pins should be shorted. For input voltages greater than 3.5V, A and B pins should be disconnected and floating. Voltages at A and B pins are internally generated, no external voltage source should be connected to either one of these pins. A Power-On-Reset is performed when V_{IN} falls below 2.5V.

Enabling the Outputs

The $\overline{\text{ENABLE}}$ pin turns on and turns off both outputs of the iP1201PbF simultaneously. The iP1201PbF outputs will be turned off by pulling the $\overline{\text{ENABLE}}$ pin to V_{IN}. $\overline{\text{ENABLE}}$ low will start the outputs. The converter can also be shutdown by pulling the soft-start pins to PGND through a logic level MOSFET the drain of which connects to the soft start pin (see Fig.14). This feature can be useful if sequencing or different start-up timing of the outputs are required. In situations where the output has undergone a latched shutdown due to overvoltage or overcurrent, cycling $\overline{\text{ENABLE}}$ will reset the outputs. Cycling soft start pins will not unlatch the outputs.

Dual Soft Start

The Soft Start function provides a controlled rise of the output voltage, thus limiting the inrush current during start-up. The iP1201PbF provides two independent soft start functions. The soft start pins can be connected to the soft start capacitors to provide different start-up and sequencing profiles.

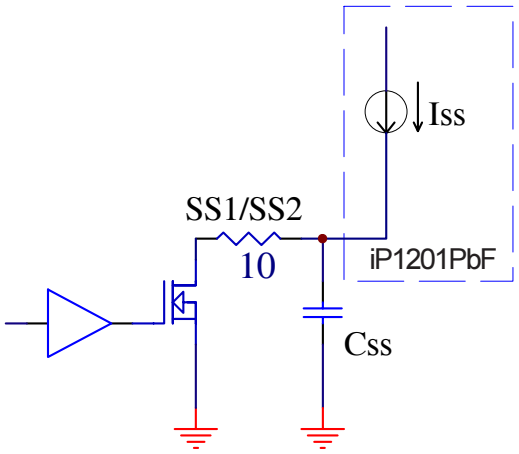


Fig. 14: Soft Start/Enable Circuit

Each soft start function has an internal 25uA +/-20% current source that charges the external soft start capacitor C_{ss} up to 3V. During power-up, the output voltage starts ramping up only after the charging voltage across the C_{ss} capacitor has reached a 0.8Vtyp threshold, as shown in Fig. 15.

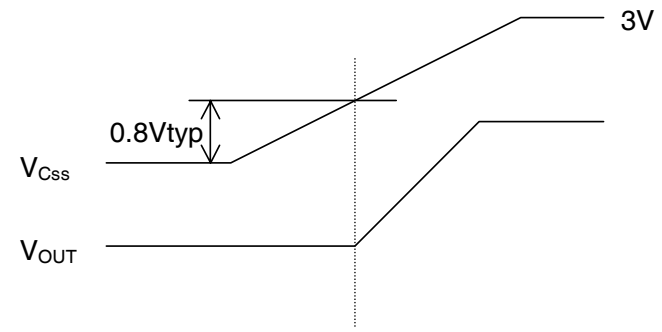


Fig. 15: Power Up Threshold

This threshold voltage should be taken into consideration when designing sequencing profiles using the iP1201PbF as it will effect start-up delays and ramp-times.
To ensure complete discharge of the soft start capacitor $C_{ss,}$ it is recommended to add a 1MΩ resistor directly across C_{ss}.

For proper implementation of sequencing of outputs using the iP1201PbF, refer to IR Application Note AN-1053 - Power sequencing techniques using iP1201 and iP1202.

Mode of Operation

The iP1201PbF can be configured to provide either two independent dual outputs or single paralleled output with current share. In dual output mode, the two error amplifiers of the PWM controller operate independently. Each output voltage of the iP1201PbF block is controlled by its own error amplifier. The output of the error amplifier and the internally generated ramp signal are compared to produce PWM pulses of fixed frequency that drive the internal power switches. In this mode, the VP-ref pin must be connected to Vref pin. Vref pin is the internally generated 0.8V reference input of first error amplifier . Refer to the internal block diagram of the iP1201PbF in Fig.1.

In single output mode, one error amplifier controls the output voltage and the other amplifier monitors the inductor current information for current sharing. In this mode, VP-ref pin must be disconnected from Vref pin and connected to the output of the inductor. See Fig. 17. The inductor current information is provided through external shunts placed in series with the output inductors.
A lossless inductor current sensing scheme can also be implemented as shown in Fig. 18 where the current is sensed throughthe DC resistance of the inductor. In this case R_L and C_L are selected such that $R_L x C_L = L / R_{dc}$. Set R_L = 1K and solve for C_L. R_{dc} is the internal DC resistance of inductor L.
In single output mode, the iP1202 does not require a soft start capacitor at SS2 pin.

The iP1201PbF can also be configured in dual output tracking mode where the second output tracks the first output.

For a specific output configuration, follow the connection diagram shown in Fig.16, Fig.17 and Fig.18 at the end of this section.

Out of Phase Operation

The dual output PWM controller inside the iP1201PbF provides a 180° out of phase operation of the PWM outputs. This method of control offers the advantage of reducing the amount of input bypass capacitors due to increase in input ripple frequency and hence reduction of ripple amplitude. Moreover, for paralleled output configurations 180° phase shifting contributes to smaller output capacitors due to output inductor ripple current cancellation and ripple reduction.

Frequency and Synchronization

The operating switching frequency (f_{SW}) range of iP1201PbF is 200 kHz to 400 kHz. The desired frequency is set by placing an external resistor to the R_T pin of the iP1201PbF. See Fig. 11 for the proper resistor value.
The iP1201PbF is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge clock. The free running oscillator frequency is twice the per-channel frequency. During synchronization, R_T is selected such that the free running frequency is 20% below the synchronization frequency. The maximum synchronization frequency that iP1201PbF can accept is 800kHz. Note that the actual free running frequency of individual output is half the synchronization frequency. Synchronization capability is provided both in independent and parallel configurations. When unused, the SYNC pin must be left floating.

Overcurrent Protection/Autorestart

The Overcurrent Protection function of the iP1201PbF offers two distinct modes: HICCUP of the output and Overcurrent Shutdown. If the Hiccup pin is pulled high (Hiccup enabled), hiccup mode will be selected. If Hiccup pin is pulled low (Hiccup dis- abled), overcurrent shutdown will be selected.

During overloads, in HICCUP disabled mode, the controller shuts down as soon as the trip threshold is reached. In HICCUP enabled mode, when overcurrent trip threshold is reached, the power supply output shuts down and attempts to restart. The time duration between the shutdown of the output and the restart is determined by the time it takes to discharge the soft start capacitor. Typically, the discharge time of the soft start capacitor is 10 times the charge time. The duty cycle of the hiccup process is typically 5%.The output will stay in hiccup indefinitely until the overload is removed. The typical overcurrent trip threshold of the device is internally set at 20A.

Overvoltage Protection (OVP)

Overvoltage is sensed through separate output voltage sense pins FB1s and FB2s. A separate OVP circuit is provided for each output and the OVP threshold is set to 115% of the output voltage. Upon overvoltage condition of either one of the outputs, the OVP forces a latched shutdown on both outputs.

In this mode, the upper FETs turn off and the lower FETs turn on, thus crowbaring the outputs. Reset is performed by recycling the ENABLE pin.

Overvoltage can be sensed by either connecting FB1s and FB2s to their corresponding outputs through separate output voltage divider resistor networks, or they can be connected directly to their corrsponding feedback pins FB1 and FB2. For Type III control loop compensation, FB1s and FB2s should be connected through separate voltage dividers only.

PGOOD

This is an output voltage status signal that is open collector and is pulled low when the output voltage falls below 85% of the outout voltage. High state indicates that outputs are in regulation. There is only one PGOOD for both outputs. The PGOOD pin can be left floating if not used.

Thermal Shutdown

The iP1201PbF provides thermal shutdown. The threshold typically is set to 140°C. When the trip threshold is exceeded, thermal shutdown turns the outputs off. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to the normal range.

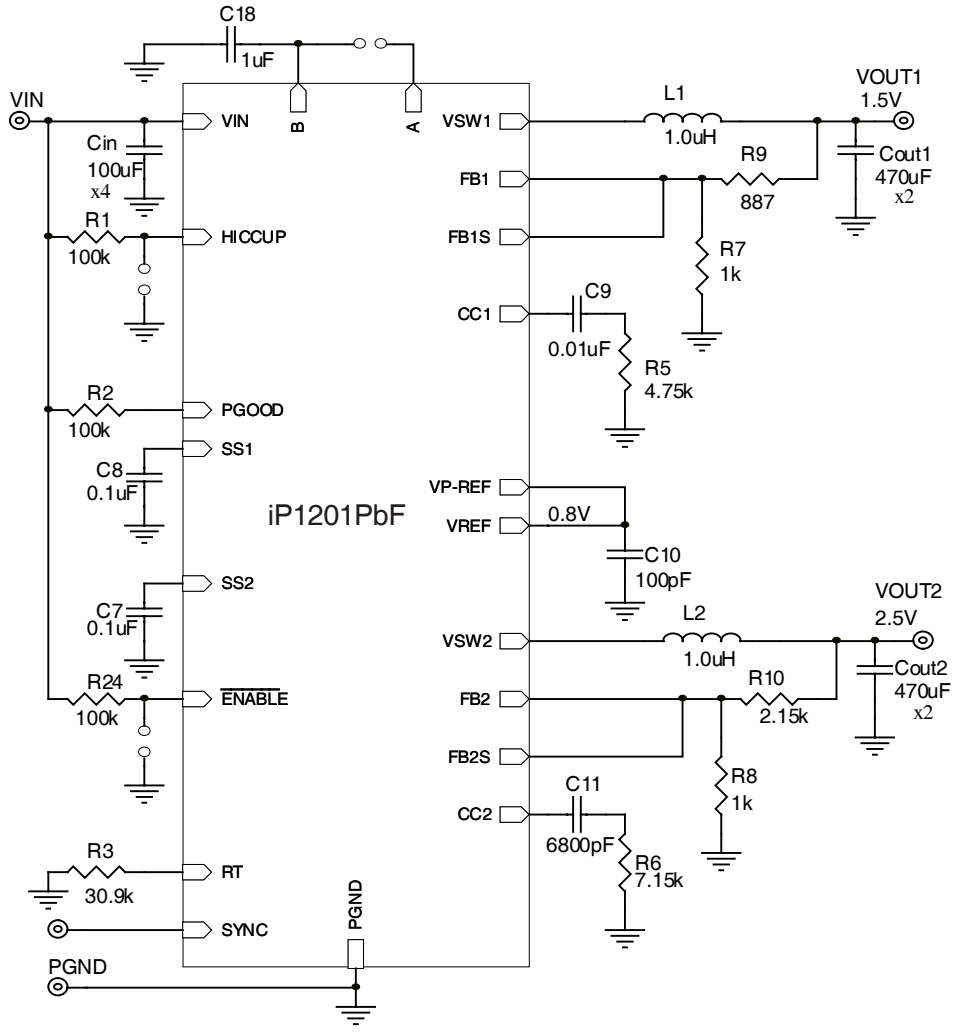


Fig. 16: iP1201PbF Dual Output Simplified Schematic

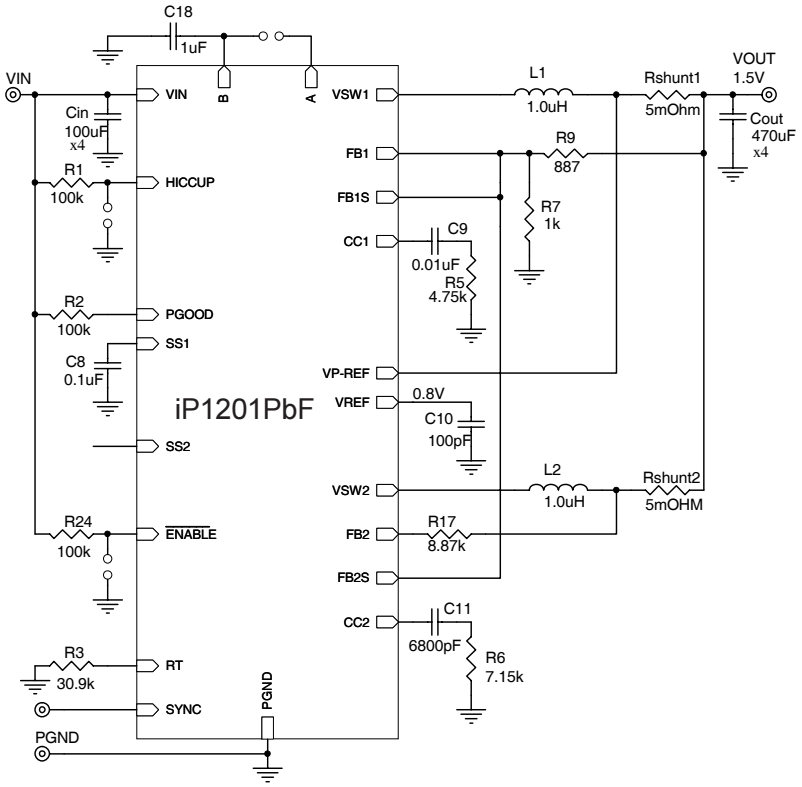


Fig. 17: iP1201PbF Single Output Simplified Schematic

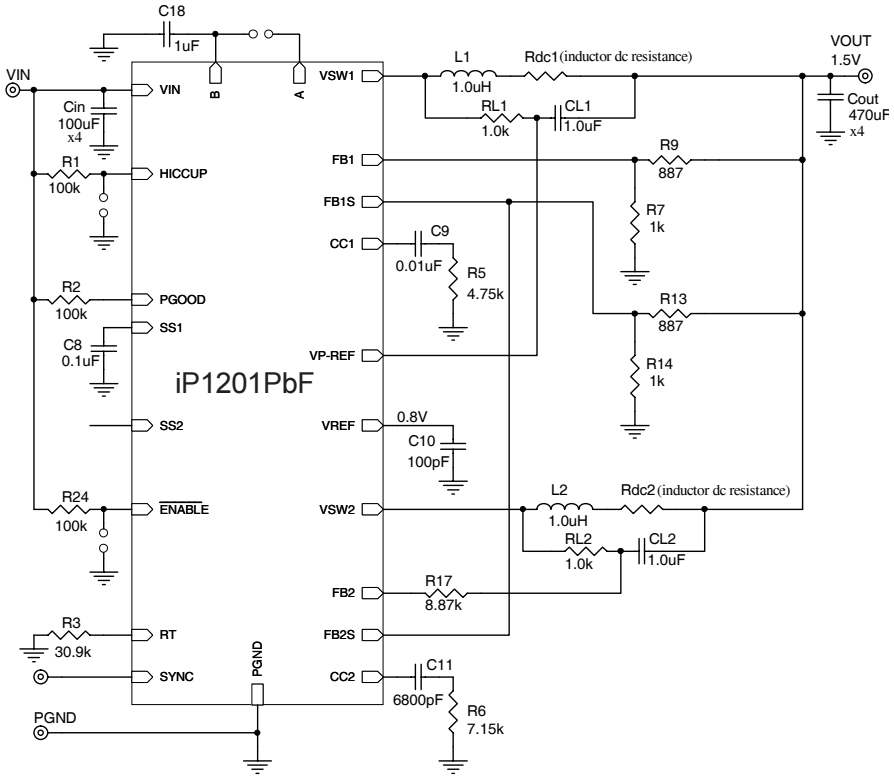


Fig. 18: iP1201PbF Single Output Lossless Inductor Current Sensing Simplified Schematic

iP1201PbF Design Procedure

Only a few external components are required to complete a dual output synchronous buck power supply using iP1201PbF. The following procedure will guide the designer through the design and selection process of these external components.

A typical application for iP1201PbF. will be:
V_{IN} = 3.3V, V_{OUT1} = 1.5V, I_{OUT1} = 10A, V_{OUT2} = 2.5V, I_{OUT2} = 6A, f_{sw} = 200kHz, V_{p-p1} = V_{p-p2} = 40mV

Setting the Output Voltage

The output voltage of the iP1201PbF. is set by the 0.8V reference Vref and external voltage dividers.

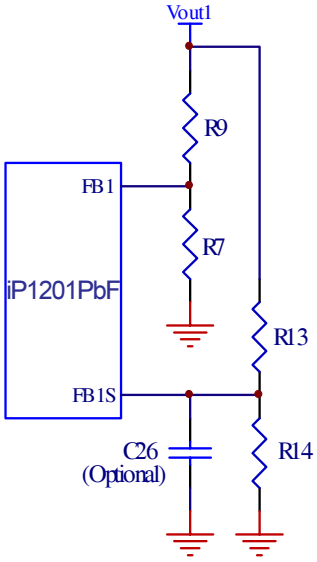


Fig. 19: Typical scheme for output voltage setting

V_{OUT1} is set according to equation (1):

$$V_{OUT1} = V_{ref} \times (1 + R_9/R_7) \text{ (see Fig. 19)} \qquad (1)$$

Setting R_7 to 1K, V_{OUT1} to 1.5V and Vref to 0.8V, will result in R_9= 875 ohms (select 887 ohms). Final values can be selected according to the desired accuracy of the output.

If the 0.8V reference is used to set the voltage for the second output V_{OUT2}, VP-ref pin must be shorted to Vref pin and in a similar way, voltage divider resistors are selected for the second output V_{OUT2}. The second output can also be set by applying an external reference source to VP-ref. In this case, to ensure proper start-up, power to VP-ref and iP1201PbF. must be applied simultaneuosly.

Setting the Overvoltage Trip

Both outputs of the iP1201PbF. will shut down if either one of the outputs experiences a voltage in the range of 115% of V_{OUT}. The overvoltage sense pins FB1s and FB2s are connected to the output through voltage dividers, R_{13} and R_{14} (Fig. 19), and the trip setpoints are programmed according to equation (1). Separate overvoltage sense pins $FB1_s$ and $FB2_s$ are provided to protect the power supply output if for some reason the main feedback loop is lost (for instance, loss of feedback resistors). If this redundancy is not required and if Type II control loop compensation scheme is utilized, FB1s and FB2s pins can be connected to FB1 and FB2 pins respectively. An optional 100pF capacitor (C26) is used for delay and filtering purposes.
In parallel configuration, FB2s should be connected to FB1s

Setting the Soft-Start Capacitor

The soft start capacitor C_{ss} is selected according to equation (2):

$$t_{ss} = 40 \times C_{ss} \qquad (2)$$

where,
t_{ss} is the output voltage ramp time in milliseconds, and C_{ss} is the soft start capacitor in µF.

A 0.1µF capacitor will provide an output voltage ramp-up time of about 4ms.

Input Capacitor Selection

The switching currents impose RMS current requirements on the input capacitors. The expression in equation (3) allows the selection of the input capacitors:

$$I_{RMS} = I_{LOAD} \times \sqrt{D(1-D)} \qquad (3)$$

where,
D is the duty cycle and is expressed as:

$D = V_{OUT} / V_{IN}$.

For output1 of the above example D= 0.45 and,
I_{RMS} = 10 x SQRT (0.45(1-0.45)) = 5A
For output2 of the above example D = 0.75 and,

I_{RMS} = 6 x SQRT (0.75(1 - 0.75)) = 2.6A

For better efficiency and low input ripple, select low ESR ceramic capacitors. The amount of the capacitors is determined based on the r.m.s. rating. In the above example, a total of 3 x 100µF, 3.5A capacitors will be required to support the input r.m.s. current (see the parts list in the reference design section of this datasheet).

The 180° out of phase operation of the iP1201PbF provides reduced voltage ripple at the input of the device. This reduction in ripple requires less input bypass capacitance. Therefore the input bypass capacitor selection criteria based on equation (3) provides a worst case solution for the selected operating conditions.

Output Capacitor C_o Selection

Selection of the output capacitors depends on two factors:
a. Low effective ESR for ripple and load transient requirements

To support the load transients and to stay within a specified voltage dip ΔV due to the transients, e.s.r. selection should satisfy equation (4):

$$R_{esr} \leq \Delta V / I_{Loadmax} \quad (4)$$

Where,
$I_{Loadmax}$ is the maximum load current.

If output voltage ripple is required to be maintained at specified levels then, the expression in equation (5) should be used to select the output capacitors.

$$R_{esr} \leq V_{p-p} / I_{ripple} \quad (5)$$

Where,
V_{p-p} is the single phase peak to peak output voltage ripple.
I_{ripple} is the inductor current peak-to peak ripple.

If the inductor current ripple I_{ripple} is 30% of $I_{OUT1,}$ the 40mV peak to peak output voltage ripple requirement will be met if the total e.s.r. of the output capacitors is less than 11mohms. This will require 3 x 470µF POSCAP capacitors (See the parts list in the reference design section of this datasheet). Additional ceramic capacitors can be added in parallel to further reduce the e.s.r. Care should be given to properly compensate the control loop for low output capacitor e.s.r. values.

When selecting output capacitors, it is important to consider the overshoot performance of the power supply. If the amount of capacitance is not adequate, then, when unloading the output, the magnitude of the overshoot due to stored inductor energy, and depending on the speed of the response of the control loop, can exceed the overvoltage trip threshold of the iP1201PbF and can cause undesirable shutdown of the output. The magnitude of the overshoot should be kept below $1.125V_{OUT}$. To prevent the overshoot from tripping the output a delay can be added by installing capacitor C26 as shown in Fig.19.

In paralleled single output configuration, due to 180° phase shift, the peak to peak output voltage ripple will be reduced because of doubling of the ripple frequency. Also, the resulting ripple current in the output capacitors will be smaller than the ripple current of each channel. There is some cancellation effect of these current, the magnitude of which depends on the duty cycle.

b. Stability

The value of the output capacitor e.s.r. zero frequency f_{esr} plays a major role in determining stability. f_{esr} is calculated by the expression in equation (6).

$$f_{esr} = 1 / (2 \pi \times R_{esr} \times C_O) \quad (6)$$

Details on how to consider this parameter to design for stability will be outlined in the control loop compensation section of this datasheet.

Inductor L_o Selection

Inductor selection is based on trade-offs between size and efficiency. Low inductor values result in smaller sizes, but can cause large ripple currents and lower efficiency. Low inductor values also benefit the transient performance.
The inductor L_o is selected according to equation (7):

$$L_O = V_{out} \times (1 - D) / (f_{sw} \times I_{ripple}) \quad (7)$$

For output 1 of the above example, and for I_{ripple} of 30% of I_{OUT1}, L_{O1} is calculated to be 1.1µH.
The core must be selected according to the peak of maximum output current.
A similar calculation can be applied to find an induc-

tor value for the second output.

Control Loop Compensation

The iP1201PbF feedback control is based on single loop voltage mode control principle if both outputs are configured in dual output independent mode. In this case, both outputs can have identical compensation. If iP1201PbF outputs are configured for parallel operation, then compensation of the outputs will differ slightly.

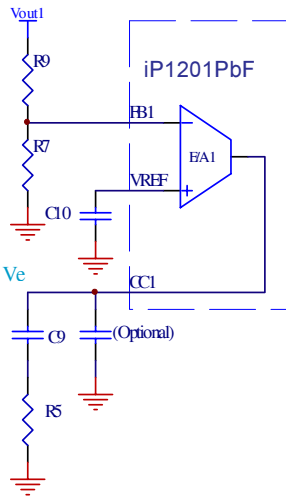
The goal in the design of the compensator is to achieve the highest unity gain (0 db) crossover frequency with sufficient phase margin for the closed loop transfer function. The LC filter of the power supply introduces a double pole with –40db/dec slope and 180^0 phase lag. The 180° phase contribution from the LC filter is the source of instabilty.
The resonant frequency of the LC filter is expressed by equation (8):

$$f_{LC} = 1/(2\pi\sqrt{L_0 \times C_0}) \qquad (8)$$

The error amplifiers of the iP1201PbF PWM controller are transconductance amplifiers, and their outputs are available for external compensation.

Two type of compensators are studied in this section. The first one is called Type II and it is used to compensate systems the e.s.r. frequency f_{esr} (equation 6) of which is in the midfrequency range and Type III that can be used for any type of output capacitors and have a wide range of f_{esr}.

Type II



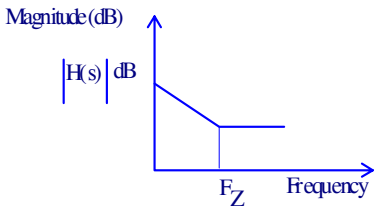


Fig. 20: Typical Type II compensation and its gain plot

From Fig.19 the transfer function H(s) of the error amplifier is given by (9):

$$H(s) = g_m \times \frac{R_7}{R_7 + R_9} \times \frac{1 + sR_5C_9}{sC_9R_5} \qquad (9)$$

The term *s* represents the frequency dependence of the transfer function.

The Type II controller introduces a gain and a zero expressed by equations (10) and (11):

$$|H(s)| = g_m \times \frac{R_7}{R_7 + R_9} \times R_5 \qquad (10)$$

where, g_m is the transconductance of the error amplifier.

$$f_z = \frac{1}{2\pi \times R_5 \times C_9} \qquad (11)$$

Follow the steps below to determine the feedback loop compensation component values:

1. Select a zero db crossover frequency f_0 in the range of 10% to 20% of the switching frequency $f_{sw.}$

2. Calculate R_5 using equation (12):

$$R_5 = V_{ramp} \times \frac{1}{V_{IN}} \times \frac{f_0 \times f_{esr}}{f_{LC}^2} \times \frac{R_7 + R_9}{R_7} \times \frac{1}{g_m} \qquad (12)$$

Where,
V_{IN} = Maximum Input voltage
f_0 = Error amplifier zero crossover frequency
f_{esr} = Output capacitor C_o zero frequency
f_{LC} = Output frequency resonant filter
g_m = Error amplifier transconductance. Use 2000μmho for g_m.
V_{ramp} = Oscillator ramp Voltage.
Use 1.25V for V_{ramp}

3. Place a zero at 75% of f_{LC} to cancel one of the LC filter poles.

$$f_z = 0.75 \times \frac{1}{2\pi\sqrt{L_o \times C_o}} \qquad (13)$$

4. Calculate C_9 using equations (11) and (13)

Calculation of compensation components for output1, based on the example above yields:

f_{LC} = 4.0kHz
f_z = 3.0kHz
f_0 = 20kHz (based on F_{sw} = 200kHz)
f_{esr} = 10kHz, per equation (7) using R_{esr} = 11mΩ.
R_5 = 4.5K
C_9 = 12nF

The same steps can be used to determine the values of the compensation components for output2.

Sometimes, a pole f_{p2} is added at half the switching frequency to filter the switching noise. This is done by adding a capacitor C_{opt} in Fig.20 from the output of the error amplifier (CC pin of iP1201PbF) to ground. This pole is given by equation (14):

$$f_{p2} \approx \frac{1}{2\pi \times R_5 \times C_{opt}} \qquad (14)$$

C_{opt} is found from equation (15) by rearranging the terms in equation (14) and by setting $f_{p2} = f_{sw}/2$:

$$C_{opt} = \frac{1}{2\pi \times f_{p2} \times R_5} \qquad (15)$$

Type III

Type III compensation scheme allows the use of any type of capacitors with esr frequency of any range. This scheme suggests a double pole double zero compensation and requires more components around the error amplifier to achieve the desired gain and phase margins. Fig. 21 represents the type III compensation network for iP1201PbF.

The transfer function of the type III compensator is given by eqaution (16)

$$H(s) \approx \frac{1}{sR_9C_9} \times \frac{(1+sR_{26}C_9)\times(1+sR_9C_{21})}{(1+sR_{26}C_{22})\times(1+sR_{25}C_{21})} \qquad (16)$$

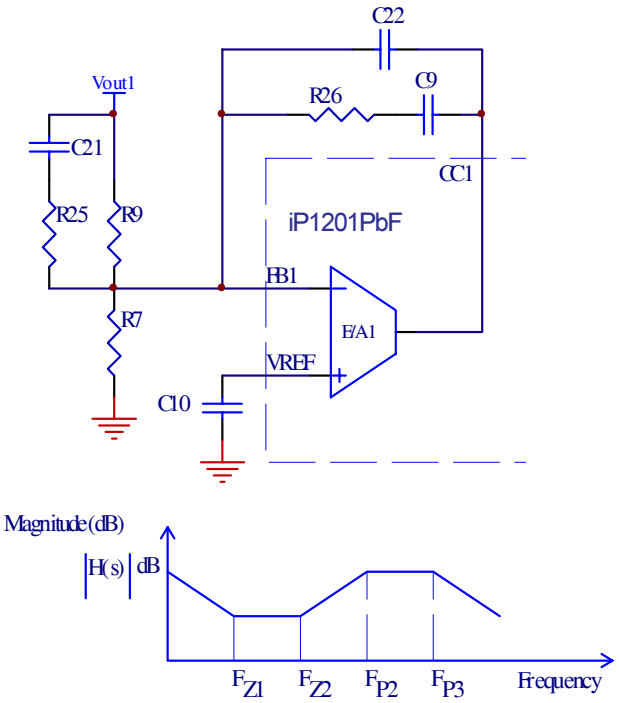


Fig. 21: Typical Type III compensation and its gain plot

The frequencies of the three poles and the two zeros of the type III compensation scheme are represented by the following equations:

$$f_{p1} = 0 \qquad (17)$$

$$f_z = \frac{1}{2\pi \times R_{25} \times C_{21}} \qquad (18)$$

$$f_{p3} \cong \frac{1}{2\pi \times R_{26} \times C_{22}} \qquad (19)$$

$$f_{z1} = \frac{1}{2\pi \times R_{26} \times C_9} \qquad (20)$$

$$f_{z2} = \frac{1}{2\pi \times R_9 \times C_{21}} \qquad (21)$$

The crossover frequency f_0 for type III compensation is represented by equation (22):

$$f_0 = \frac{1}{V_{ramp}} \times V_{IN} \times R_{26} \times C_{21} \times \frac{1}{2\pi \times L_0 \times C_0} \qquad (22)$$

Follow the steps below to determine the feedback loop compensation component values:

1. Select a zero db crossover frequency f_0 in the range of 10% to 20% of the switching frequency f_{sw}.

2. Select R_{26} = ~10kΩ

3. Place the first zero f_{z1} at 75% of the resonant frequency f_{LC} of the output filter.
Determine C_9 from equation (20).

4. Place a third pole f_{P3} at or near the switching frequency f_{SW}.

Select C22 such that $C_{22} << \frac{C_9}{10}$

5. Calculate C_{21} from equation (22).

6. Place the second zero at 125% of the resonant frequency f_{LC} of the output filter. Calculate R_9 using equation (21).

7. Place the second pole f_{p2} at or near f_{esr} of the output capacitor C_o and determine the value of R_{25} from equation (18). Make sure $R_{25} < \frac{R_9}{10}$

8. Use equation (23) to calculate R_7.

$$R_7 = R_9 \times \frac{V_{ref}}{V_0 - V_{ref}} \qquad (23)$$

More than one iteration may be required to calculate the values of the compensation components if crossover frequencies higher than the range specified in step 1 are required (for higher bandwidths and faster transient response performance). To ensure stability a phase margin greater than 45° should be achieved.
Refer to AN-1043 for more detailed compensation techniques using Transconductance Amplifiers.

Compensation in Current Share Mode

The iP1201PbF can be configured in single output paralleled configuration. The feedback loop of the first output is closed around the output voltage, and the second amplifier, which is also a transconductance one, forces equal sharing of the inductor currents in both outputs.

Voltage Loop

Type II and Type III methods of voltage loop compensation discussed above, can be used to compensate the voltage loop of a single output iP1201PbF. In this case the total amount of capacitance seen by both channels and the inductance of the voltage controlling channel should be considered for compensation.

Current Loop

Use the following procedure for current loop compensation:

In Fig. 22, L_1 and L_2 are the inductors for outputs 1 and 2 respectively. Rsh1 and Rsh2 are the current sensing shunts for the same outputs.

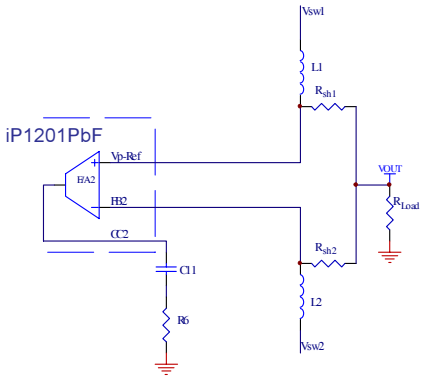


Fig. 22: Output 2 error amplifier compensation network for parallel configuration.

Resistor R_6 of the compensation network is calculated according to equation (24)

$$R_6 = V_{ramp} \times \frac{1}{g_m \times R_{sh1}} \times \frac{2\pi \times L_2 \times f_{02}}{V_{in}} \qquad (24)$$

The power stage of the current loop has a dominant pole at frequency expressed by equation (25):

$$f_p = \frac{R_{eq}}{2 \cdot \pi \cdot L_2} \qquad (25)$$

where, R_{eq} represents the total resistance of the power stage that includes the Rdson of the FET switches, the DC resistance of the inductor and the shunt resistance, and is expressed by equation (26):

$$R_{eq} = R_{dson} + R_L + R_{sh} \qquad (26)$$

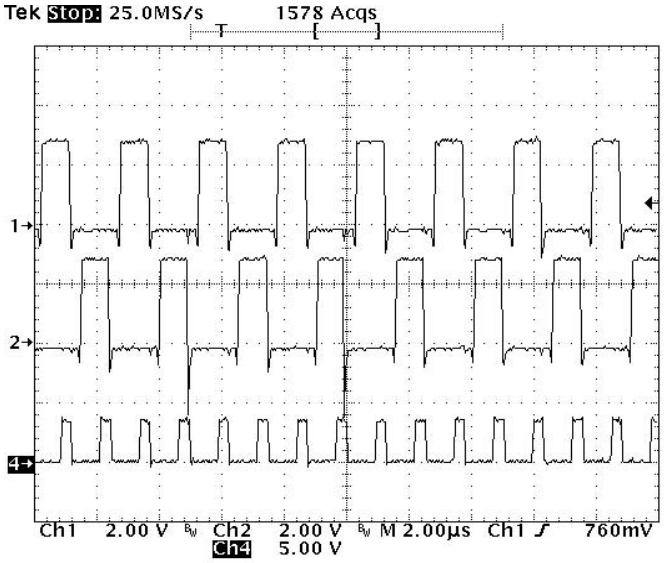
use 10mohm for FET Rdson.
To calculate for C11, place the zero frequency f_z at 10 times the dominant pole frequency f_p using equation (27):

$$f_z = 10 \times f_p$$

$$C_{11} = \frac{1}{2\pi \times R_6 \times f_z} \qquad (27)$$

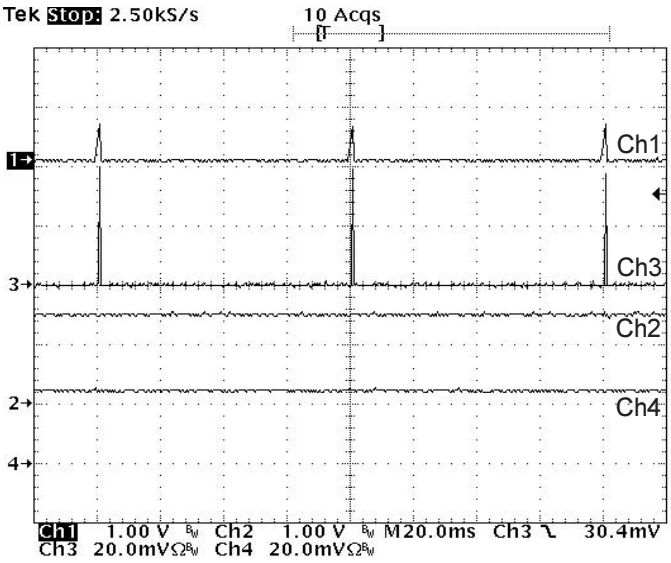
Select $C_{11} \le 6.8nf$

Typical Waveforms



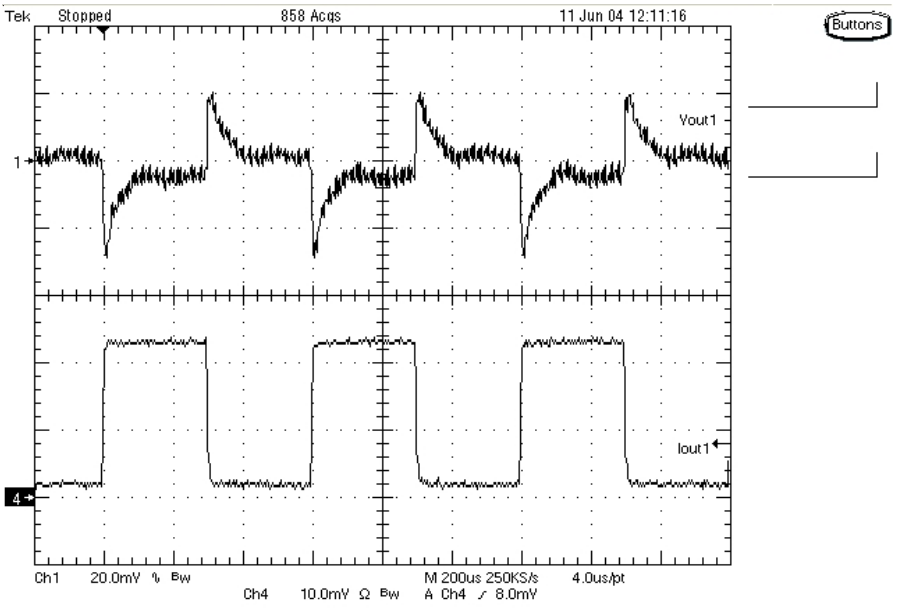
Ch1: Output 1 switching node, 400kHz
Ch2: Output 2 switching node, 400kHz
Ch4: 800kHz external synchronization

Fig. 23: iP1201PbF Outputs synchronized to 800kHz



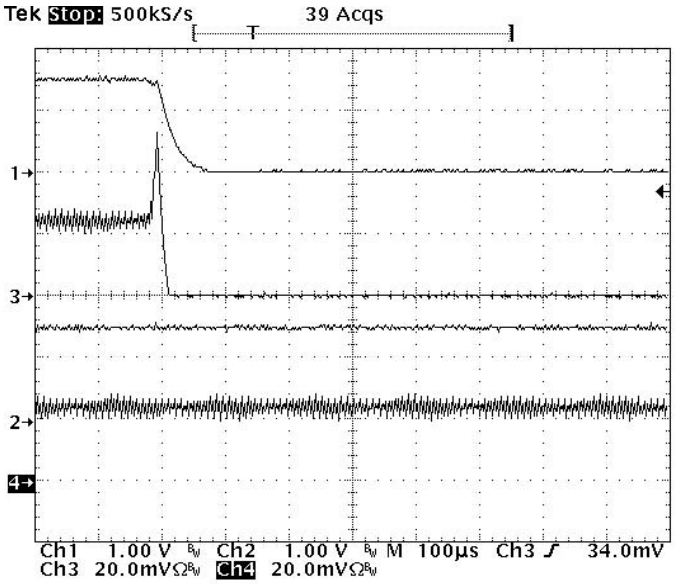
Ch1: Output 1 voltage, 1V/div
Ch2: Output 2 voltage, 1V/div
Ch3: Output 1 load current, 10A/div
Ch4: Output 2 load current, 10A/div

Fig. 24: iP1201PbF hiccup response (Output 1 hiccups due to overload, whereas Output 2 continues uniterrupted)



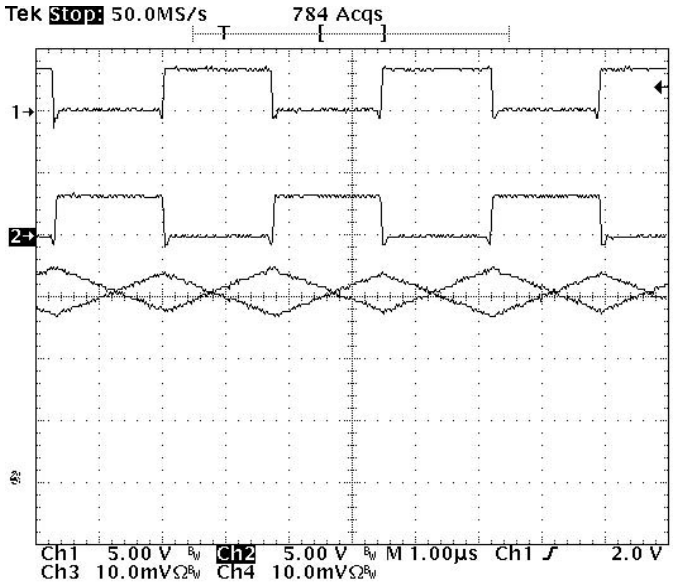
Ch1: Output voltage, 20mV/div ac
Ch4: Load current, 5A/div

Fig. 25: iP1201PbF Transient response load steps 1A to 12A and 12A to 1A



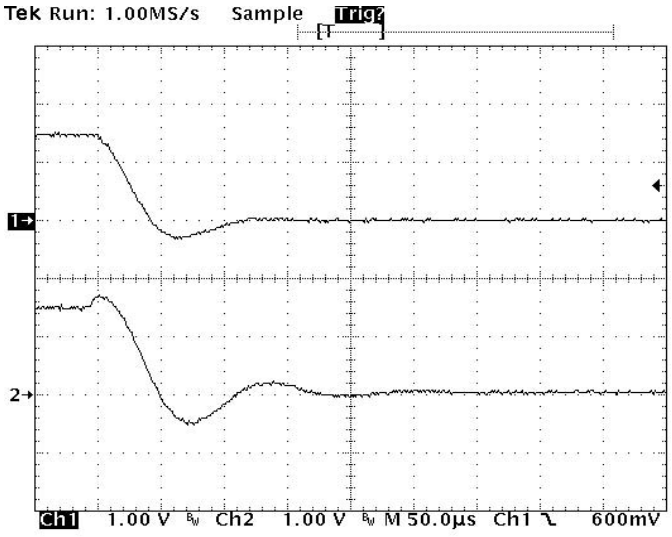
Ch1: Output 1 voltage, 1V/div
Ch2: Output 2 voltage, 1V/div
Ch3: Output 1 load current, 10A/div
Ch4: Output 2 load current, 10A/div

Fig. 27: iP1201PbF latched overcurrent response (output1 shutsdown due to overload, whereas output2 continues uninterrupted)



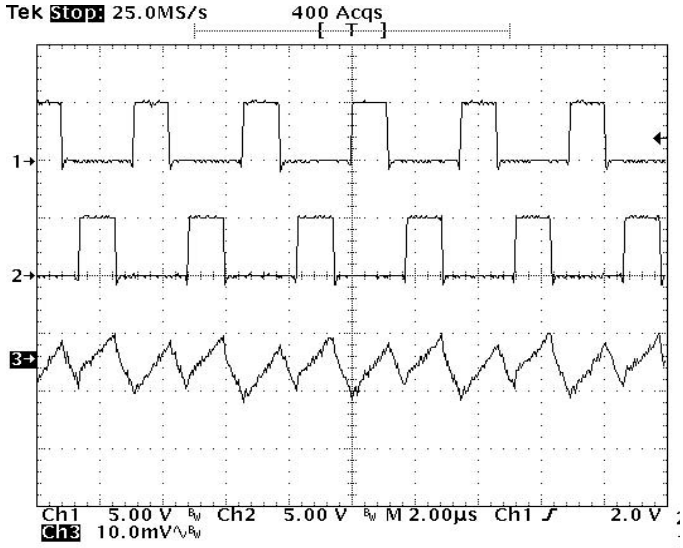
Vin=3.3V
Ch1: Output 1 switch node voltage 5V/div
Ch2: Output 2 switch node voltage 5V/div
Ch3: Output 1 inductor current, 5A/div
Ch4: Output 2 inductor current , 5A/div

Fig. 28: iP1201PbF inductor current sharing



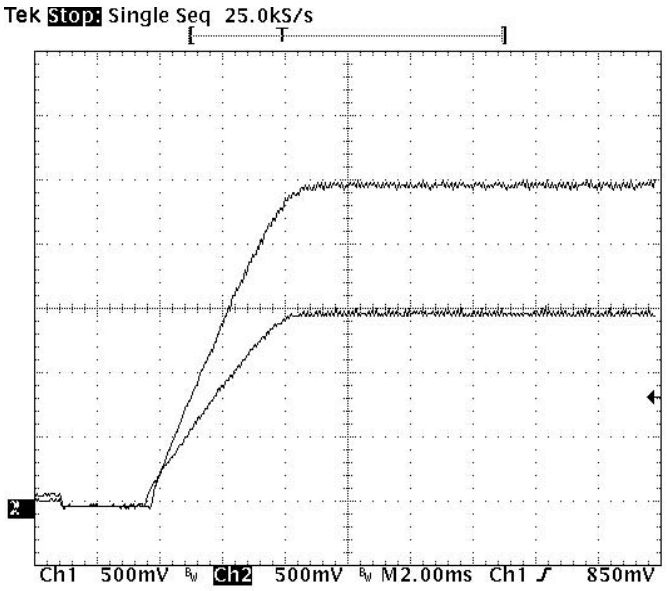
Ch1: Output1 voltage, 1V/div
Ch2: Output2 voltage, 1V/div

Fig. 29: iP1201PbF overvoltage trip. (Overvoltage on output2 causes both outputs to shutdown)



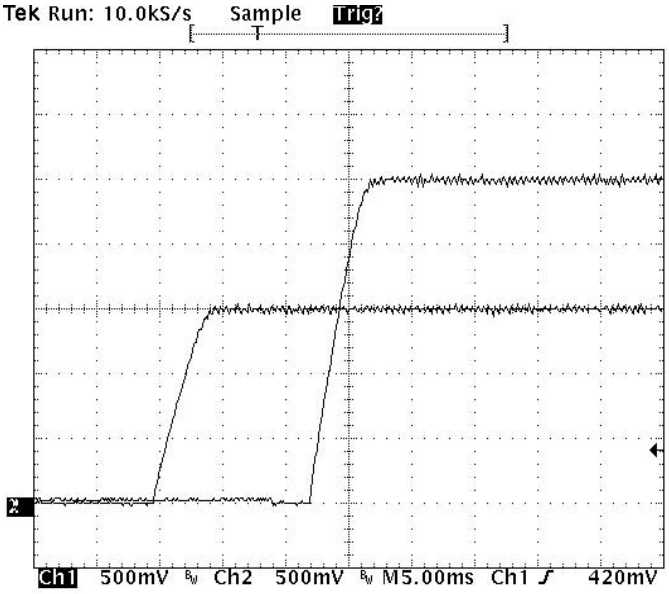
Vin=5V
Ch1: Output 1 switch node voltage 5V/div
Ch2: Output 2 switch node voltage 5V/div
Ch3: Output voltage ripple, 10mV/div

Fig. 30: iP1201PbF Output voltage ripple in parallel configuration



Ch1: Output 1, 0.5V/div
Ch2: Output 2, 0.5V/div

Fig. 31: iP1201PbF output sequencing with separate soft-start capacitors



Ch1: Output 1, 0.5V/div
Ch2: Output 2, 0.5V/div

Fig. 32: iP1201PbF output sequencing with separate soft-start capacitor and delayed turn-on

Layout Guidelines

For stable and noise free operation of the whole power system, it is recommended that the designer uses the following guidelines:

1. Follow the layout scheme presented in Fig. 33. Make sure that the output inductors L1 and L2 are placed as close to iP1201PbF as possible to prevent noise propagation that can be caused by switching of power at the switching node Vsw, to sensitive circuits.

2. Provide a mid-layer solid ground plane with connections to the top layer through vias. The PGND pads of iP1201PbF also need to be connected to the same ground plane through vias.

3. To increase power supply noise immunity, place input and output capacitors close to one another, as shown in the layout diagram. This will provide short high current paths that are essential at the ground terminals.

4. Although there is a certain degree of V_{IN} bypassing inside the iP1201PbF, the external input decoupling capacitors should be as close to the device as possible.

5. The Feedback tracks from the outputs V_{OUT1} and V_{OUT2} to FB1 and FB2 respectively, should be routed as far away from noise generating traces as possible.

6. The compensation components and the Vref bypass capacitor should be placed as close as possible to their corresponding iP1201PbF pins.

7. For single output configuration, the parasitic paths leading to the common output connector from each parallel branch should be symmetrically routed to ensure equal current sharing.

8. Refer to IR application note AN-1029 to determine what size vias and copper weight and thickness to use when designing the PCB.

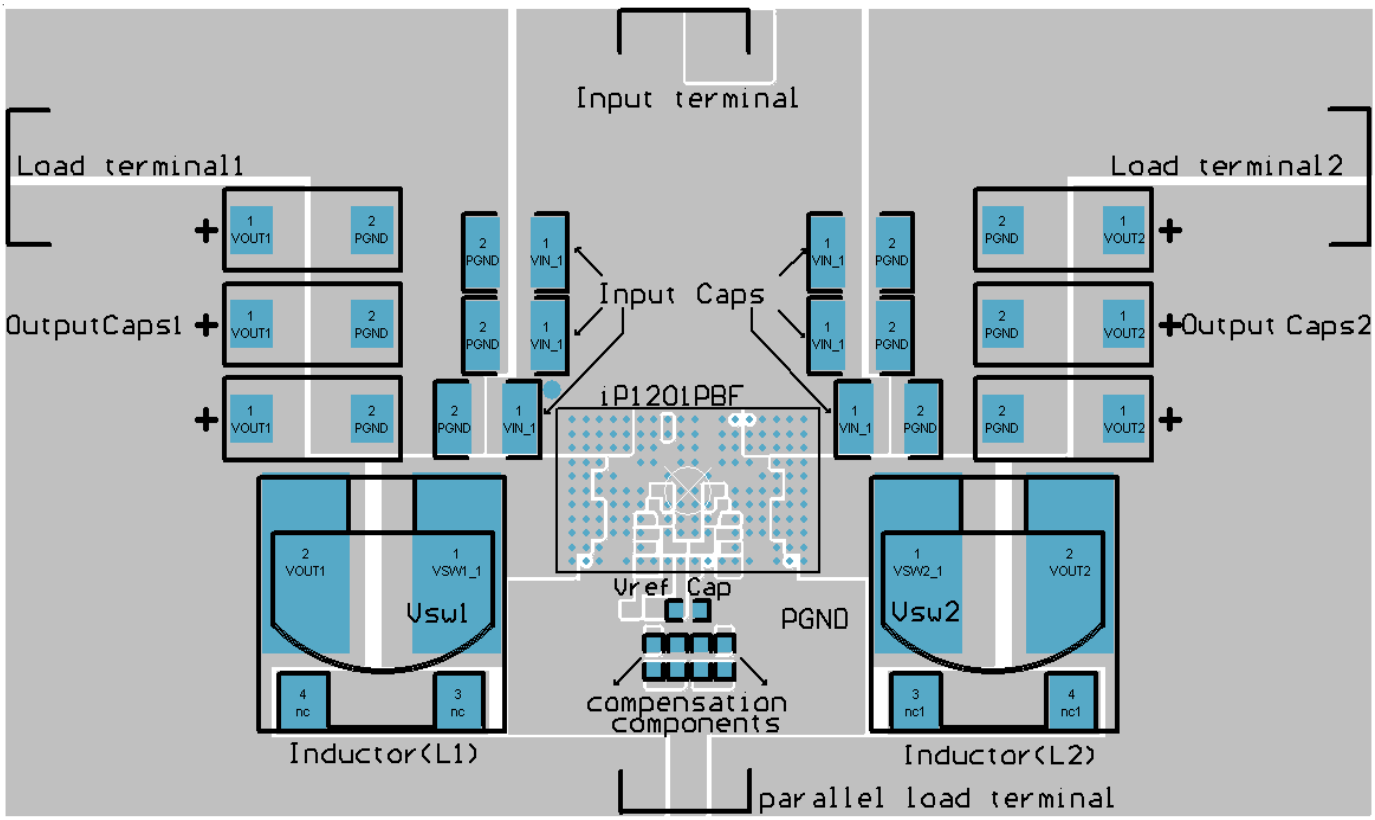


Fig. 33: iP1201PbF suggested layout