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KA3524

SMPS Controller

Features

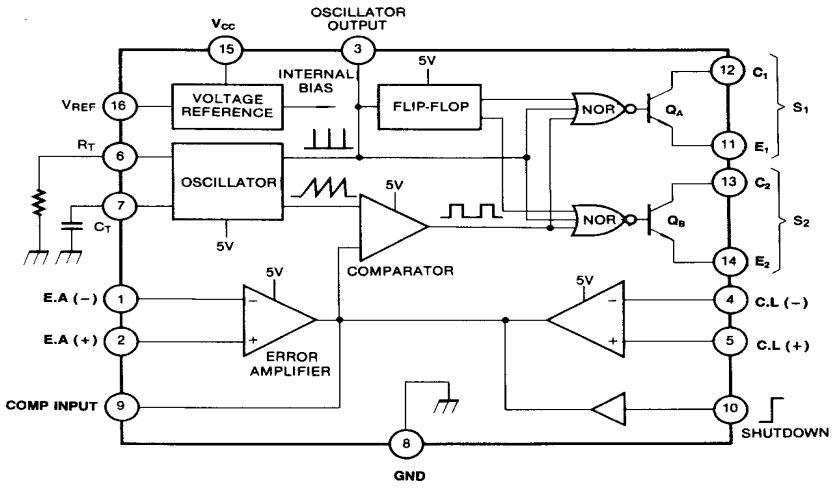
- Complete PWM power control circuit
- Operation beyond 100KHz
- 2% frequency stability with temperature
- Total quiescent current less than 10mA
- Single ended or push-pull outputs
- Current limit amplifier provides external component protection
- On-chip protection against excessive junction temperature and output current
- 5V, 50mA linear regulator output available to user

Description

The KA3524 regulating pulse width modulator contains all of the control circuit necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50mA to external circuit , a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shut-down circuit. Both the regulator output transistor and each output switch are internally current limiting and, to limit junction temperature, aninternal thermal shutdown circuit is employed.

16-DIP

Internal Block Diagram



Rev. 5.0

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	40	V
Reference Output Current	I_{REF}	50	mA
Output Current (Each Output)	I_O	100	mA
Oscillator Charging Current (pin 6 or 7)	$I_{CHG(OSC)}$	5	mA
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	300	°C
Power Dissipation (T_A = 25°C)	P_D	1000	mW
Operating Temperature	T_{POR}	0 ~ +70	°C
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Electrical Characteristics

(V_{IN}=20V, f=20KHz, T_A = 0 to +70°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	-	4.6	5.0	5.4	V
Line Regulation	ΔV_{REF}	V_{CC} = 8V to 40V	-	10	30	mV
Load Regulation	ΔV_{REF}	I_{REF} = 0 mA to 20 mA	-	20	50	mV
Ripple Rejection	RR	f = 120Hz, T_A = 25°C	-	66	-	dB
Short-Circuit Output Current	I_{SC}	V_{REF} = 0, T_A = 25°C	-	100	-	mA
Temperature Stability	ST_T	-	-	0.3	1	%
Long Term Stability	ST	T_A = 25°C	-	20	-	mV/KHr
OSCILLATOR SECTION						
Maximum Frequency	$f_{(MAX)}$	C_T = 0.001uF, R_T = 2KΩ	-	350	-	KHz
Initial Accuracy	ACCUR	R_T and C_T constant	-	5	-	%
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	V_{CC} = 8V to 40V, T_A = 25°C	-	-	1	%
Frequency Change with Temperature	$\Delta f/\Delta T$	Over operating temperature range	-	-	2	%
Clock Amplitude (Pin 3)	$V_{(CLK)}$	T_A = 25°C	-	3.5	-	V
Clock Width (Pin 3)	$t_{W(CLK)}$	C_T = 0.01uF, T_A = 25°C	-	0.5	-	μs
ERROR AMPLIFIER SECTION						
Input Offset Voltage	V_{IO}	V_{CM} = 2.5V	-	2	10	mV
Input Bias Current	I_{BIAS}	V_{CM} = 2.5V	-	2	10	μA
Open Loop Voltage Gain	G_{VO}	-	60	80	-	dB
Common-Mode Input Voltage	V_{CM}	T_A = 25°C	1.8	-	3.4	V
Common-Mode Rejection Ratio	CMRR	T_A = 25°C	-	70	-	dB
Small Signal Bandwidth	BW_{SS}	G_V = 0dB, T_A= 25°C	-	3	-	MHz
Output Voltage Swing	$V_{O(ERR)}$	T_A = 25°C	0.5	-	3.8	V

Electrical Characteristics

(V_{IN}=20V, f=20KHz, T_A=0°C to +70°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
COMPARATOR SECTION						
Maximum Duty Cycle	$D_{(MAX)}$	% Each output on	45	-	-	%
Input Threshold (Pin 9)	V_{TH1}	Zero duty cycle	-	1	-	V
Input Threshold (Pin 9)	V_{TH2}	Maximum duty cycle	-	3.5	-	V
Input Bias Current	I_{BIAS}	-	-	1	-	μA
CURRENT LIMITING SECTION						
Sense Voltage	V_{SENSE}	$V_2 - V_1 \geq 50mV$ V_9 = 2V, T_A = 25°C	180	200	220	mV
Temperature Coefficient of Vsense	$\Delta V_{SENSE}/\Delta T$	-	-	0.2	-	mV/°C
Common-Mode Voltage	V_{CM}	-	0.7	-	1	V
OUTPUT SECTION (EACHOUTPUT)						
Collector-Emitter Voltage	V_{CEO}	-	40	-	-	V
Collector Leakage Current	I_{LKG}	V_{CE} = 40V	-	0.1	50	μA
Saturation Voltage	$V_{CE(SAT)}$	I_C = 50mA	-	1	2	V
Emitter Output Voltage	V_E	V_C = 20V	17	18	-	V
Rise Time (10 to 90)	t_R	R_C = 2KΩ, T_A = 25°C	-	0.2	-	μs
Fall Time (90 to 10)	t_F	R_C = 2KΩ, T_A = 25°C	-	0.1	-	μs
Supply Current	I_{CC}	V_{CC} =40V, PINS 1,4,7,8,11 and 14 are grounded, V_2=2V All other inputs and Outputs open	-	5	10	mA

Application Information

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher current with an external PNP as shown in Figure 2.

Expanded Reference Current Capability

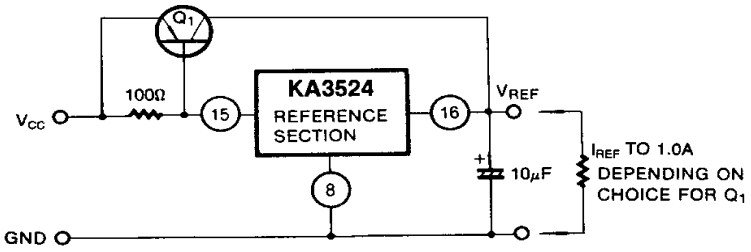


Fig. 2

Oscillator

The oscillator in the KA3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T), While this uses more current than a series connected PC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V/R_T$ and should be kept within the range of approximately 30uA to 2mA, i.e., $1.8K < R_T < 100K$. The range of values for C_T also has limits as the discharge time of C_t determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figures. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing he blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (= 100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit of the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.01 and0.1 micro farad. The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T ohms and C_T = micro farads. The selection of R_T and C_T can be made for a wide range of operating frequencies by using Fig. 7. Note that for sense regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If It is desired to synchronize the KA3524 to an external clock, a pulse of +3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms. If two or more KA3524s must be synchronized together, one must be designated as the master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for an approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse-which occurs first and has a wider pulse width - will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal pin 9, which is a high impedance node ($R_{L:}$=5MΩ). The gain is

$$G_V = gmR_L = \frac{8I_L R_L}{2K_T} = 0.002\ R_L$$

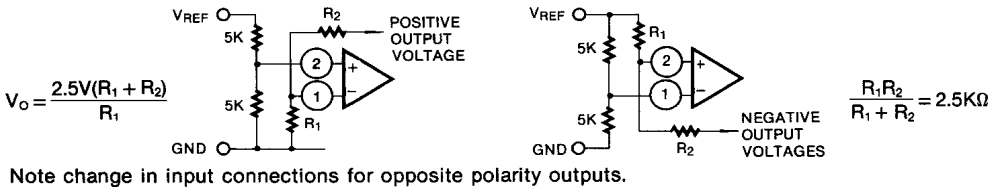
and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 8,In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 5 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over frequency at 5MHz.typically, most output filter designs will introduce one or more addition poles at a significantly higher power frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50KΩ plus 0.001 micro farad. One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200uA can pull this point to ground, thus shutting off both outputs. While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output sign inversions may happen. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 3. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the KA3524 is shown in Figure 4.
By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1 :

Threshold = $V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$
= I_1R_2 = 200mV

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle. In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, fold back current limiting can be provided with the network of Figure 5. This circuit can reduce the short circuit current (I_{SC})to approximately one third the maximum available output current (I_{MAX}).



$$V_O = \frac{2.5V(R_1 + R_2)}{R_1} \qquad \frac{R_1R_2}{R_1 + R_2} = 2.5K\Omega$$

Figure 3. Error Amplifier Biasing Circuits

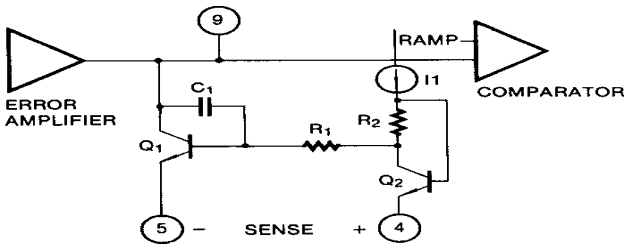


Figure 4. Current Limiting Circuit Of The Ka3524

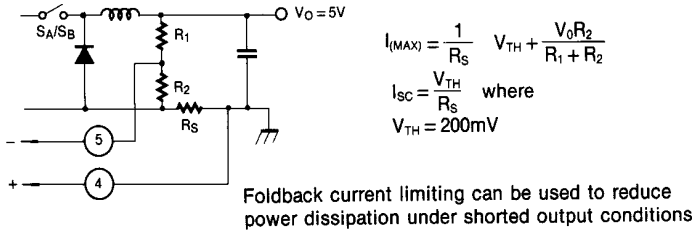


Figure 5. Foldback Current Limiting

Typical Performance Characteristics

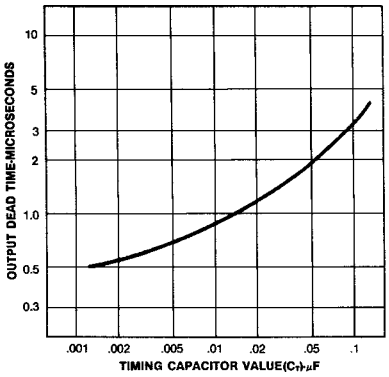


Figure 6. Output Stage Dead Time As A Function

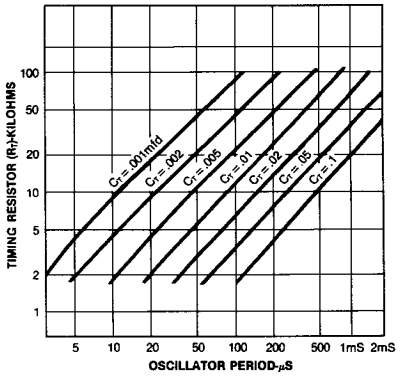


Figure 7. Oscillator Period As A Function Of R_t And C_t Of The Timing Capacitor Value

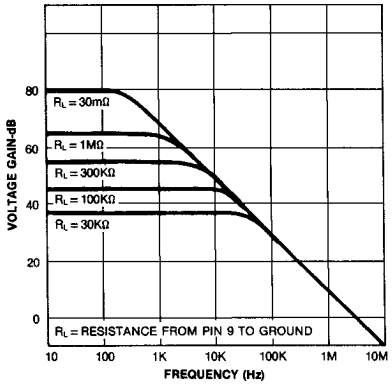


Figure 8. Amplifies Open-loop Gain As A Function Of Freguency And Loading On Pin 9

Typical Applications

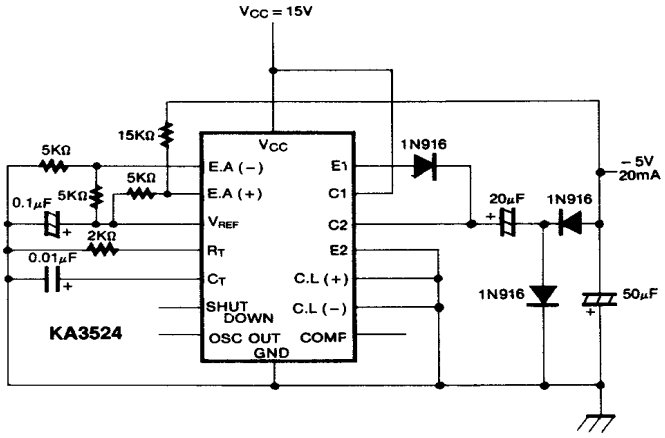


Figure 9. Capacitor-diode Output Circuit

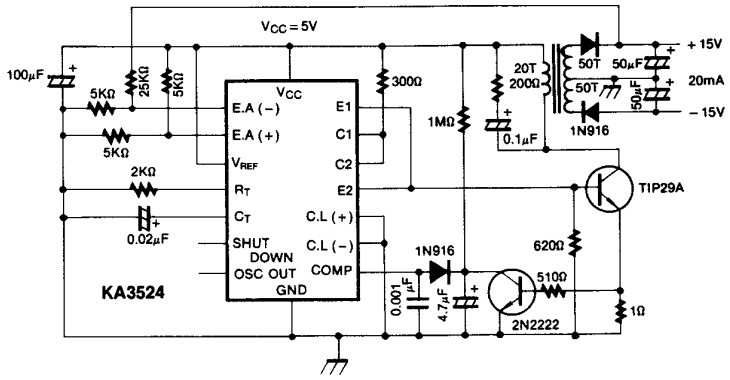


Figure 10. Flyback Converter Circuit

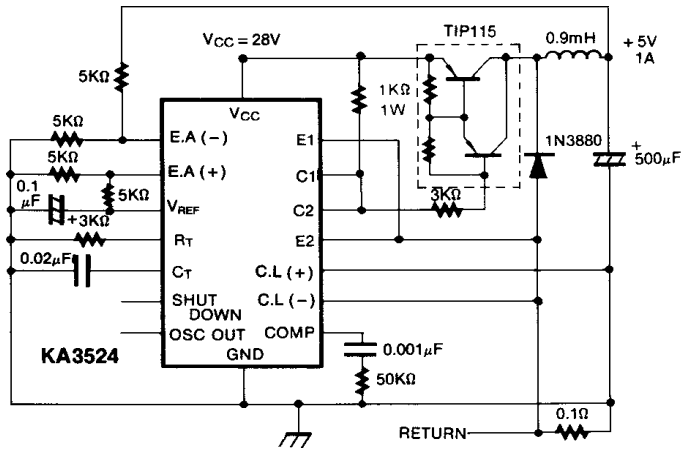


Figure 11. Single-ended Lc Circuit

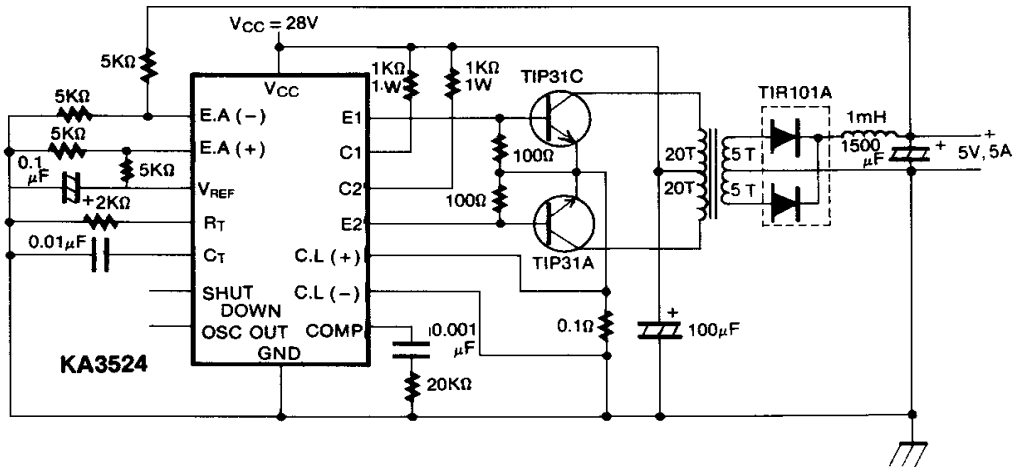
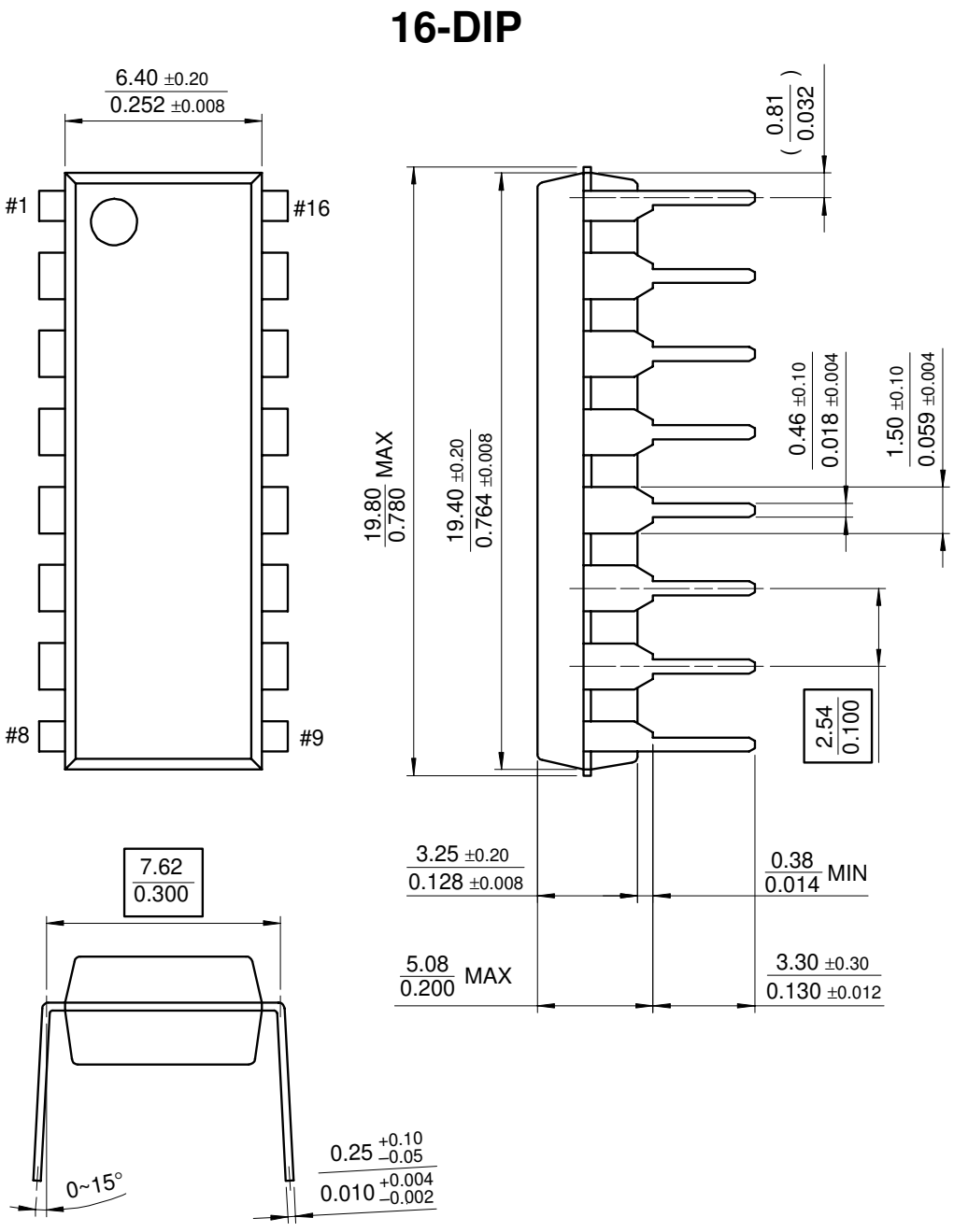


Figure 12. Push-pull Transformer-coupled Circuit

Mechanical Dimensions

Package

Dimensions in millimeters



Ordering Information

Product Number	Package	Operating Temperature
KA3524	16-DIP	0 ~ 70°C

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