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TEA1753LT

HV start-up DCM/QR flyback controller with integrated DCM/QR PFC controller

Rev. 3 — 24 August 2012 Product data sheet

1. General description

The TEA1753LT is the third generation of green Switched Mode Power Supply (SMPS) controller ICs. The TEA1753LT combines a controller for Power Factor Correction (PFC) and a flyback controller. Its high level of integration allows the design of a cost-effective power supply with a very low number of external components.

The special built-in green functions provide high efficiency at all power levels. This efficiency applies to quasi-resonant operation at high-power levels, quasi-resonant operation with valley skipping, as well as to reduced frequency operation at lower power levels. At low-power levels, the PFC switches off to maintain high efficiency.

During low-power conditions, the flyback controller switches to frequency reduction mode and limits the peak current to an adjustable minimum value. This mode ensures high efficiency at low-power and good standby power performance while minimizing audible noise from the transformer.

The controller can be switched to the power-down mode for no-load operation. In this mode, the controller is shut down for very low standby power applications

The TEA1753LT is a Multi-Chip Module (MCM), containing 2 chips. The proprietary high-voltage BCD800 process which makes direct start-up possible from the rectified universal mains voltage in an effective and green way. The second low voltage Silicon On Insulator (SOI) is used for accurate, high-speed protection functions and control.

The TEA1753LT enables the design of highly efficient and reliable supplies with power requirements of up to 250 W using a minimum number of external components.

Remark: All values provided throughout the running text, are typical values unless otherwise stated.

2. Features and benefits

2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Dual-boost PFC with accurate maximum output voltage (NXP patented)
- High level of integration, resulting in a very low external component count and a cost-effective design
- Adjustable PFC switch-off delay

2.2 Green features

- On-chip start-up current source
- Power down functionality for very low standby power

2.3 PFC green features

- Valley/zero voltage switching (ZVS) for minimum switching losses (NXP patented)
- Frequency limitation to reduce switching losses
- PFC is switched off when a low load is detected at the flyback output

2.4 Flyback green features

- Valley switching for minimum switching losses (NXP patented)
- Frequency reduction with adjustable minimum peak current at low-power operation to maintain high efficiency at low output power levels

2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection with demagnetization detection for both converters (NXP patented)
- UnderVoltage Protection (UVP) (foldback during overload)
- Accurate OverVoltage Protection (OVP) for both converters (adjustable for flyback converter)
- Mains voltage independent OverPower Protection (OPP)
- Open control loop protection for both converters. The open-loop protection on the flyback converter is latched
- OverTemperature Protection (OTP)
- Low and adjustable OverCurrent Protection (OCP) trip level for both converters
- General-purpose latched protection input for system OverTemperature Protection (OTP) for example

3. Applications

- The device is used in all applications requiring an efficient and cost-effective power supply solution up to 250 W. Notebook adapters, in particular, benefit from the high level of integration

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1753LT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

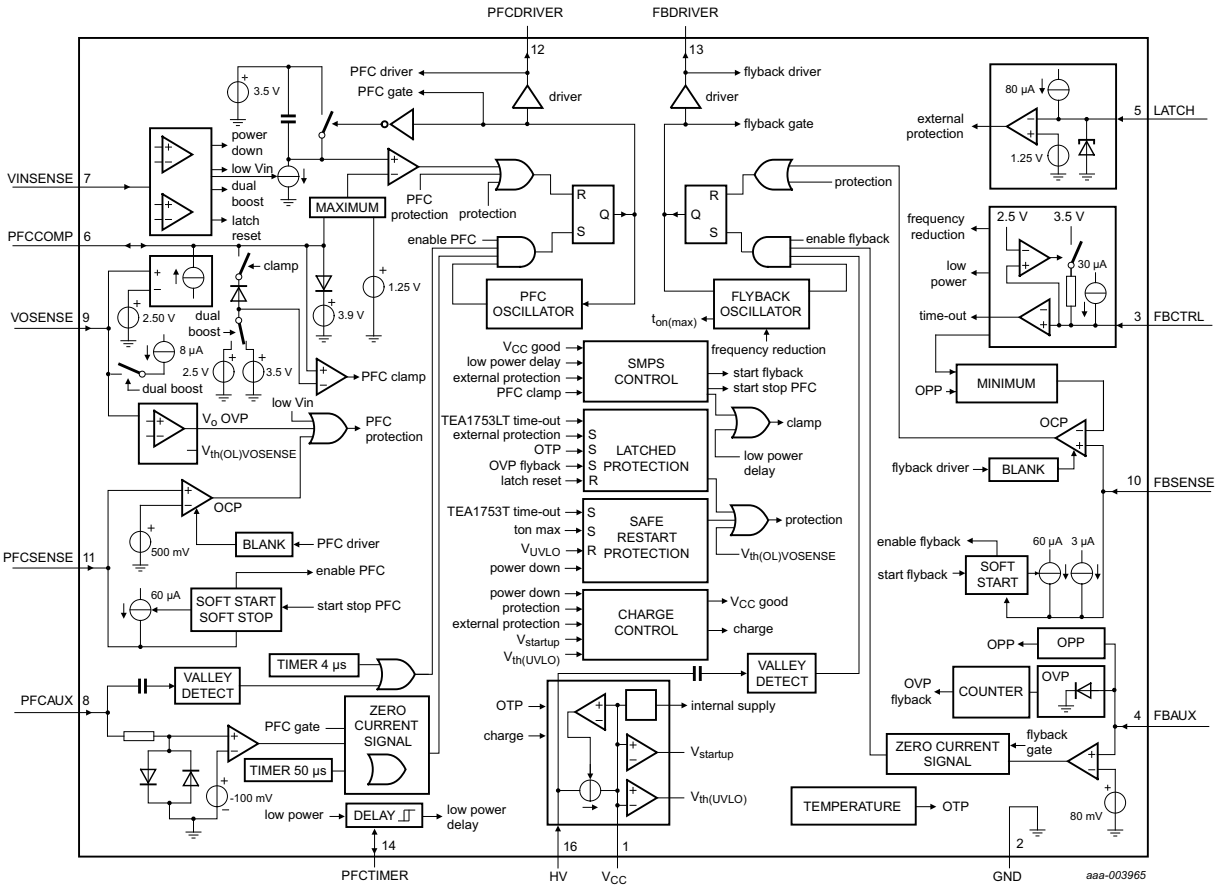


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

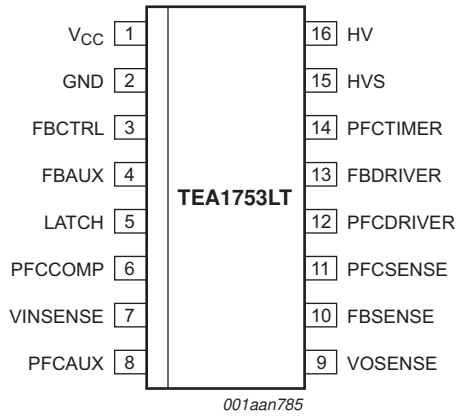


Fig 2. Pin configuration: TEA1753LT (SOT109-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
FBCTRL	3	flyback control input
FBAUX	4	auxiliary winding input for demagnetization timing and flyback OVP
LATCH	5	general-purpose protection input
PFCCOMP	6	frequency compensation pin for PFC
VINSENSE	7	mains voltage sense input
PFCAUX	8	auxiliary winding input for demagnetization timing for PFC
VOSENSE	9	sense input for PFC output voltage
FBSENSE	10	flyback current sense input
PFCSENSE	11	PFC current sense input
PFCDRIVER	12	PFC gate-driver output
FBDRIVER	13	flyback gate-driver output
PFCTIMER	14	delay timer pin for PFC on/off control
HVS	15	high-voltage safety spacer, not connected
HV	16	high-voltage start-up/ flyback valley sensing

7. Functional description

7.1 General control

The TEA1753LT contains a controller for a power factor correction circuit as well as a controller for a flyback circuit. A typical configuration is shown in Figure 3.

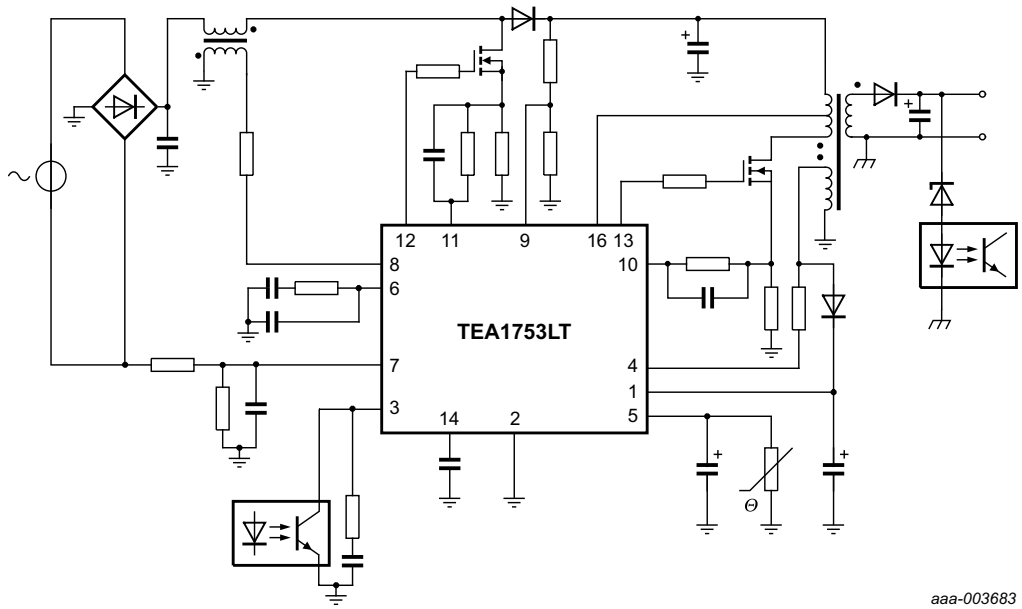


Fig 3. TEA1753LT IC typical configuration

7.1.1 Start-up and UnderVoltage LockOut (UVLO)

Initially the capacitor on the V_{CC} pin is charged from the high-voltage mains using the HV pin.

When V_{CC} is less than V_{trip}, the charge current is low. This low current protects the IC if the V_{CC} pin is shorted to ground. To ensure a short start-up time, the charge current above V_{trip} is increased until V_{CC} reaches $V_{th(UVLO)}$. When V_{CC} is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current returns to low to ensure a low safe restart duty cycle during fault conditions.

The control logic activates the internal circuitry and switches off the HV charge current when the voltage on pin V_{CC} passes the $V_{startup}$ level. First, the LATCH pin current source is activated and the soft-start capacitors on the PFCSENSE and FBSENSE pins are charged. Also the clamp circuit on the PFCCOMP pin is activated.

The PFC circuit is activated when the following conditions are met:

- the LATCH pin voltage exceeds the $V_{en(LATCH)}$ voltage
- the PFCCOMP pin voltage reaches the $V_{en(PFCCOMP)}$ voltage
- the soft-start capacitor on the PFCSENSE pin is charged

If the soft start capacitor on the FBSENSE pin is charged, the flyback converter is also activated. The flyback converter output voltage is then regulated to its nominal output voltage. The auxiliary winding of the flyback converter takes over the IC supply. See Figure 4.

If during start-up the LATCH pin does not reach the $V_{en(LATCH)}$ level before V_{CC} reaches $V_{th(UVLO)}$, it is deactivated. The charge current is then switched on again.

When the flyback converter starts, V_{FBCTRL} is monitored. If this output voltage does not reach its intended regulation level within a specified time, the voltage on the FBCTRL pin reaches the $V_{to(FBCTRL)}$ level. An error is then assumed and a latched protection is initiated.

When one of the protection functions is activated, both converters stop switching and the V_{CC} voltage drops to $V_{th(UVLO)}$. A latched protection recharges capacitor C_{VCC} using the HV pin, but does not restart the converters. To provide safe restart protection, the capacitor is recharged using the HV pin and the device restarts (see block diagram, Figure 1).

If OVP of the PFC circuit ($V_{VOSENSE} > V_{OVP(VOSENSE))}$ occurs, the PFC controller stops switching until the VOSENSE pin voltage drops to less than $V_{OVP(VOSENSE)}$. If a mains undervoltage is detected, $V_{VINSENSE} < V_{stop(VINSENSE)}$, the PFC controller stops switching until $V_{VINSENSE} > V_{start(VINSENSE)}$ again.

When the voltage on the V_{CC} pin drops below the undervoltage lockout level, both controllers stop switching and re-enter the safe restart mode. In the safe restart mode, the driver outputs are disabled and the V_{CC} pin voltage is recharged using the HV pin.

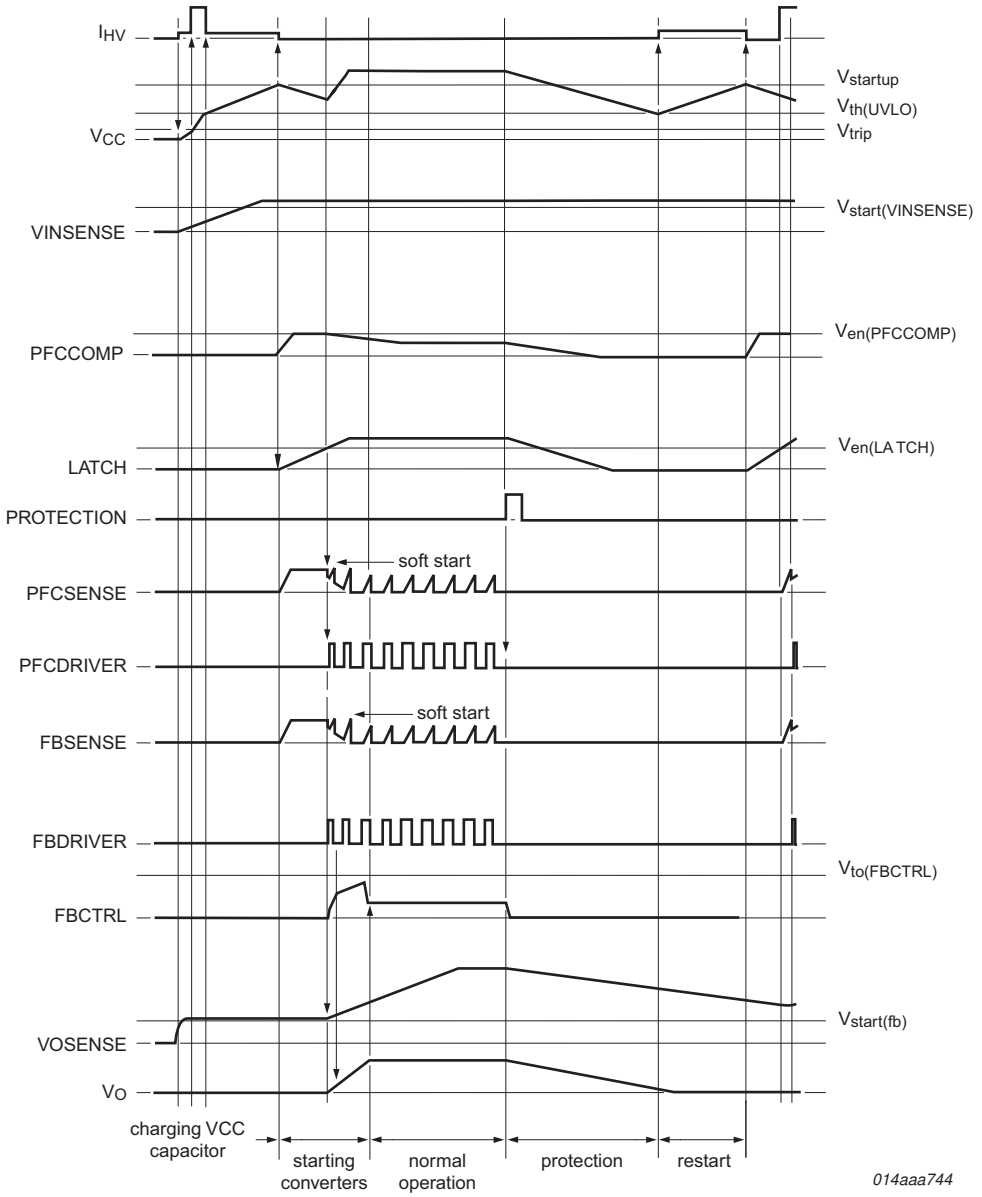


Fig 4. Start-up sequence, normal operation and restart sequence

7.1.2 Power down

The power-down mode is activated for very low standby power applications by pulling the VINSENSE pin below the $V_{th(pd)}$ level. The TEA1753LT stops switching and the safe restart protection is activated. The high-voltage start-up current source is also disabled during power-down, so the TEA1753LT does not restart until the VINSENSE pin voltage is raised again. During power down all internal circuitry is disabled except for a voltage detection circuit on the VINSENSE pin. This circuit is supplied by the HV pin and draws 16 μA from the HV pin for biasing.

If the VINSENSE pin is pulled low, a latched protection is also reset. (see Section 7.1.5)

7.1.3 Supply management

All internal reference voltages are derived from a temperature compensated and trimmed on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

7.1.4 Latch input

The LATCH pin is a general-purpose input pin, which is used to switch off both converters. The pin sources a current $I_{O(LATCH)}$ of 80 μA. Switching is stopped as soon as the voltage on this pin drops below 1.25 V.

At initial start-up, switching is inhibited until the capacitor on the LATCH pin is charged above 1.35 V. No internal filtering is done on this pin. An internal Zener clamp of 2.9 V protects this pin from excessive voltages.

7.1.5 Fast latch reset

In a typical application, the mains is interrupted briefly to reset the latched protection. The PFC bus capacitor, C_{bus}, does not have to discharge for this latched protection to reset.

When the VINSENSE voltage drops below 750 mV and is then raised to 870 mV, the latched protection is reset.

The latched protection is also reset by removing the voltage on the V_{CC} and HV pins.

7.1.6 Overtemperature protection

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching. As long as OTP is active, the capacitor C_{VCC} is not recharged from the HV mains. If the V_{CC} supply voltage is not sufficient, the OTP circuit is supplied from the HV pin.

OTP is a latched protection. It is reset by removing the voltage on the V_{CC} and HV pins or by the fast latch reset function. (See Section 7.1.5)

7.2 Power factor correction circuit

The power factor correction circuit operates in quasi-resonant or Discontinuous Conduction Mode (CDM) with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. V_{PFCAUX} is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

7.2.1 t_{on} control

The power factor correction circuit is operated in t_{on} control. The resulting mains harmonic reduction is well within the class-D requirements.

7.2.2 Valley switching and demagnetization (PFCAUX pin)

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. To reduce switching losses and electromagnetic Interference (EMI) (valley switching), the next stroke is started if the voltage across the PFC MOSFET is at its minimum.

If a demagnetization signal is not detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 μs after the last PFCGATE signal.

If a valley signal is not detected on the PFCAUX pin, the controller generates a valley signal 4 μs after demagnetization is detected.

To protect the internal circuitry during lightning events, for example, add a 5 kΩ series resistor to PFCAUX. To prevent incorrect switching due to external disturbance, place the resistor close to the IC on the printed-circuit board.

7.2.3 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation is above the $f_{sw(PFC)max}$ limit, the system switches over to DCM. The PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching).

7.2.4 Mains voltage compensation (VINSENSE pin)

The equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application this results in a low bandwidth for low mains input voltages and a high bandwidth for high mains input voltages.

To compensate for the mains input voltage influence, TEA1753LT contains a correction circuit. The average input voltage is measured using the VINSENSE pin and the information is fed to an internal compensation circuit. Using this compensation, it is possible to keep the regulation loop bandwidth constant over the mains input range. This yields a fast transient response on load steps, while still complying with class-D MHR requirements.

In a typical application, a resistor and two capacitors on the PFCCOMP pin set the bandwidth of the regulation loop.

7.2.5 Soft start-up (PFCSENSE pin)

To prevent audible transformer noise at start-up or during hiccup, the soft-start function slowly increases the transformer peak current. This increase is achieved by inserting R_{SS1} and C_{SS1} between the PFCSENSE pin and current sense resistor R_{SENSE1}. An internal current source charges the capacitor to:

$$V_{PFCSENSE} = I_{start(soft)PFC} \times R_{SS1} \quad (1)$$

The voltage is limited to $V_{start(soft)PFC}$.

The start level and the time constant of the increasing primary current level is adjusted externally by changing the values of R_{SS1} and C_{SS1}.

$$\tau soft\text{–}start = 3 \times R_{SS1} \times C_{SS1} \quad (2)$$

The charging current $I_{start(soft)PFC}$ flows as long as $V_{PFCSENSE}$ is below 0.5 V. If $V_{PFCSENSE}$ exceeds 0.5 V, the soft-start current source starts limiting current $I_{start(soft)PFC}$. When the PFC starts switching, the $I_{start(soft)PFC}$ current source is switched off; see Figure 5.

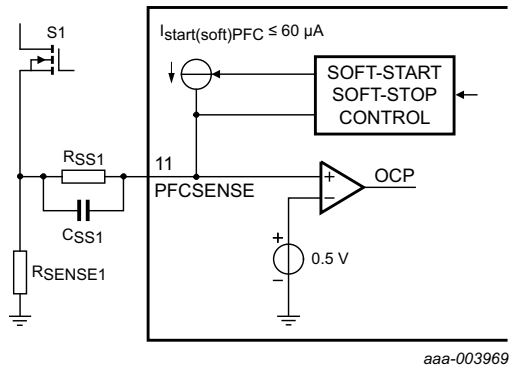


Fig 5. Soft-start-up of PFC

7.2.6 Low-power mode

When the output power of the flyback converter (see Section 7.3) is low, the flyback converter switches over to frequency modulation mode. When the maximum switching frequency of the flyback drops below 48 kHz, the power factor correction circuit is switched off to maintain high efficiency. Connect a capacitor to the PFCTIMER pin to delay switching off (see also Section 7.2.7).

During low-power mode operation, the PFCCOMP pin is clamped to a minimum voltage of 3.5 V or 2.5 V and a maximum voltage of 3.9 V. The lower clamp voltage depends on the voltage on VINSENSE pin. This voltage limits the maximum power that is delivered when the PFC is switched on again. The upper clamp voltage ensures that the PFC returns from low-power mode to its normal regulation point in a limited time.

When the maximum switching frequency of the flyback converter exceeds 86 kHz, the power factor correction circuit restores normal operation.

7.2.7 PFC off delay (pin PFCTIMER)

When the flyback converter maximum frequency drops below 48 kHz, the PFC is switched off. The IC then outputs a 5 µA current to the PFCTIMER pin. When the voltage on the PFCTIMER pin reaches 3.6 V, the PFC is switched off by performing a soft-stop.

When the flyback converter frequency exceeds 86 kHz, a switch discharges the PFCTIMER pin capacitor. When the voltage on the PCTIMER pin drops below 1.27 V, the PFC is switched on (see Figure 6).

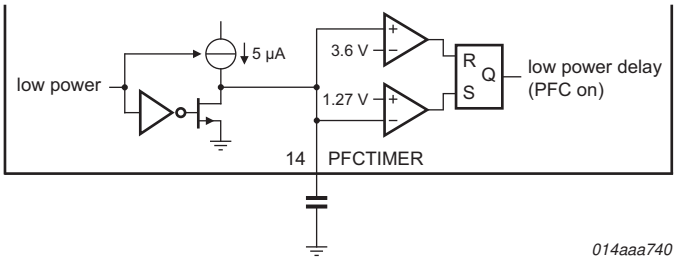


Fig 6. PFC start/stop via PPFCTIMER pin

7.2.8 Dual-boost PFC

The mains input voltage modulates the PFC output voltage. The mains input voltage is measured using the VINSENSE pin. If the voltage on the VINSENSE pin drops below 2.2 V, the current is sourced from the VOSENSE pin. To ensure the stable switch-over, a 200 mV transition region is inserted around the 2.2 V, see Figure 7.

For low VINSENSE input voltages, the output current is 8 μA. This output current, in combination with the resistors on the VOSENSE pin, sets the lower PFC output voltage level at low mains voltages. At high mains input voltages, the current is switched to zero. The PFC output voltage is then at its maximum. As this current is zero in this situation, it does not affect the accuracy of the PFC output voltage.

For proper switch-off, the VOSENSE current is switched to its maximum value of 8 μA when the voltage on pin VOSENSE drops below 2.1 V.

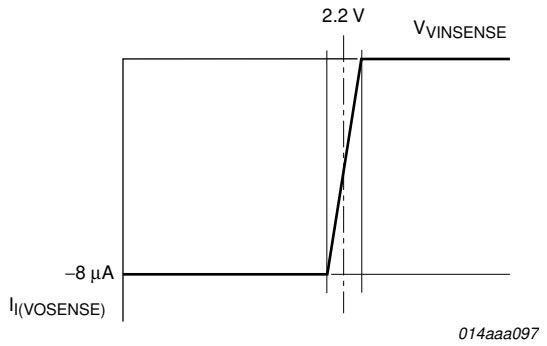


Fig 7. Voltage to current transfer function for dual boost PFC

7.2.9 Overcurrent protection (PFCSENSE pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor, R_{SENSE1}, on the source of the external MOSFET. The voltage is measured using the PFCSENSE pin.

7.2.10 Mains undervoltage lockout/brownout protection (VINSENSE pin)

To prevent the PFC from operating at very low mains input voltages, the voltage on the VINSENSE pin is continuously sensed. When the voltage on this pin drops below the $V_{stop(VINSENSE)}$ level, switching of the PFC is stopped.

7.2.11 Overvoltage protection (VOSENSE pin)

To prevent output overvoltage during load steps and mains transients, an overvoltage protection circuit is built in.

When the voltage on the VOSENSE pin exceeds the $V_{ovp(VOSENSE)}$ level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences when the VOSENSE pin voltage drops below the $V_{ovp(VOSENSE)}$ level again.

When the resistor between the VOSENSE pin and ground is open, the overvoltage protection is also triggered.

7.2.12 PFC open-loop protection (VOSENSE pin)

The power factor correction circuit does not start switching until the voltage on the VOSENSE pin is above the $V_{th(ol)(VOSENSE)}$ level. This feature protects the circuit from open-loop and VOSENSE short-circuit.

7.2.13 Driver (PFCDRIVER pin)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of −500 mA and a current sink capability of 1.2 A. These capabilities permit fast turn-on and turn-off of the power MOSFET for efficient operation.

7.3 Flyback controller

The TEA1753LT includes a controller for a flyback converter. The flyback converter operates in quasi-resonant or DCM with valley switching. The auxiliary winding of the flyback transformer provides demagnetization detection and powers the IC after start-up.

7.3.1 Multimode operation

The TEA1753LT flyback controller operates in several modes; see Figure 8.

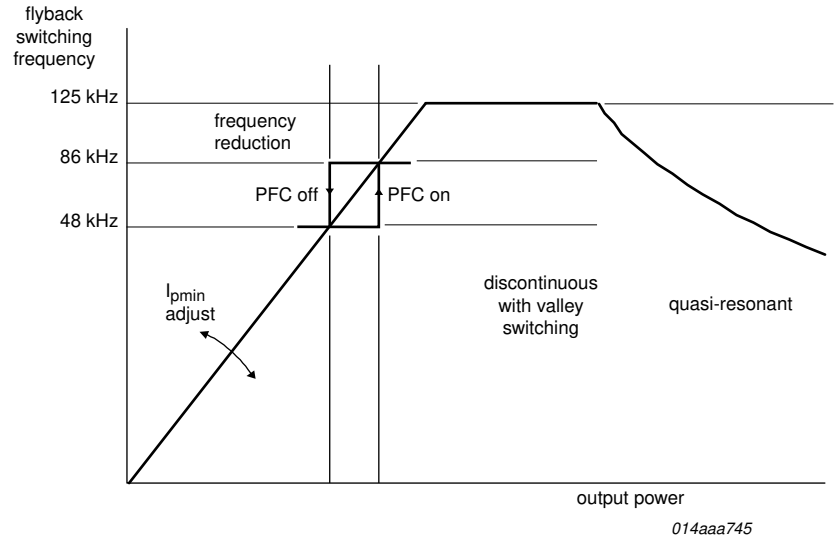


Fig 8. Multimode operation flyback

At high output power the converter switches to quasi-resonant mode. The next converter stroke starts after demagnetization of the transformer and detection of the valley. In quasi-resonant mode switching losses are minimized. This minimization is achieved by the converter only switching on when the voltage across the external MOSFET is at its minimum (see also Section 7.3.2).

To prevent high frequency operation at low loads, the maximum switching frequency is limited to 125 kHz. When the frequency limit is reached, the quasi-resonant operation changes to DCM with valley skipping. This mode limits the MOSFET switch-on losses and conducted EMI.

A Voltage Controlled Oscillator (VCO) controls the frequency at very low power and standby levels. The minimum frequency is reduced to zero. During frequency reduction mode, the primary peak current is kept at an adjustable minimal level to maintain a high efficiency. As the primary peak current is low in frequency reduction operation, no audible noise is noticeable at switching frequencies in the audible range. Valley switching is also active in this mode.

In frequency reduction mode, the PFC controller is switched off. The flyback maximum frequency changes linearly with the control voltage on the FBCTRL pin (see Figure 9). Hysteresis has been added for stable on and off switching of the PFC. At no-load operation, the switching frequency is reduced to (almost) zero.

The input voltage of the flyback converter and the capacitance on the drain node of the flyback power switch affect the frequency reduction slope. By choosing the proper compensation, the frequency reduction slope for high input voltages is chosen as the same as for low input voltages. This compensation yields an input voltage independent PFC switch-on and switch-off power level (see the application information in Section 11).

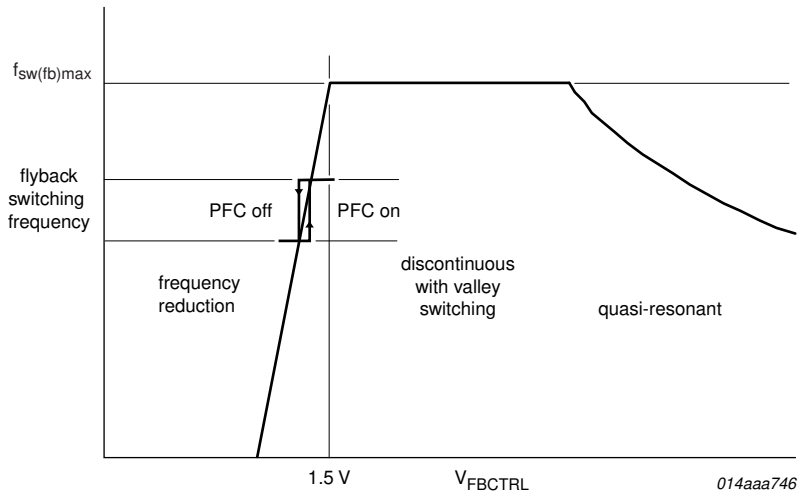


Fig 9. Frequency control of flyback

7.3.2 Valley switching (HV pin)

A new cycle starts when the external MOSFET is switched on. $V_{FBSENSE}$ and V_{FBCTRL} determine the on-time. The MOSFET is then switched off and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately:

$$f = \frac{1}{[2 \times \pi \times \sqrt{(L_p \times C_d)}]} \quad (3)$$

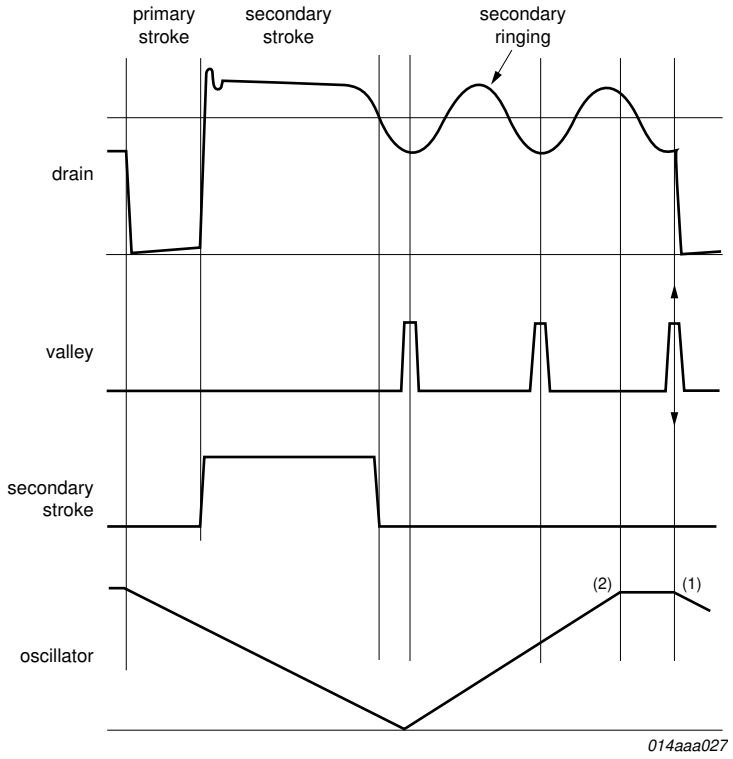
where L_p is the primary self-inductance of the flyback transformer and C_d is the capacitance on the drain node.

When the internal oscillator voltage is high and the secondary stroke ended, the circuit waits for the lowest drain voltage before starting a new primary stroke.

Figure 10 shows the drain voltage, valley signal, secondary stroke signal and the internal oscillator signal.

Valley switching allows high frequency operation as capacitive switching losses are reduced, see Equation 4. High frequency operation makes small and cost-effective magnetic components possible.

$$P = \frac{1}{2} \times C_d \times V^2 \times f \quad (4)$$



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical Pulse Width Modulation (PWM) system without valley detection.

Fig 10. Signals for valley switching

7.3.3 Current mode control (FBSENSE pin)

Current mode control is used for the flyback converter for its good line regulation.

The FBSENSE pin senses the primary current across an external resistor and compares it with an internal control voltage. The internal control voltage is proportional to the FBCTRL pin voltage, see Figure 11.

The FBSENSE pin outputs a current of 3 μA. This current runs through the resistors from the FBSENSE pin to the sense resistor and creates an offset voltage. The minimum peak current of the flyback is adjusted using this offset voltage. Adjusting the minimum peak current level, changes the frequency reduction slope (see Figure 8).

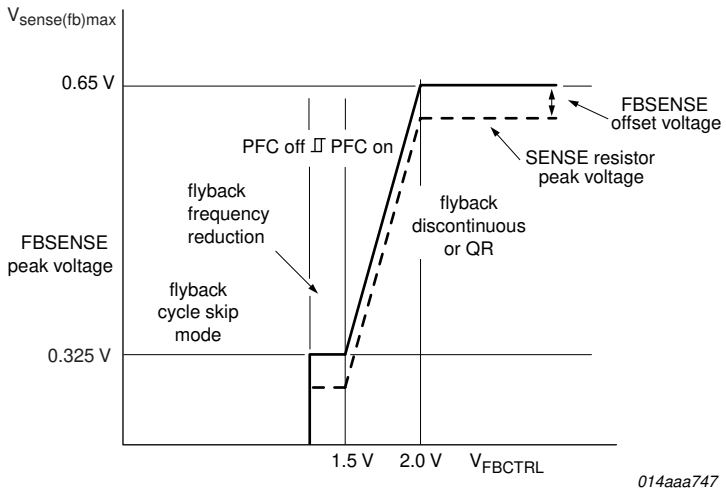


Fig 11. Peak current control of flyback

The driver output is latched in the logic, preventing multiple switch-on.

7.3.4 Demagnetization (FBAUX pin)

The system is always in QR or DCM. The internal oscillator does not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thus reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time of 2 μs. This suppression is necessary at low output voltages and at start-up. It is also required in applications where the transformer has a large leakage inductance.

If the FBAUX pin is open-circuit or not connected, a fault condition is assumed and the converter immediately stops. Operation restarts as soon as the fault condition is removed.

7.3.5 Flyback control/time-out (FBCTRL pin)

The FBCTRL pin is connected to an internal voltage source of 3.5 V using an internal resistor of 3 kΩ. When the voltage on this pin exceeds 2.5 V, the connection is disabled and the pin is biased with a small current. If the voltage on this pin exceeds 4.5 V, a fault is assumed, switching is stopped and a latched protection is activated.

If a capacitor and a resistor are connected in series to this pin, a time-out function is created to protect against an open control loop. See Figure 12 and Figure 13. The time-out function is disabled by connecting a resistor (100 kΩ) to ground on the FBCTRL pin.

If the pin is short-circuited to ground, switching of the flyback controller is prevented.

During normal operating conditions, the converter regulates the output voltage. The voltage on the FBCTRL pin is then between 1.3 V for the minimum output power and 2 V for the maximum output power.

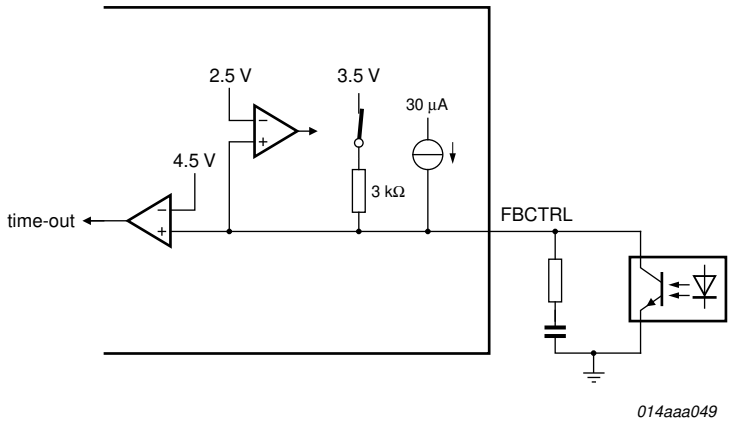


Fig 12. Time-out protection circuit

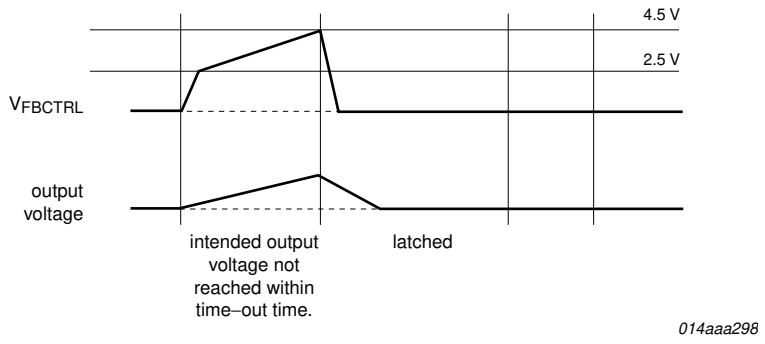


Fig 13. Latched time-out protection (signals) in the TEA1753LT

7.3.6 Soft start-up (FBSENSE pin)

To prevent audible transformer noise during start-up, the soft-start function slowly increases the transformer peak current. This increase is achieved by inserting a resistor and a capacitor between pin 10 (FBSENSE) and the current sense resistor.

An internal current source charges the capacitor to:

$$V = I_{start(soft)fb} \times R_{SS2} \quad (5)$$

with a maximum of approximately 0.63 V.

The start level and the time constant of the increasing primary current level is adjusted externally by changing the values of R_{SS2} and C_{SS2}.

$$\tau soft\text{–}start = 3 \times R_{SS1} \times C_{SS1} \quad (6)$$

The soft-start current $I_{start(soft)fb}$ is switched on as soon as V_{CC} reaches $V_{startup}$. When $V_{FBSENSE}$ has reached 0.63 V, the flyback converter starts switching.

The charging current $I_{start(soft)(FB)}$ flows as long as $V_{FBSENSE}$ is less than approximately 0.63 V. If $V_{FBSENSE}$ exceeds 0.63 V, the soft start current source starts limiting the current. After the flyback converter has started, the soft-start current source is switched off.

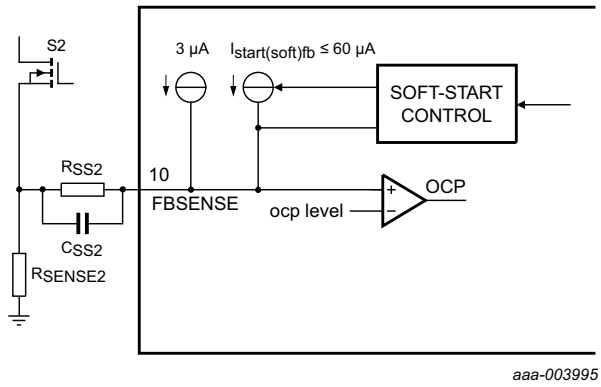


Fig 14. Soft start-up of flyback.

7.3.7 Maximum on-time

The flyback controller limits the on-time of the external MOSFET to 40 µs. When the on-time is longer than 40 µs, the IC stops switching and enters the safe restart mode.

7.3.8 Overvoltage protection (FBAUX pin)

An output overvoltage protection is implemented in the GreenChip III series. In the TEA1753LT, the auxiliary voltage is sensed using the current flowing into the FBAUX pin during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. An internal filter averages voltage spikes.

An internal up-down counter prevents false OVP detection which occurs during ESD or lightning events. The internal counter counts up by one when the output voltage exceeds the OVP trip level within one switching cycle. The internal counter counts down by two when the output voltage has not exceeded the OVP trip level within one switching cycle. When the counter has reached eight, the IC assumes a true OVP, sets the latched protection and switches off both converters.

The converter only restarts after the OVP latch is reset. In a typical application, the internal latch is reset when the VINSENSE voltage drops below 750 mV and is then raised to 870 mV.

The latched protection is also reset by removing both the voltage on the VCC and HV pins.

The demagnetization resistor, R_{FBAUX} sets the output voltage $V_{o(OVP)}$ at which the OVP function trips:

$$V_{o(OVP)} = \frac{N_s}{N_{aux}}(I_{ovp(FBAUX)} \times R_{FBAUX} + V_{clamp(FBAUX)}) \quad (7)$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer. Current $I_{ovp(FBAUX)}$ is internally trimmed.

Accurate OVP detection is made possible by adjusting the value of R_{FBAUX} to the turns ratio of the transformer.

7.3.9 Overcurrent protection (FBSENSE pin)

The primary peak current in the transformer is measured accurately cycle-by-cycle using the external sense resistor R_{sense2}. The OCP circuit limits $V_{FBSENSE}$ to a level set by V_{fbctrl} (see also Section 7.3.3). The OCP detection is suppressed during the leading-edge blanking period, t_{leb}, to prevent false triggering due to switch-on spikes.

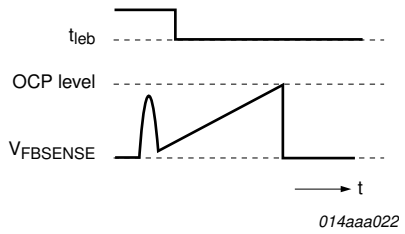


Fig 15. OCP leading edge blanking

7.3.10 Overpower protection

During the primary stroke of the flyback converter, the input voltage is measured by sensing the current that is drawn from the FBAUX pin.

The current information is used to limit the maximum peak current of the flyback converter, measured from the FBSENSE pin. The internal compensation is such, that a maximum output power is realized which is almost independent of the input voltage.

The OPP curve is given in Figure 16.

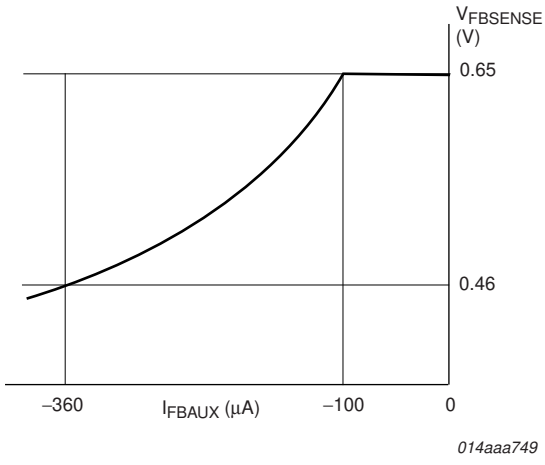


Fig 16. Overpower protection curve

7.3.11 Driver (FBDRIVER pin)

The driver circuit to the power MOSFET gate has a current sourcing capability of −500 mA and a current sink capability of 1.2 A. These capabilities permit fast switching of the power MOSFET for efficient operation.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage			−0.4	+38	V
V_{LATCH}	voltage on the LATCH pin	current limited		−0.4	+5	V
V_{FBCTRL}	voltage on the FBCTRL pin			−0.4	+5	V
$V_{PFCCOMP}$	voltage on the PFCCOMP pin			−0.4	+5	V
$V_{VINSENSE}$	voltage on the VINSENSE pin			−0.4	+5	V
$V_{VOSENSE}$	voltage on the VOSENSE pin			−0.4	+5	V
V_{PFCAUX}	voltage on the PFCAUX pin			−25	+25	V
$V_{FBSENSE}$	voltage on the FBSENSE pin	current limited		−0.4	+5	V
$V_{PFCSENSE}$	voltage on the PFCSENSE pin	current limited		−0.4	+5	V
$V_{PFCTIMER}$	voltage on the PFCTIMER pin			−0.4	+5.5	V
V_{HV}	voltage on the HV pin			−0.4	+650	V
Currents						
I_{FBCTRL}	current on the FBCTRL pin			−3	0	mA
I_{FBAUX}	current on the FBAUX pin			−1	+1	mA
$I_{PFCSENSE}$	current on the PFCSENSE pin			−1	+10	mA
$I_{FBSENSE}$	current on the FBSENSE pin			−1	+10	mA
$I_{FBDRIVER}$	current on the FBDRIVER pin	duty cycle < 10 %		−0.8	+2	A
$I_{PFCDRIVER}$	current on the PFCDRIVER pin	duty cycle < 10 %		−0.8	+2	A
I_{HV}	current on the HV pin			-	8	mA
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.6	W
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model				
		pins 1 to 13	[1]	-	2000	V
		pin 16 (HV)	[1]	-	1500	V
		machine model	[2]	-	200	V
		charged device model		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	124	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	37	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (HV pin)						
I_{HV}	current on the HV pin	V_{HV} > 80 V				
		$V_{CC} < V_{trip}$; $V_{th(UVLO)} < V_{CC} < V_{startup}$	-	1.0	-	mA
		$V_{trip} < V_{CC} < V_{th(UVLO)}$	-	5.4	-	mA
		with auxiliary supply	8	20	40	μA
		in Power-down mode	5	16	20	μA
V_{BR}	breakdown voltage		650	-	-	V
Supply voltage management (V_{CC} pin)						
V_{trip}	trip voltage		0.55	0.65	0.75	V
$V_{startup}$	start-up voltage		21	22	23	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		14	15	16	V
$V_{start(hys)}$	hysteresis of start voltage	during start-up phase	-	300	-	mV
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	6.3	7	7.7	V
$I_{ch(low)}$	low charging current	V_{HV} > 80 V; $V_{CC} < V_{trip}$ or $V_{th(UVLO)} < V_{CC} < V_{startup}$	−1.2	−1.0	−0.8	mA
$I_{ch(high)}$	high charging current	V_{HV} > 80 V; $V_{trip} < V_{CC} < V_{th(UVLO)}$	−4.6	−5.4	−6.3	mA
$I_{CC(oper)}$	operating supply current	no load on the FBDRIVER and PFCDRIVER pins	2.25	3	3.75	mA
Input Voltage Sensing PFC (VINSENSE pin)						
$V_{stop(VINSENSE)}$	stop voltage on the VINSENSE pin		0.85	0.88	0.91	V
$V_{start(VINSENSE)}$	start voltage on the VINSENSE pin		1.11	1.15	1.19	V
$V_{mvc(VINSENSE)max}$	maximum mains voltage compensation voltage on the VINSENSE pin		4	-	-	V
V_{flr}	fast latch reset voltage	active after $V_{th(UVLO)}$ is detected	-	0.75	-	V

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{flr(hys)}$	hysteresis of fast latch reset voltage		-	0.12	-	V
$I_{I(VINSENSE)}$	input current on the VINSENSE pin	$V_{VINSENSE} > V_{stop(VINSENSE)}$ after $V_{start(VINSENSE)}$ is detected	5	33	100	nA
$V_{bst(dual)}$	dual boost voltage	current switch-over point	-	2.2	-	V
		switch-over region	-	200	-	mV
$V_{th(pd)}$	power-down threshold voltage		305	355	405	mV
$V_{hys(pd)}$	power-down hysteresis voltage		55	85	120	mV
Loop compensation PFC (PFCCOMP pin)						
g_m	transconductance	$V_{VOSENSE}$ to $I_{O(PFCCOMP)}$	60	80	100	µA/V
$I_{O(PFCCOMP)}$	output current on the PFCCOMP pin	$V_{VOSENSE}$ = 2 V	33	39	45	µA
		$V_{VOSENSE}$ = 3.3 V	−45	−39	−33	µA
$V_{en(PFCCOMP)}$	enable voltage on the PFCCOMP pin	VINSENSE ≥ $V_{bst(dual)}$		3.5		V
		VINSENSE < $V_{bst(dual)}$		2.5		V
$V_{clamp(PFCCOMP)}$	clamp voltage on the PFCCOMP pin	Low-power mode; PFC off; lower clamp voltage. [1]				
		VINSENSE ≥ $V_{bst(dual)}$	-	3.5	-	V
		VINSENSE < $V_{bst(dual)}$	-	2.5	-	V
		Upper clamp voltage	-	3.9	-	V
$V_{ton(PFCCOMP)zero}$	zero on-time voltage on the PFCCOMP pin		3.4	3.5	3.6	V
$V_{ton(PFCCOMP)max}$	maximum on-time voltage the pin PFCCOMP pin		1.20	1.25	1.30	V
Pulse width modulator PFC						
$t_{on(PFC)}$	PFC on-time	$V_{VINSENSE}$ = 3.3 V; $V_{PFCCOMP} = V_{ton(PFCCOMP)max}$	3.6	4.5	5	µs
		$V_{VINSENSE}$ = 0.9 V; $V_{PFCCOMP} = V_{ton(PFCCOMP)max}$	30	40	53	µs
Output voltage sensing PFC (VOSENSE pin)						
$V_{th(ol)(VOSENSE)}$	open-loop threshold voltage on the VOSENSE pin		-	1.15	-	V
$V_{reg(VOSENSE)}$	regulation voltage on the VOSENSE pin	for $I_{O(PFCCOMP)}$ = 0	2.475	2.500	2.525	V
$V_{ovp(VOSENSE)}$	overvoltage protection voltage on the VOSENSE pin		2.60	2.63	2.67	V
$I_{bst(dual)}$	dual boost current	$V_{VINSENSE} < V_{bst(dual)}$ or $V_{VOSENSE}$ < 2.1 V	-	−8	-	µA
		$V_{VINSENSE} > V_{bst(dual)}$	-	−30	-	nA
Over current protection PFC (PFCSENSE pin)						
$V_{sense(PFC)max}$	maximum PFC sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.49	0.52	0.55	V
		$\Delta V/\Delta t$ = 200 mV/µs	0.51	0.54	0.57	V
$t_{leb(PFC)}$	PFC leading edge blanking time		250	310	370	ns

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{prot(PFCSENSE)}$	protection current on the PFCSENSE pin			–50	-	–5	nA
Soft-start PFC (PFCSENSE pin)							
$I_{start(soft)PFC}$	PFC soft-start current			–75	–60	–45	µA
$V_{start(soft)PFC}$	PFC soft-start voltage	enabling voltage		0.46	0.50	0.54	V
$V_{stop(soft)PFC}$	PFC soft-stop voltage	disabling voltage		0.42	0.45	0.48	V
Oscillator PFC							
$f_{sw(PFC)max}$	maximum PFC switching frequency			-	250	-	kHz
$t_{off(PFC)min}$	minimum PFC off-time			0.8	1.1	1.4	µs
Valley switching PFC (PFCAUX pin)							
$(\Delta V/\Delta t)_{vrec(PFC)}$	PFC valley recognition voltage change with time			-	-	1.7	V/µs
$t_{vrec(PFC)}$	PFC valley recognition time	V_{PFCAUX} = 1 V peak to peak	[2]	-	-	300	ns
		demagnetization to $\Delta V/\Delta t$ = 0	[3]	-	-	50	ns
$t_{to(vrec)PFC}$	PFC valley recognition time-out time			3	4	6	µs
Demagnetization management PFC (PFCAUX pin)							
$V_{th(comp)PFCAUX}$	comparator threshold voltage on the PFCAUX pin			–150	–100	–50	mV
$t_{to(demag)PFC}$	PFC demagnetization time-out time			40	50	60	µs
$I_{prot(PFCAUX)}$	protection current on the PFCAUX pin	V_{PFCAUX} = 50 mV		–75	-	–5	nA
PFC off delay (PFCTIMER pin)							
$I_{source(PFCTIMER)}$	source current on the PFCTIMER pin			-	–5	-	µA
$I_{sink(PFCTIMER)}$	sink current on the PFCTIMER pin	$V_{PFCTIMER}$ = 5 V		-	3.5	-	mA
$V_{start(PFCTIMER)}$	start voltage on the PFCTIMER pin			-	1.27	-	V
$V_{stop(PFCTIMER)}$	stop voltage on the PFCTIMER pin			-	3.6	-	V
Driver (PFCDRIVER pin)							
$I_{src(PFCDRIVER)}$	source current on the PFCDRIVER pin	$V_{PFCDRIVER}$ = 2 V		-	–0.5	-	A
$I_{sink(PFCDRIVER)}$	sink current on the PFCDRIVER pin	$V_{PFCDRIVER}$ = 2 V		-	0.7	-	A
		$V_{PFCDRIVER}$ = 10 V		-	1.2	-	A
$V_{O(PFCDRIVER)max}$	maximum output voltage on the PFCDRIVER pin			9.5	10.8	12	V
OverVoltage Protection flyback (FBAUX pin)							
$I_{ovp(FBAUX)}$	overvoltage protection current on the FBAUX pin			279	300	321	µA

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{cy(ovp)}$	number of overvoltage protection cycles		6	8	12	
Demagnetization management flyback (FBAUX pin)						
$V_{th(comp)FBAUX}$	comparator threshold voltage on the FBAUX pin		60	80	110	mV
$I_{prot(FBAUX)}$	protection current on the FBAUX pin	V_{FBAUX} = 50 mV	−75	-	−5	nA
$V_{clamp(FBAUX)}$	clamp voltage on the FBAUX pin	I_{FBAUX} = −100 μA	−0.85	−0.7	−0.55	V
		I_{FBAUX} = 300 μA	0.79	0.94	1.09	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.5	2	2.5	μs
Pulse width modulator flyback						
$t_{on(fb)min}$	minimum flyback on-time		-	t_{leb}	-	ns
$t_{on(fb)max}$	maximum flyback on-time		32	40	48	μs
Oscillator flyback						
$f_{sw(fb)max}$	maximum flyback switching frequency		100	125	150	kHz
$V_{start(VCO)FBCTRL}$	VCO start voltage on the FBCTRL pin		1.3	1.5	1.7	V
$f_{sw(fb)swon(PFC)}$	PFC switch-on flyback switching frequency		-	86	-	kHz
$f_{sw(fb)swoff(PFC)}$	PFC switch-off flyback switching frequency		-	48	-	kHz
$\Delta V_{VCO(FBCTRL)}$	VCO voltage difference on the FBCTRL pin		-	−0.12	-	V
Peak current control flyback (FBCTRL pin)						
V_{FBCTRL}	voltage on the FBCTRL pin	for maximum flyback peak current	1.85	2	2.15	V
$V_{to(FBCTRL)}$	time-out voltage on the FBCTRL pin	enable voltage	-	2.5	-	V
		trip voltage	4.2	4.5	4.8	V
$R_{int(FBCTRL)}$	internal resistance on the FBCTRL pin		-	3	-	kΩ
$I_{O(FBCTRL)}$	output current on the FBCTRL pin	V_{FBCTRL} = 0 V	−1.4	−1.19	−0.93	mA
		V_{FBCTRL} = 2 V	−0.6	−0.5	−0.4	mA
$I_{to(FBCTRL)}$	time-out current on the FBCTRL pin	V_{FBCTRL} = 2.6 V	−36	−30	−24	μA
		V_{FBCTRL} = 4.1 V	−34.5	−28.5	−22.5	μA
Valley switching flyback (HV pin)						
$(\Delta V/\Delta t)_{vrec(fb)}$	flyback valley recognition voltage change with time		−75	-	+75	V/μs
$t_{d(vrec-swon)}$	valley recognition to switch on delay time	[4]	-	150	-	ns
Soft-start flyback (FBSENSE pin)						
$I_{start(soft)fb}$	flyback soft-start current		−75	−60	−45	μA
$V_{start(soft)fb}$	flyback soft-start voltage	enable voltage	0.55	0.63	0.70	V

Table 5. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overcurrent protection flyback (FBSENSE pin)						
$V_{sense(fb)max}$	maximum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.61	0.65	0.69	V
		$\Delta V/\Delta t$ = 200 mV/µs	0.64	0.68	0.72	
$V_{sense(fb)min}$	minimum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.305	0.325	0.345	V
$t_{leb(fb)}$	flyback leading-edge blanking time		255	305	355	ns
$I_{adj(FBSENSE)}$	adjust current on the FBSENSE pin		−3.2	−3	−2.8	µA
Overpower protection flyback (FBSENSE pin)						
$V_{sense(fb)max}$	maximum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs				
		I_{FBAUX} = 80 µA	0.61	0.65	0.69	V
		I_{FBAUX} = 120 µA	0.57	0.62	0.67	V
		I_{FBAUX} = 240 µA	0.47	0.52	0.57	V
		I_{FBAUX} = 360 µA	0.41	0.46	0.51	V
Driver (FBDRIVER pin)						
$I_{src(FBDRIVER)}$	source current on the FBDRIVER pin	$V_{FBDRIVER}$ = 2 V	-	−0.5	-	A
$I_{sink(FBDRIVER)}$	sink current on the FBDRIVER pin	$V_{FBDRIVER}$ = 2 V	-	0.7	-	A
		$V_{FBDRIVER}$ = 10 V	-	1.2	-	A
$V_{O(FBDRIVER)(max)}$	maximum output voltage on the FBDRIVER pin		9.5	10.8	12	V
LATCH input (LATCH pin)						
$V_{prot(LATCH)}$	protection voltage on the LATCH pin		1.23	1.25	1.27	V
$I_{O(LATCH)}$	output current on the LATCH pin	$V_{prot(LATCH)} < V_{LATCH} < V_{oc(LATCH)}$	−85	−80	−75	µA
$V_{en(LATCH)}$	enable voltage on the LATCH pin	at start-up	1.30	1.35	1.40	V
$V_{hys(LATCH)}$	hysteresis voltage on the LATCH pin	$V_{en(LATCH)} - V_{prot(LATCH)}$	80	100	140	mV
$V_{oc(LATCH)}$	open-circuit voltage on the LATCH pin		2.65	2.9	3.15	V
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C
$T_{pl(IC)hys}$	hysteresis of IC protection level temperature		-	10	-	°C

[1] For a typical application with a compensation network on pin PFCCOMP, like the example in Figure 3.

[2] Minimum required voltage change time for valley recognition on pin PFCAUX.

[3] Minimum time required between demagnetization detection and $\Delta V/\Delta t$ = 0 on pin PFCAUX.

[4] Guaranteed by design.