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Geelead Technology Limited
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采购部

FAIRCHILD
SEMICONDUCTOR®

February 2004

FDS4080N3

40V N-Channel FLMP PowerTrench® MOSFET

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low $R_{DS(ON)}$ in a small package.

Applications

- Synchronous rectifier
- DC/DC converter

Features

- 13 A, 40 V $R_{DS(ON)}$ = 10.5 mΩ @ V_{GS} = 10 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Fast switching (Qg = 30 nC)
- FLMP SO-8 package: Enhanced thermal performance in industry-standard package size

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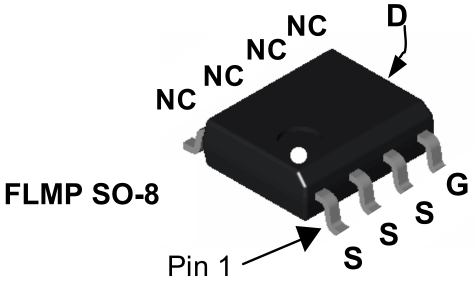
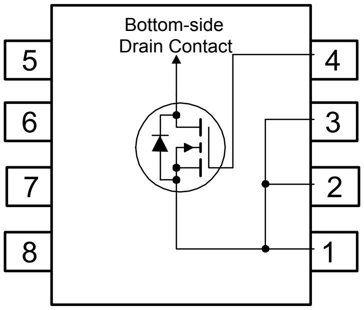




Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current – Continuous	(Note 1a)	13	A
	– Pulsed		60	
P_D	Power Dissipation for Single Operation	(Note 1a)	3.0	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Ambient		0.5	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4080N3	FDS4080N3	13''	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

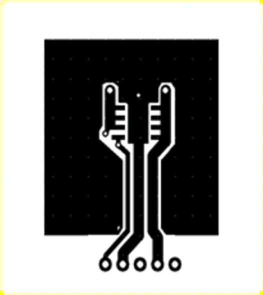
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
E_{AS}	Drain-Source Avalanche Energy	Single Pulse, V_{DD} = 10V, I_D=13A			200	mJ
I_{AS}	Drain-Source Avalanche Current				13	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		44		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V ,V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2	3.9	5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–8		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 10 V, I_D = 13 A, T_J=125°C		8.5 12.5	10.5 22	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A		41		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1.0 MHz		1750		pF
C_{oss}	Output Capacitance			357		pF
C_{rss}	Reverse Transfer Capacitance			138		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 20 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	21	ns
t_r	Turn–On Rise Time			8	17	ns
$t_{d(off)}$	Turn–Off Delay Time			29	46	ns
t_f	Turn–Off Fall Time			14	25	ns
Q_g	Total Gate Charge	V_{DS} = 20 V, I_D = 13 A, V_{GS} = 10 V		30	40	nC
Q_{gs}	Gate–Source Charge			9		nC
Q_{gd}	Gate–Drain Charge			10		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.2 A (Note 2)		0.7	1.2	V

Electrical Characteristics

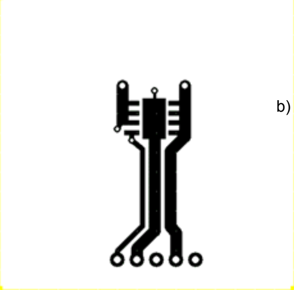
T_A = 25°C unless otherwise noted

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 49°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 85°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

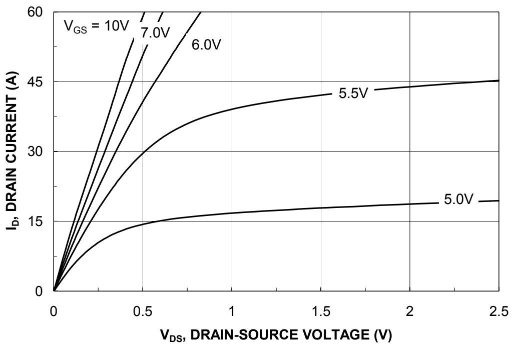


Figure 1. On-Region Characteristics.

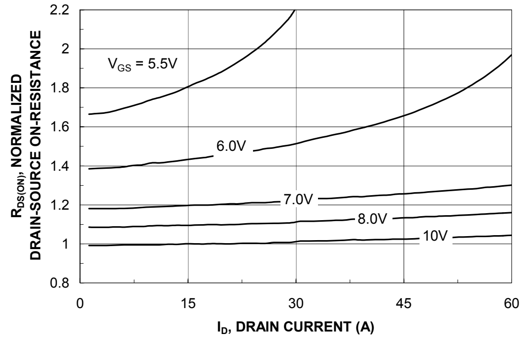


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

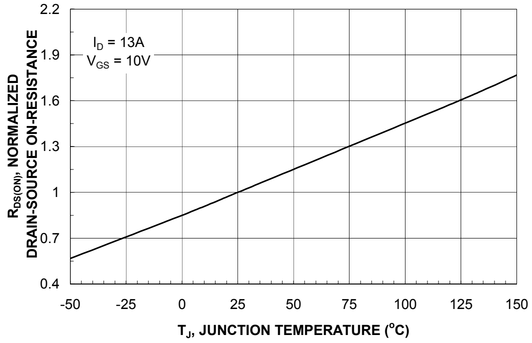


Figure 3. On-Resistance Variation withTemperature.

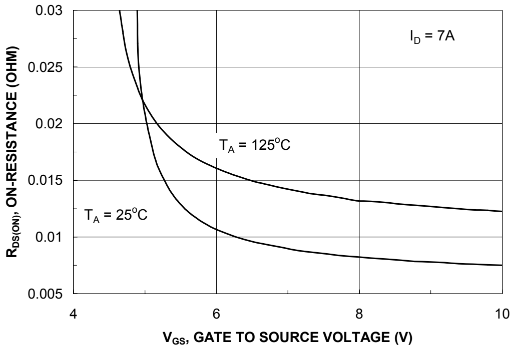


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

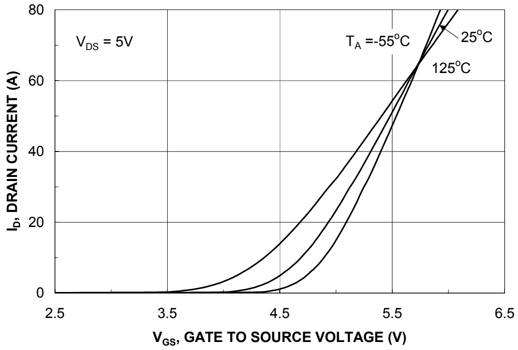


Figure 5. Transfer Characteristics.

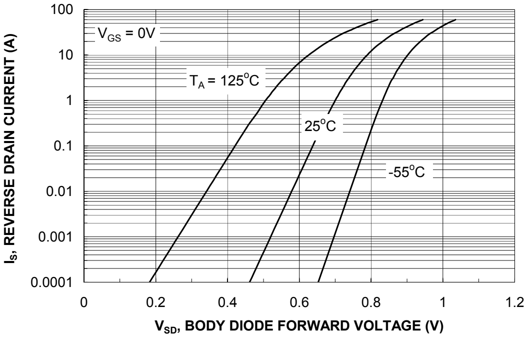


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

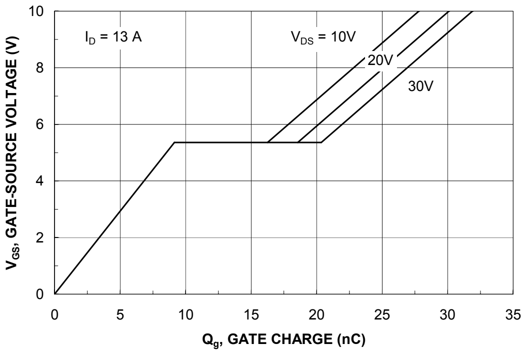


Figure 7. Gate Charge Characteristics.

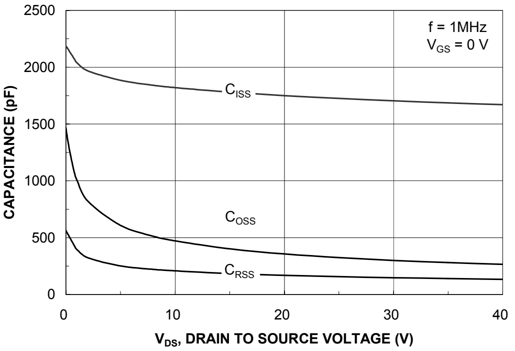


Figure 8. Capacitance Characteristics.

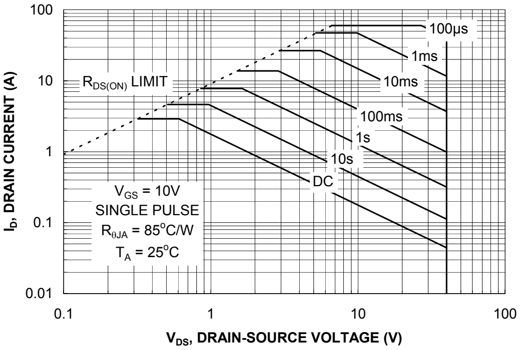


Figure 9. Maximum Safe Operating Area.

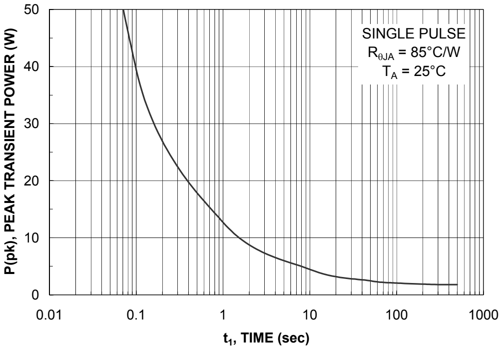


Figure 10. Single Pulse Maximum Power Dissipation.

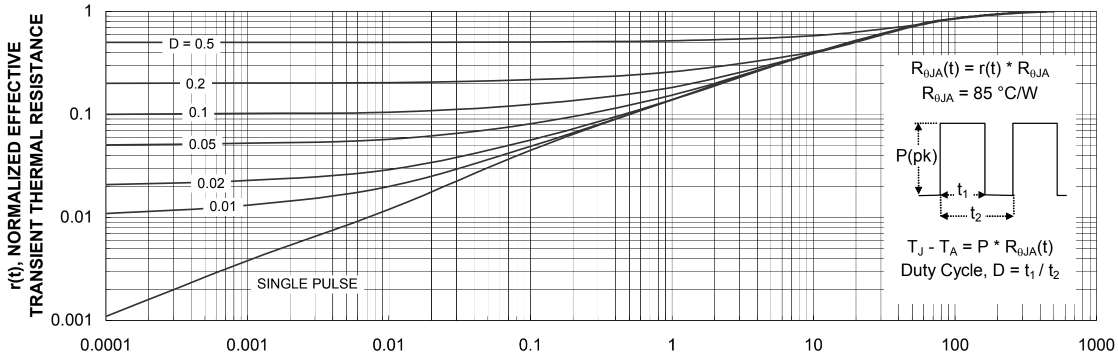
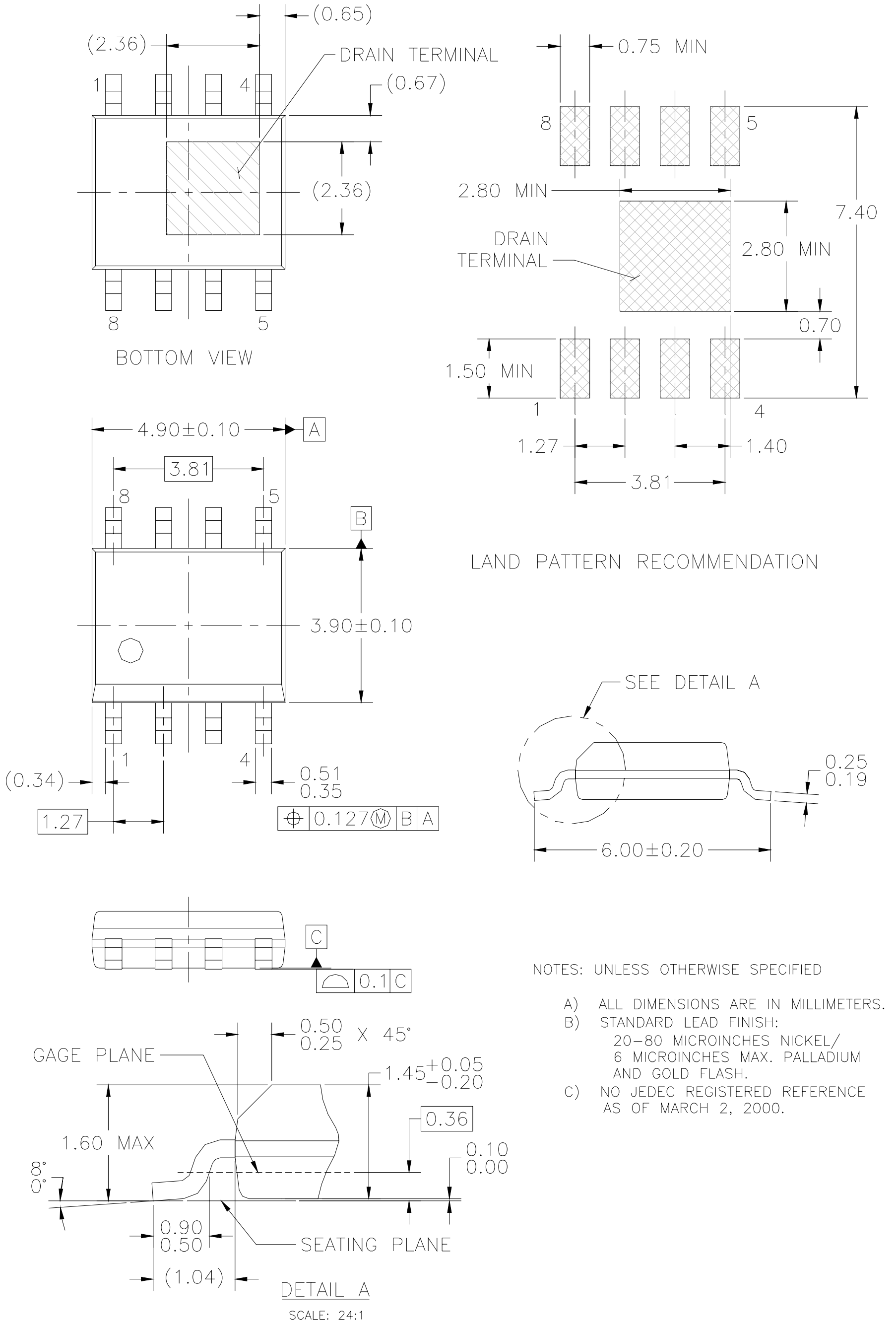


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) STANDARD LEAD FINISH:
20–80 MICROINCHES NICKEL/
6 MICROINCHES MAX. PALLADIUM
AND GOLD FLASH.

C) NO JEDEC REGISTERED REFERENCE
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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