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ISL6560/62 Evaluation Board

Application Note | **April 2002** | **AN1009.0**

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Introduction

The ISL6560/62 Evaluation Board was designed to accommodate either the ISL6560 or the ISL6562 power supply controller ICs. CORE voltage is set by a five bit DAC that is usually programmed by the microprocessor. For this board, DAC codes are entered via a five position dip switch. Power supply input voltages may be applied through three banana posts or an ATX connector on the board. With an ATX supply the main input voltage to the converter is 5V. The ATX 12V supply powers the ISL6560/62, the HIP6601 gate drivers and the transient load generator. A toggle switch is provided on the board to enable the ATX supply.

Converter input voltage via the banana connectors can range from 5V to 12V. A separate connector supplies 12V to the ISL6560/62, transient load generator and the gate drivers as described above.

Figure 1 shows the Evaluation Board. Note the ATX connector at the top of the board. The ATX power switch SW2, is located to the right of the connector.

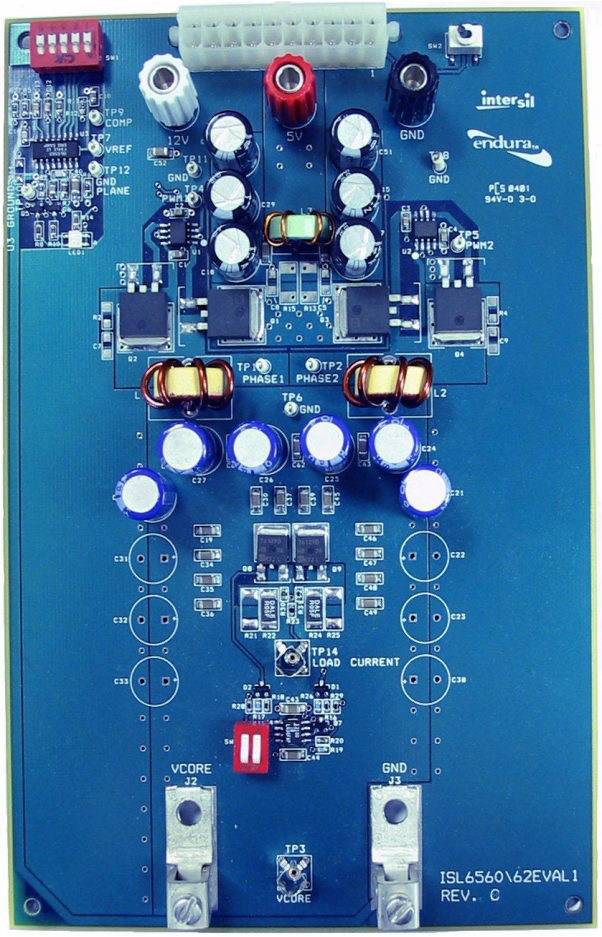


FIGURE 1. EVALUATION BOARD

Description

This board was design so that a wide range of input voltages could be used. Burndy binding posts at the lower end of the board provide the high current connections for the output load.

Just above the output connectors is a pulse generator to provide 40A transient loading to verify response to pulse loading of the supply. Scope probe connectors monitor the current pulse, and output voltage.

Extra output capacitor locations are available to modify the output capacitor configuration or type of capacitors. 22µF ceramic capacitors accompany the bulk electrolytic capacitors. In an application where the supply is connected to an active load, high frequency capacitors should be located as close as possible to the load to help reduce undesired transient voltage changes at the load.

The ISL6560/62 is located on the left side of the board. Immediately below the controller IC is the POWER GOOD monitoring circuit. A dual RED-GREEN LED indicator is green when the CORE voltage is within the defined data sheet limits. Figure 13 shows a schematic diagram of the POWER GOOD monitoring circuit.

ISL6560 and ISL6562

Figure 2 shows a simplified functional block diagram of these devices, outlining the major differences between the two ICs.

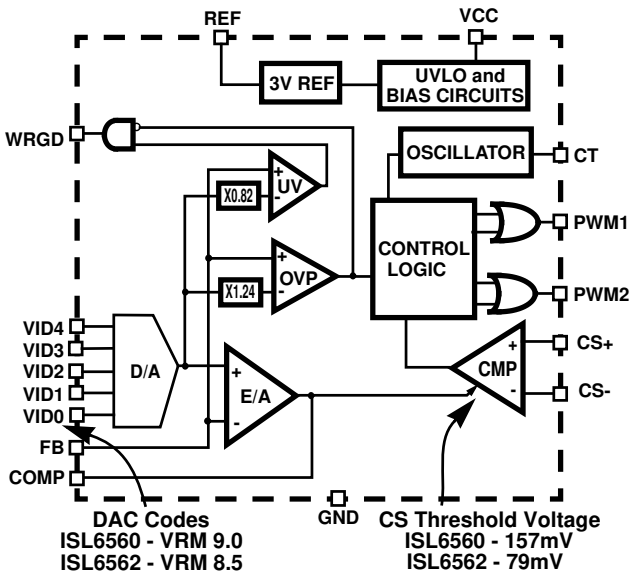


FIGURE 2. SIMPLIFIED BLOCK DIAGRAM SHOWING MAJOR DEVICE DIFFERENCES

The ISL6560 has a DAC scaled for VRM9.0 codes while the ISL6562's DAC is set to VRM8.5 codes. The other major difference is the Current Comparator threshold voltage.

The typical threshold voltage for the ISL6560 is 157mV while the ISL6562 is more sensitive and has a threshold voltage of 79mV.

Figure 3 shows the Current Comparator threshold voltage versus the COMP voltage.

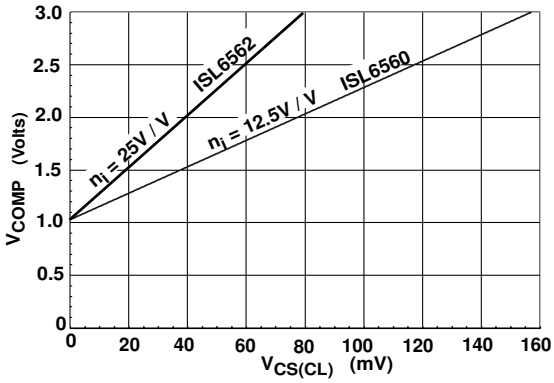


FIGURE 3. CURRENT COMPARATOR THRESHOLD VOLTAGE AS A FUNCTION OF V_{COMP}

Oscillator

An oscillator drives a divider that reduces the channel frequency to one half of the oscillator. Each channel is initiated by the oscillator and terminated by the current comparator. A maximum duty cycle of 50% is established by this arrangement.

Power Good

Operation of the controller is monitored by the Power Good circuitry which controls an open drain N-Channel MOS transistor. When the CORE voltage is outside the 82% and 124% limits, the MOSFET pulls down an external load. Over voltage switches both upper PWM power MOSFETs OFF and pulls down the lower output power MOSFETs to protect the load.

Over Current

Over current is detected by the output voltage dropping below the under voltage limit. This results in several occurrences. First the Current Comparator limit is reduce to 95mV from 157mV for the ISL6560 and 47mV from 79mV for the ISL6562. This effectively folds back the current, while the CORE voltage is now set to a lower limit of 400mV to 500mV. Moreover, the oscillator frequency is reduce to about one fifth of its normal operating value by reducing the oscillator charging current to 36µA from its normal operating value of 150µA.

Converter Disable

To disable the converter, the COMP terminal may be pulled to ground with a NPN transistor, N-Channel MOS transistor or a switch. This device should be located next the COMP pin to reduce the possibility of external pickup by the pin. The oscillator is disabled when the COMP voltage drops below 0.56V for the ISL6560 and 0.64V for the ISL6562. Minimum current for the pull down device should be 2mA. The COMP terminal is brought out as a test point on the Evaluation Board. A ground terminal and the 3V Reference terminal are located near the COMP terminal on the Evaluation Board.

ISL6562 On The Board

As explained earlier the board is designed to be used with either the ISL6560 or the ISL6562. The boards are usually shipped with the ISL6560. Boards populated with the ISL6562 have an additional 5mΩ resistor placed in the R15 location.

Evaluation Board Quick Start

To aid in getting the board functioning as quickly as possible, a sheet similar to Figure 4 is included with each board. This shows the location of all pertinent parts and test points.

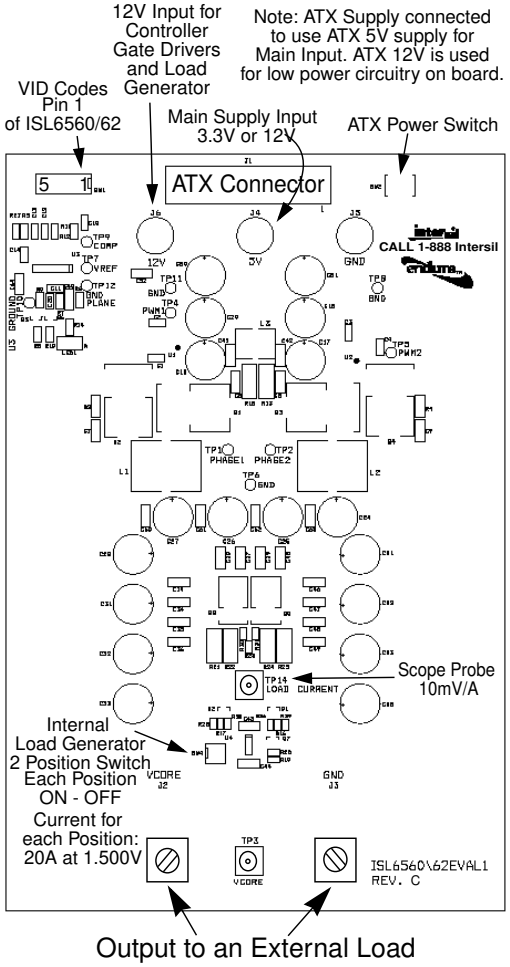


FIGURE 4. PERTIENT POINTS ON ISL6560/62 EVALUATION BOARD

Transient Load Generator

Probably one of the most interesting tests for a regulator system is the transient load. From this single test one can access voltage droop, loop stability and the regulator's response to load changes going from no load to full load and the recovery after rapid load removal. To quickly determine these characteristics, a pulse load generator is incorporated on the evaluation board. A current load pulse at about 20A per position at 1.5V output is activated with two slide switches. A scope probe connector is provided to monitor the current pulse and is calibrated to read 10mV/A. Figures 5, 6, and 7 show the transient response of the Evaluation Board with 12V input, operating with the internal load generator which provides slightly over a 40A load step. For all scope shots: Top trace is PWM 1 output, next is V_{COMP} at 1V/div. Center trace is V_{CORE} at 50mV/div and the lower trace is the load current at 20A/div. DAC set to 1.500V.

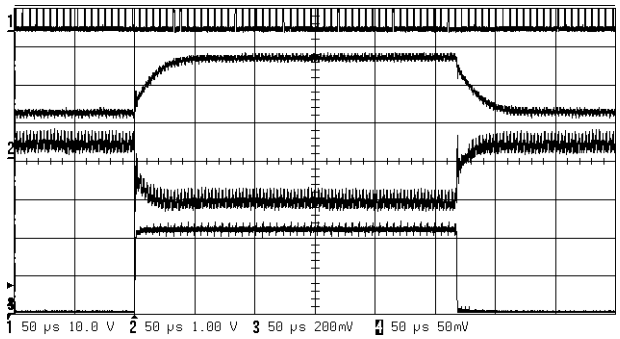


FIGURE 5. 44A TRANSIENT CURRENT PULSE

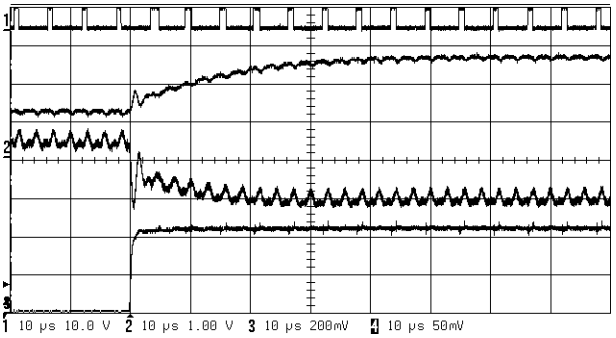


FIGURE 6. EXPANDED FRONT EDGE OF CURRENT PULSE

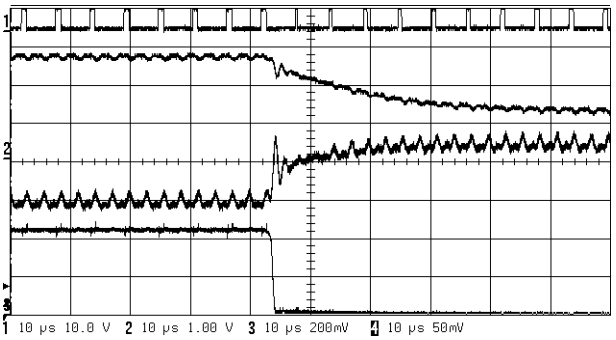


FIGURE 7. EXPANDED BACK EDGE OF CURRENT PULSE

Efficiency

Figures 8 and 9 show the efficiency of the converter with CORE voltage at the two extremes of the DAC voltage and at 1.500V, near the middle of the range. The curves show 12V input and 5V input. Note the improvement in efficiency as the output voltage approaches the input voltage, with increasing duty cycle.

Snubber Networks

Snubbers are not used in this design, but pad locations and connections to PHASE and ground are provided by R2 - C7 for PHASE 1 and R4 - C9 for PHASE 2.

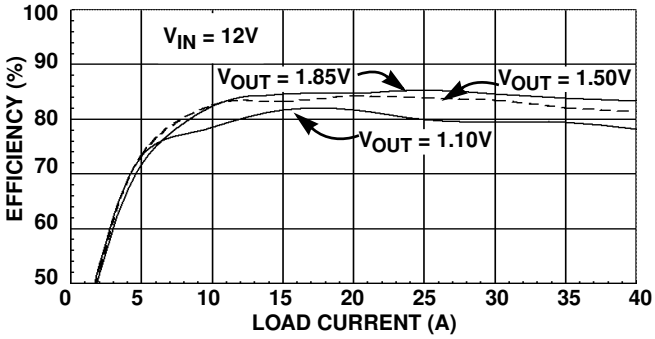


FIGURE 8. 12V INPUT EFFICIENCY AT DAC EXTREMES

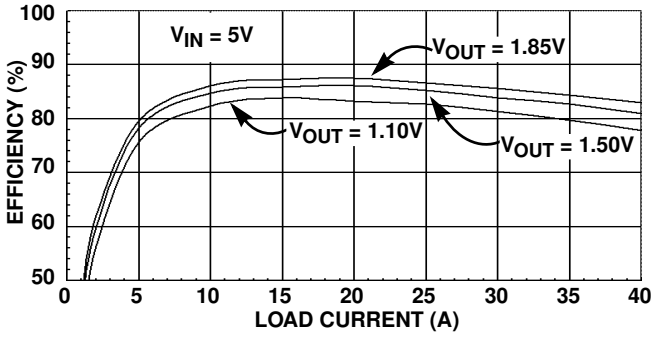


FIGURE 9. 5V INPUT EFFICIENCY AT DAC EXTREMES

PC Board Schematic

Figure 11 shows the main schematic. The Power Good indicator circuit is shown in figure 13. Figure 12 shows the schematic of the transient load generator.

The layout is shown in Figures 14 and 15, starting with the silk screen in Figure 14. The Bill of Material is shown in Table 1. Following the Bill of Materials is quick design guide.

PC Board Layout Considerations

Like all high current supplies where low voltage control signals in the millivolt range must live with high voltage, high current switching signals, PC board layout becomes crucial in obtaining a satisfactory supply.

Figure 10 shows a simplified diagram highlighting the critical areas of a PC board layout. This diagram and the following material represent goals to work towards during the layout phase. Goals will be compromised during the layout process due to component placement and space constraints. The following text reviews these layout considerations in more detail.

Current Sampling

1. Place the current sampling or sense resistor as close as possible to the upper MOSFET drains. This is important since the added inductance and resistance increase the impedance and result in a reduction in drain voltage during high peak pulse currents.

2. Current sense is critical, especially at lower current levels where the current comparator threshold voltage is lower. A good Kelvin connection requires that the voltage sample must be taken at the R_{SENSE} resistor ends and not at the planes that the resistor is connected.

3. The lines to the current sense resistor should be parallel and run away from the PHASE or PWM signals to prevent coupling of spikes to the current comparator input that may delay or advance triggering of the comparator. Parallel routing will work towards equal exposure for both lines, so that the comparator common mode rejection characteristic will reduce the influence of coupled noise.

4. Place the current sense filter network near the controller. This will help reduce extraneous inputs to the comparator.

Voltage Sampling

1. To obtain optimum regulation use the Kelvin connection for the output voltage sample as shown on the Functional System Schematic Diagram of Figure 10. The ground connection, pin 9 of the ISL6560 should be connected to the system ground at the load.

2. The two voltage sampling lines described in item 1 above should also be routed away from any high current or high pulse voltages such as the phase lines or pads. Doing this will reduce the possibility of coupling undesired pulses into the feedback signal and either modifying the output of the error amplifier or, if of sufficient amplitude, spuriously triggering the current comparator by readjusting the threshold voltage.

Other Considerations

1. Keep the leads to the timing capacitor connected to pin CT short and return the ground directly to pin 9.

2. When using a transistor to disable the converter by pulling the CT pin to ground, place the transistor close to the CT pin to minimize extraneous signal pickup.

3. As in all designs, keep decoupling networks near the pins that must be decoupled. For example, the decoupling/filter network on the FB input shown below. The series resistor should be located next to the FB pin.

4. Large power and ground planes are critical to keeping performance and efficiency high. Consider a 1mΩ resistance in a 40A supply line. With 1.8V output, this results in slightly over 2% power loss in a 72W supply.

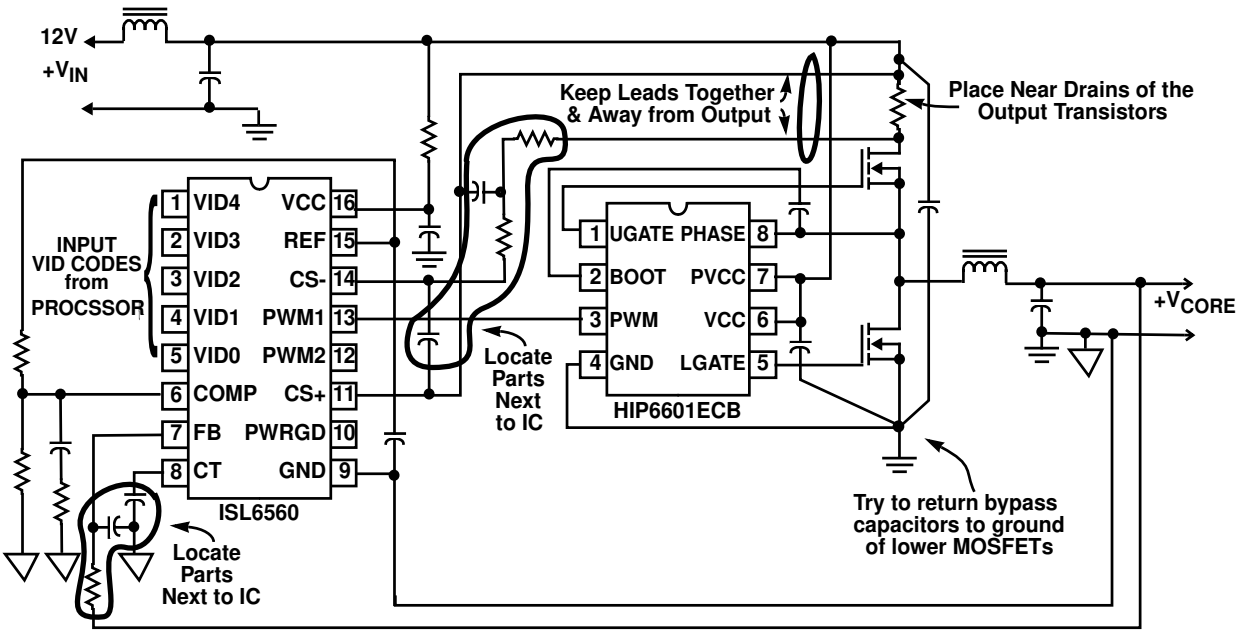


FIGURE 10. SCHEMATIC DIAGRAM SHOWING ONLY ONE CHANNEL OF "IDEAL" COMPONENT PLACEMENT

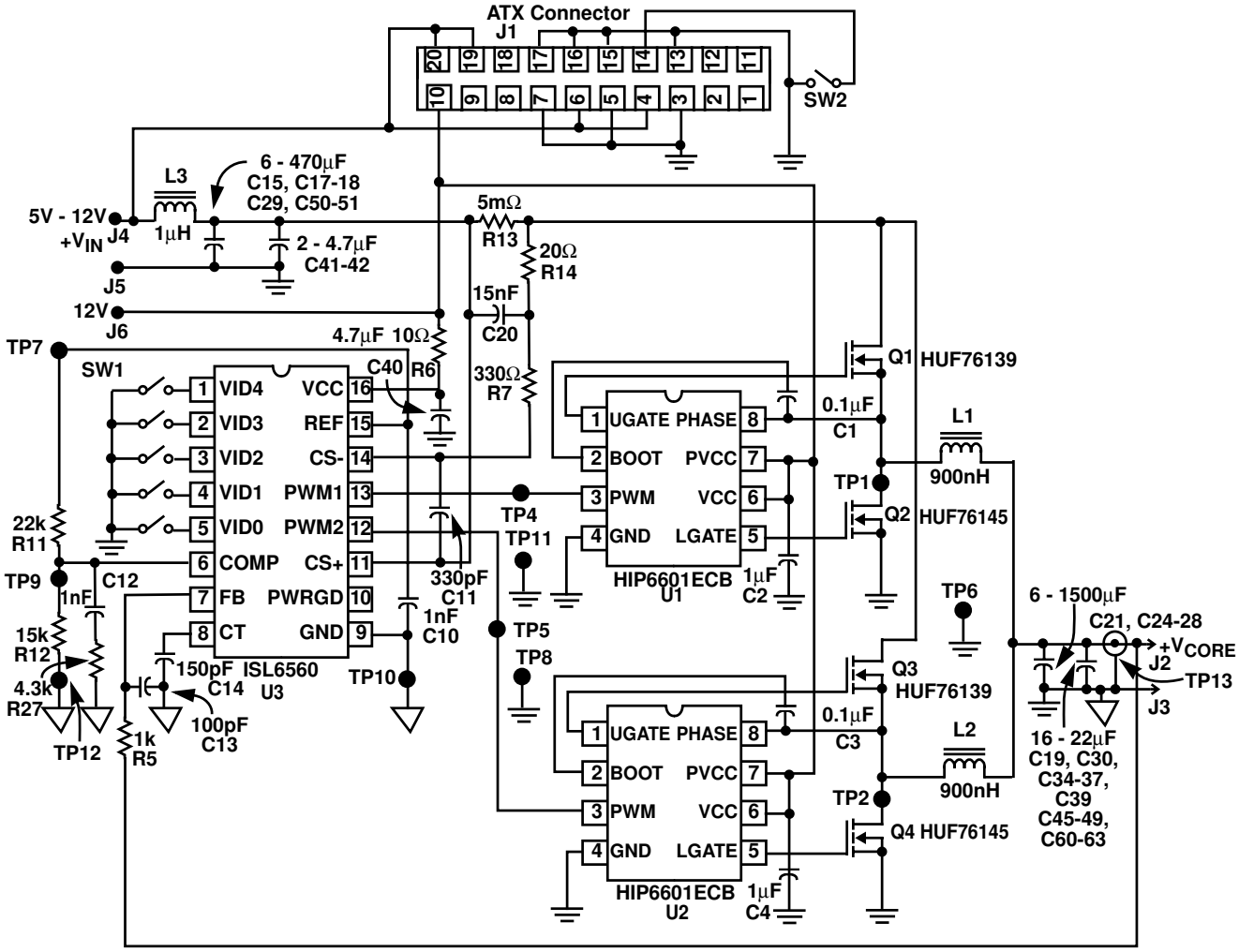


FIGURE 11. SCHEMATIC DIAGRAM OF A 40A SUPPLY USING THE ISL6560 CONTROLLER AND HIP6601 GATE DRIVERS

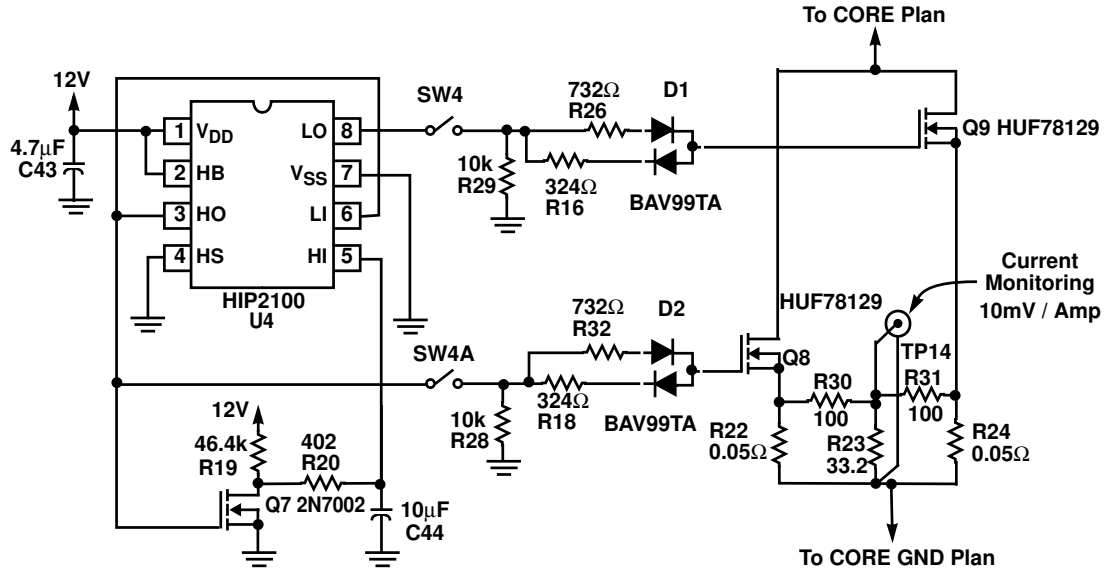


FIGURE 12. SCHEMATIC DIAGRAM OF THE 40A PULSE GENERATOR ON THE POWER SUPPLY BOARD

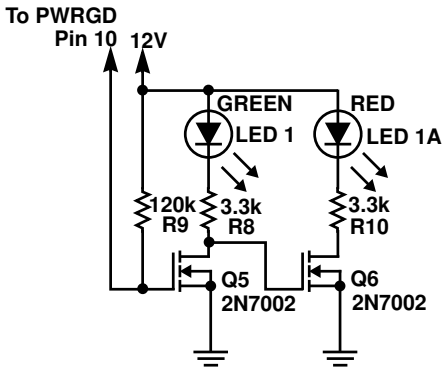


FIGURE 13. SCHEMATIC DIAGRAM OF THE POWER GOOD MONITORING CIRCUIT

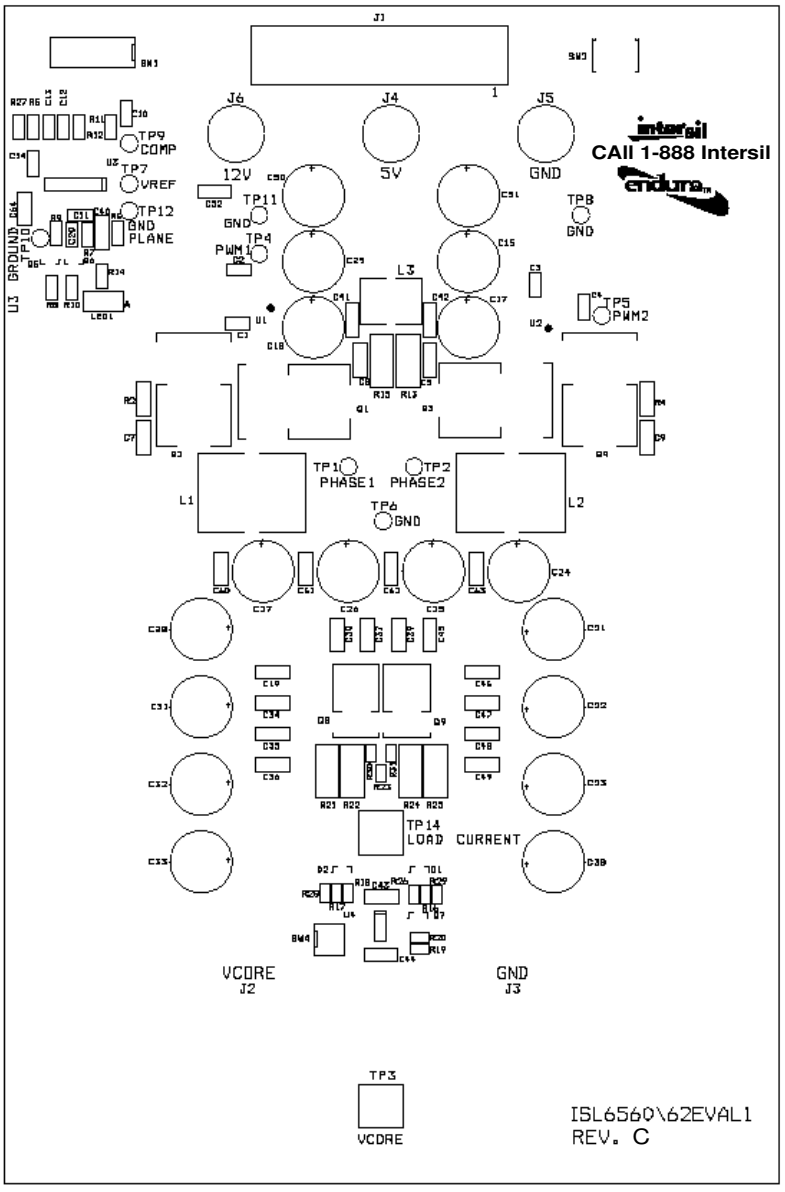


FIGURE 14. SILK SCREEN

FIGURE 15A. TOP COPPER

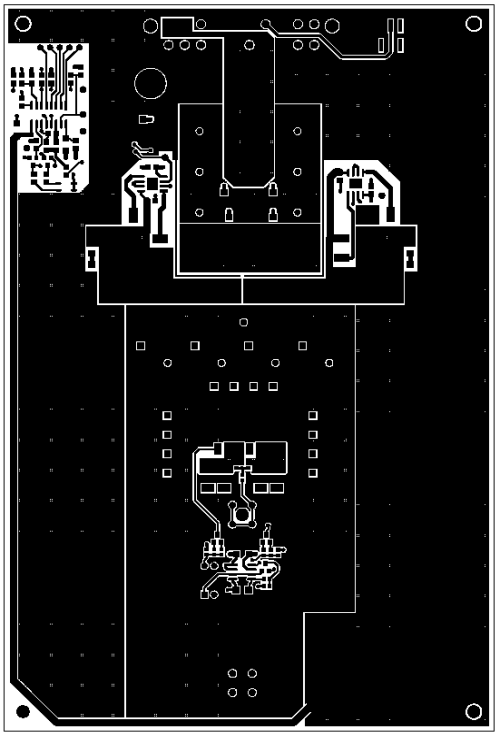


FIGURE 15B. GROUND PLAN

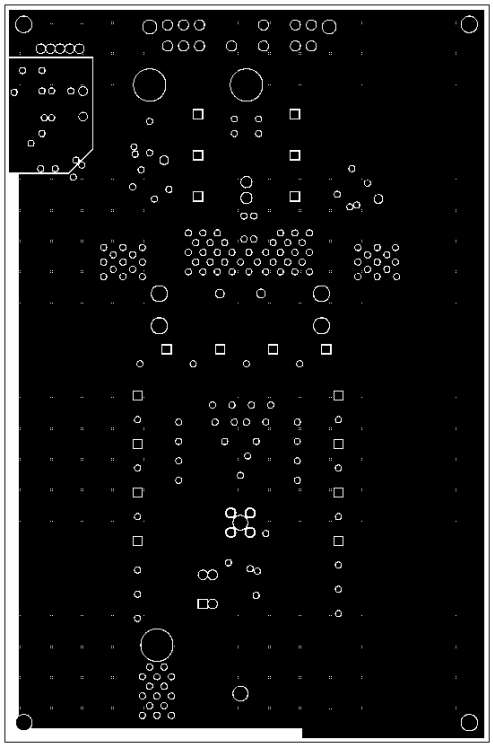


FIGURE 15C. POWER PLAN

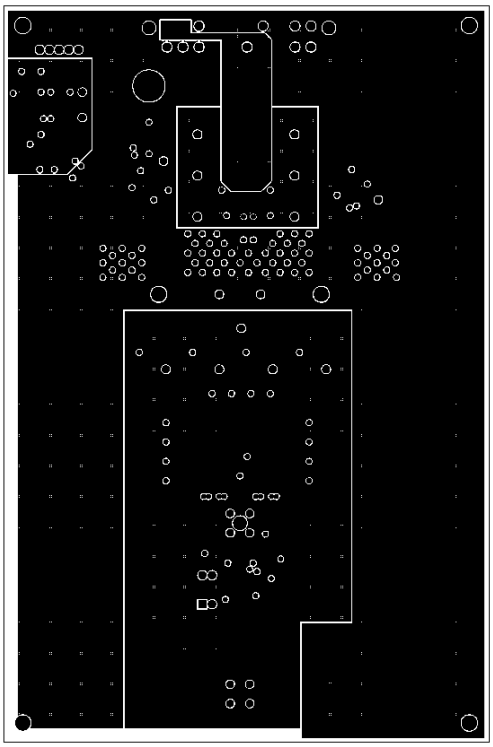
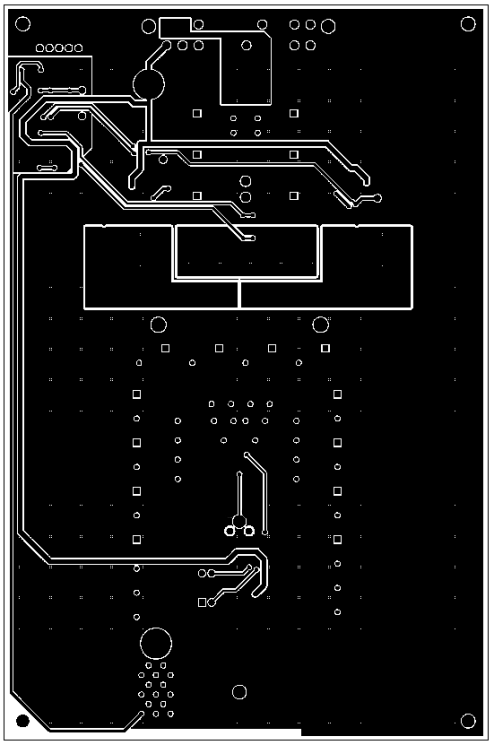


FIGURE 15D. BOTTOM COPPER



FIGURES 15A-D. Showing ALL FOUR LAYERS OF THE PC BOARD

TABLE 1. Bill of Materials

Quantity	Reference	Part	PCB Footprint	Vendor	Part Number
2	C1,C3	0.1uF, 25V, X7R Ceramic	P0805	Various	
2	C2,C4	1uF, 25V, X7R Ceramic	P0805	Various	
2	C5,C8,	Not Populated	P1206		
2	C7,C9	Not populated	P1206		
2	C10, C12	1nF, 25V, X7R Ceramic	P0805	Various	
1	C11	330pF, 5%, 25V, NPO Ceramic	P0805	Various	
1	C13	100pF, 5%, 25V, NPO Ceramic	P0805	Various	
1	C14	150pF, 5%, 25V, NPO Ceramic	P0805	Various	
6	C15,C17,C18,C29,C50,C51	470uF, 16V	10x16	Rubycon	16ZA470-10x16
16	C19,C30,C34,C35,C36,C37, C39,C45,C46,C47,C48,C49, C60,C61,C62,C63	22uF, 6.3V, X5R Ceramic	P1206	Various	
1	C20	15nF, 10%, 25V, X7R Ceramic	P0805	Various	
6	C21,C24,C25,C26,C27,C28	1500uF, 4V	10x20	Sanyo OS CON	4SP1500M
6	C22,C23,C38,C31,C32,C33	Not Populated	10x20		
5	C40,C41,C42, C43, C52	4.7uF,16V, Y5V Ceramic	P1206	Various	
1	C44	10uF, 10%, 6.3V, X5R Ceramic	P1206	Various	
1	C64	Not Populated	P1206		
2	D1,D2	BAV99LT1	SM/SOT23_123	ZETEX	BAV99TA
1	J1	ATX CONNECTOR	ATX/CONN/20P	Molex or Jameco	39-29-9202 147379
2	J3,J2	LUG	BINDING/POST_2	Burndy	KPA8CTP
1	J4	Red Binding Post	Post	Johnson	111-0702-001
1	J5	Black Binding Post	Post	Johnson	111-0703-001
1	J6	White Binding Post	Post	Johnson	111-0701-001
1	LED1	GREEN / RED	SMT/3MM/2.5MM/4LEAD	Panasonic	LN2162C13-(TR)
2	L1,L2	600nH 5T, AWG14	250WD/700LN	Micrometals	T60-8/90
1	L3	1uH 5T, AWG19	128WD/307OD	Micrometals	T50-52
2	Q1,Q3	HUF76139	TO263AB_M	Fairchild	
2	Q2,Q4	HUF76145	TO263AB_M	Fairchild	
3	Q5, Q6, Q7	2N7002	SM/SOT23_123	Various	
2	Q9,Q8	HUF76129D3S	TO252AA/DPAK	Fairchild	
2	R2,R4	Not populated	P1206		
1	R5	1K, 5%	P0805	Various	
1	R6	10Ω, 5%	P0805	Various	

TABLE 1. Bill of Materials (contiued)

1	R7	330Ω, 5%	P0805	Various	
2	R10,R8	3.3K, 5%	P0805	Various	
1	R9	120K, 5%	P0805	Various	
1	R11	22K, 5%	P0805	Various	
1	R12	15K, 5%	P0805	Various	
1	R13	5mΩ, 1%	P2512	Panasonic	ERJM1WSF5M0U, 0.005 1%
1	R15	5mΩ, 1% for ISL6562 only	P2512 Not populated. Only populated for ISL6562 operation	Panasonic	ERJM1WSF5M0U, 0.005 1%
1	R14	20Ω, 5%	P0805	Various	
2	R16,R18	324Ω, 1%	P0603	Various	
2	R26,R17	732Ω, 1%	P0603	Various	
1	R19	46.4k, 1%	P0603	Various	
1	R20	402 1%	P0603	Various	
2	R21, R25	Not Populated	P2512		
2	R22, R24	50mΩ, 1%	P2512	Vishay	WSL2512, 0.05 1%
1	R23	33.2Ω, 1%	P0603	Various	
1	R27	4.3K, 5%	P0805	Various	
2	R28, R29	10K, 5%	P0603	Various	
2	R30, R31	100Ω, 1%	P0603	Various	
1	SW1	SW DIP-5	DIPSW.100/10/W.300/L.550	CTS	2085
1	SW2	DPST	DPST_SWITCH	CK	GT11MSCK
1	SW4,SW4A	SW DIP-2	SPST_SWITCHs	Grayhill	76SB02
11	TP1,TP2,TP4,TP5,TP6,TP7 TP8,TP9,TP10,TP11,TP12,	TEST POINTS	TP	Keystone	5002
3	TP3, TP14	Test Probe	TP\PROBE-SOCKET	Tektronix	131-4353-00
2	U1,U2	HIP6601ECB	8L\EPAD\SOIC	Intersil	
1	U3	ISL6560/62 Using an ISL6562 - Populate R15 with resistor	16L\SOIC	Intersil	
1	U4	HIP2100	8L\SOIC	Intersil	
1	PC Board	4 layers	2 0z Copper	Various	

ISL6560 Supply Design Sequence

The ISL6560 data sheet describes in more detail the following equations. There are several changes from the computations in the body of the data sheet. First, an operating frequency of 400kHz was chosen. Next, this design sequence shows the method of setting the initial no load voltage at the DAC setting and offsetting the no load voltage 15mV above the programmed DAC voltage.

A. Specifications:

Output Current: 40A
Input Voltage: 12V
Output Voltage: VDAC + 15mV
Output Voltage for Calculations:
V_{DAC} = 1.8V + 15mV
Droop Voltage: 65mV
Oscillator Frequency: 400kHz (f_{SW})

B. Calculate R_{OUT}:

$$R_{OUT} = \frac{V_{DROOP}}{I_{OUT}} = \frac{65mV}{40A} = 1.63m\Omega$$

C. Determine Frequency Setting Capacitor CT:.

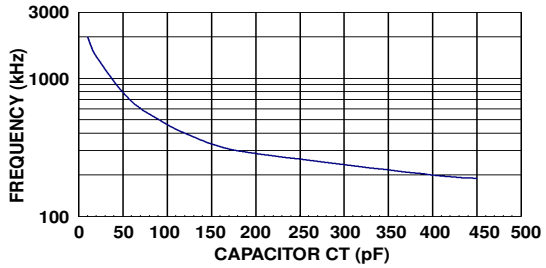


FIGURE A. OSCILLATOR FREQUENCY vs. TIMING CAPACITOR

From curve above, for 400kHz use 120pF.

D. Select Inductor Ripple Current (ΔI_L):

Choose 40% of IOUT

$$\Delta I_L = 40A \times 0.4 = 16A$$

Or 8A / Channel

E. Determine the Inductors:

$$L = \frac{V_{IN} - V_{OUT}}{\frac{f_{SW}}{2} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}} = \frac{12V - 1.8V}{200kHz \times 8A} \times \frac{1.8V}{12V}$$

$$= 956nH$$

F. Output Capacitors:

$$Capacitor_{ESR} \cong R_{OUT} = 1.63m\Omega$$

Sonya 1500µF, 4V OS-CON Capacitors
have an ESR < 10mΩ
Six capacitors < 1.66mΩ
Total Capacitance = 9mF

G. Input Capacitor's RMS Current:

Use the curve of Figure B

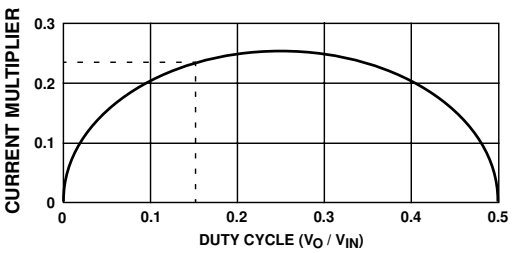


FIGURE B. CURRENT MULTIPLIER vs. DUTY CYCLE

For 40A with a duty cycle (D) of:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{1.8V}{12V} = 0.15$$

The multiplier from Figure B is 0.24.

$$I_{RMS} = 0.24 \times 40A = 9.6A$$

Pensioned 470µF, 16V Rubdown ZA series capacitors have a RMS current rating of 1.6A.

Six capacitors were selected.

H. Current Sense Resistor (R_{SENSE}):

$$R_{SENSE} = \frac{V_{CS(TH)MIN}}{\frac{I_{OUT}}{2} + \frac{I_{RIPPLE}}{2}} = \frac{142mV}{20A + 8A} = 5.07m\Omega$$

Use a 5mΩ resistor

I. R_{SENSE} Dissipation:

$$I_{RMS} = I_{PEAK}\sqrt{D}$$

$$\therefore Power = I_P^2 \times D \times R_{SENSE}$$

Where: I_P = 20A + 4A = 24A (Using half 0f ripple current

$$Power = 24A^2 \times 0.15 \times 5m\Omega$$

$$= 432mW$$ Used a 1W resistor

J. R_L Selection:

$$R_L = \frac{ni \times R_{SENSE}}{gm \times R_{OUT} \times 2} = \frac{12.5 \times 5m\Omega}{2.2mS \times 1.63m\Omega \times 2} = 8.7k\Omega$$

ni = ΔV_{COMP} / V_{CS} (from data sheet)

am Amplifier Gain = gm × RL = 2.2mS × 8.7k = 19.1

K. V_{SET} Computation for No Load Voltage = DAC:

V_{OUT}, the no load voltage programed to the DAC voltage

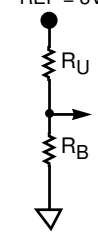
V_{SET}, the voltage set at the COMP pin

$$VSET = 1V + \frac{I_{RIPPLE} \times R_{SENSE} \times ni}{2}$$

$$= 1V + \frac{8A \times 5m\Omega \times 12.5}{2}$$

$$= 1V + 250mV = 1.25V$$

L. gm Amplifier Output Load Network:



$$R_U \| R_B = R_L \qquad R_U = \frac{V_{REF}}{V_{SET}} \times R_L$$

$$R_U = \frac{3V}{1.25V} \times 8.7k = 20.9k$$

$$R_B = \frac{V_{SET}}{V_{REF} - V_{SET}} \times R_U$$

$$R_B = \frac{1.25V}{3V - 1.25V} \times 20.9k = 14.9k$$

M. V_{SET} Computation for No Load Voltage = DAC +15mV:

V_{OUT}, no load voltage to be set 15mV above programed DAC voltage

Added output voltage of the gm amplifier will be:

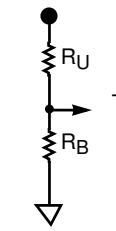
15mV X gm Amplifier gain = 15mv x 19.1 = 287mV

$$V_{SET} = 1V + \frac{I_{RIPPLE} \times R_{SENSE} \times ni}{2} + 287mV$$

$$= 1V + \frac{8A \times 5m\Omega \times 12.5}{2} + 287mV$$

$$= 1V + 250mV + 287mV = 1.536V$$

N. gm Amplifier Output Load Network:



$$R_U \| R_B = R_L \qquad R_U = \frac{V_{REF}}{V_{SET}} \times R_L$$

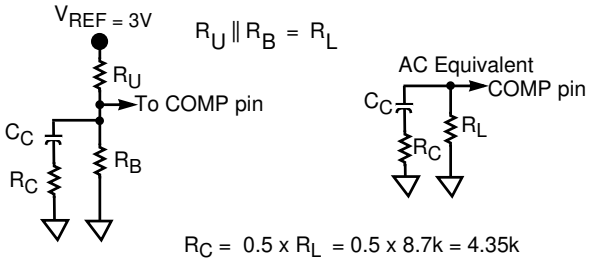
$$R_U = \frac{3V}{1.54V} \times 8.7k = 16.9K$$

$$R_B = \frac{V_{SET}}{V_{REF} - V_{SET}} \times R_U$$

$$R_B = \frac{1.54V}{3V - 1.54V} \times 16.9k = 17.8k$$

O. C_C and R_C Selection:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{R_L} = \frac{1.63m\Omega \times 9mF}{8.7k} = 1.68nF$$



$R_U \| R_B = R_L$

$R_C = 0.5 \times R_L = 0.5 \times 8.7k = 4.35k$