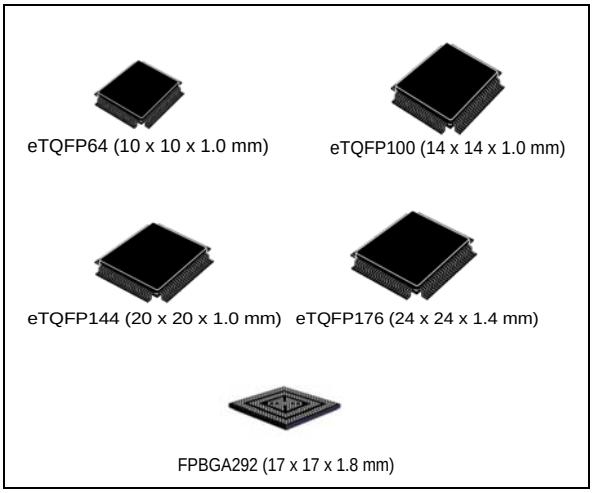
# SPC584Cx, SPC58ECx

## 32-bit Power Architecture® microcontroller for automotive ASIL-B applications

**Data brief**




## Features

- AEC-Q100 qualified
- High performance e200z420n3 dual core:
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 180 MHz
  - Variable Length Encoding (VLE)
- 4224 KB (4096 KB code flash + 128 KB data flash) on-chip flash memory: supports read during program and erases operations, and multiple blocks allowing EEPROM emulation
- 176 KB HSM dedicated flash memory (144 KB code + 32 KB data)
- 384 KB on-chip general-purpose SRAM (in addition to 128 KB core local data RAM: 64 KB included in each CPU)
- Multi-channel direct memory access controller (eDMA) with 64 channels
- 1 interrupt controller (INTC)
- Comprehensive new generation ASIL-B safety concept:
  - ASIL-B of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Body cross triggering unit (BCTU):
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
- Enhanced modular IO subsystem (eMIOS): up to 64 timed I/O channels with 16-bit counter resolution
- Enhanced analog-to-digital converter system with:
  - 3 independent fast 12-bit SAR analog converters
  - 1 supervisor 12-bit SAR analog converter
  - 1 10-bit SAR analog converter with STDBY mode support:
- Communication interfaces:
  - 18 LINFlexD modules
  - 8 deserial serial peripheral interface (DSPI) modules
  - 8 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support
  - Dual channel FlexRay controller
  - 1 Ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008

- Low power capabilities:
  - Versatile low power modes
  - Ultra low power standby with RTC
  - Smart wake-up Unit for contact monitoring
  - Fast wakeup schemes
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART
- Junction temperature range: -40°C to 150°C

**Table 1. Device summary**

| Package | Part number | | | | | |
|---|---|---|---|---|---|---|
| | 2 MB | | 3MB | | 4MB | |
| | Single core | Dual core | Single core | Dual core | Single core | Dual core |
| eTQFP64 | SPC584C70E1 | SPC58EC70E1 | SPC584C74E1 | SPC58EC74E1 | SPC584C80E1 | SPC58EC80E1 |
| eTQFP100 | SPC584C70E3 | SPC58EC70E3 | SPC584C74E3 | SPC58EC74E3 | SPC584C80E3 | SPC58EC80E3 |
| eTQFP144 | SPC584C70E5 | SPC58EC70E5 | SPC584C74E5 | SPC58EC74E5 | SPC584C80E5 | SPC58EC80E5 |
| eLQFP176 | SPC584C70E7 | SPC58EC70E7 | SPC584C74E7 | SPC58EC74E7 | SPC584C80E7 | SPC58EC80E7 |
| FPBGA292 | SPC584C70C3 | SPC58EC70C3 | SPC584C74C3 | SPC58EC74C3 | SPC584C80C3 | SPC58EC80C3 |

# 1 Description

The SPC584Cx and SPC58ECx microcontroller are the first in a new family of devices superseding the SPC564Cx and SPC56ECx family. SPC584Cx and SPC58ECx build on the legacy of the SPC564Cx and SPC56ECx, while introducing new features coupled with higher throughput to provide substantial reduction of cost per feature and significant power and performance improvement (MIPS per mW). On the SPC584Cx and SPC58ECx devices, there are two processor cores e200z420 and one e200z0 core embedded in the Hardware Security Module.

For further info, or full datasheet request, please contact your local ST office.

# 1 Revision history

**Table 1. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 3-sep-2018 | 1 | Initial release. |
| 10-sep-2018 | 2 | Change wrong root part number in *Table 1: Device summary*. |