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DC Brushless Fan Motor Drivers

Multifunction Single-phase Full-wave Fan Motor Driver

BD61245EFV

General Description

BD61245EFV is a 1chip driver that is composed of H-bridge power DMOS FET. Moreover, the circuit configuration is restructured, and convenience has been improved by reducing the external parts and simplifying the setting compared with the conventional driver.

Key Specifications

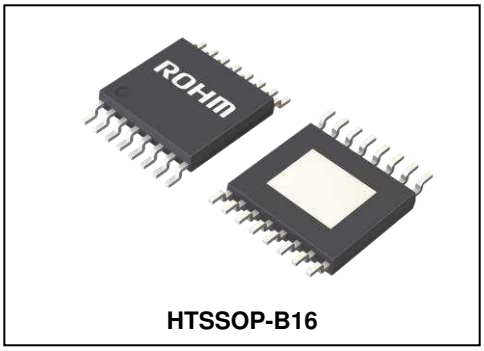
- Operating Voltage Range: 4V to 16V
- Operating Temperature Range: –40°C to +105°C
- Output Voltage(total): 0.2V(Typ) at 0.4A

Features

- High Heat Radiation Package
- Driver Including Power DMOS FET
- Speed Controllable by DC / PWM Input
- I/O Duty Slope Adjust
- PWM Soft Switching
- Current Limit
- Start Duty Assist
- Lock Protection and Automatic Restart
- Quick Start
- Rotation Speed Pulse Signal (FG) Output

Package

W (Typ) x D (Typ) x H (Max)
5.00mm x 6.40mm x 1.00mm



HTSSOP-B16

Applications

- Fan motors for general consumer equipment of desktop PC, Projector, etc.

Typical Application Circuits

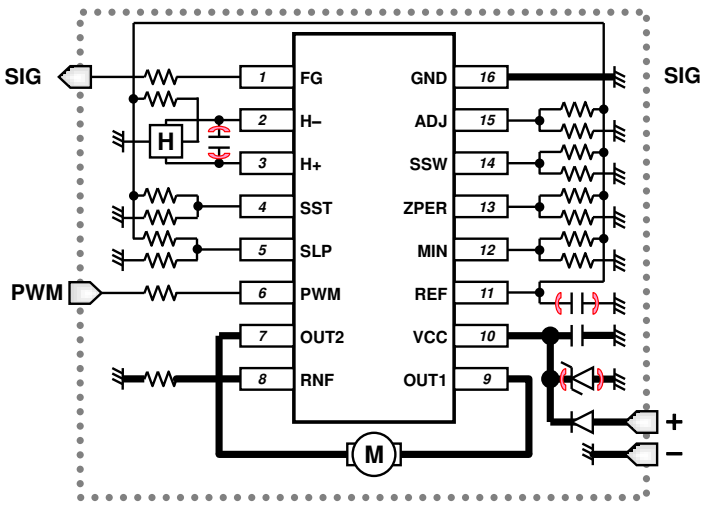


Figure 1. Application of Direct PWM Input

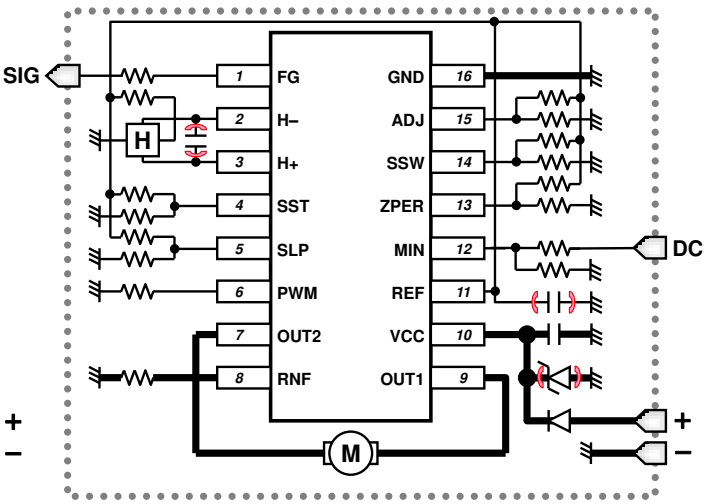
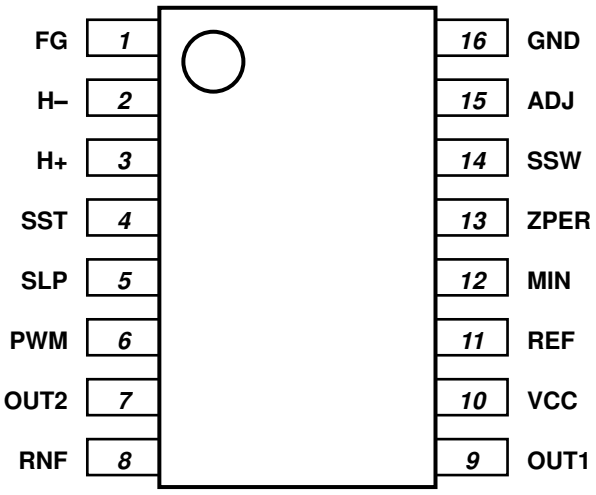


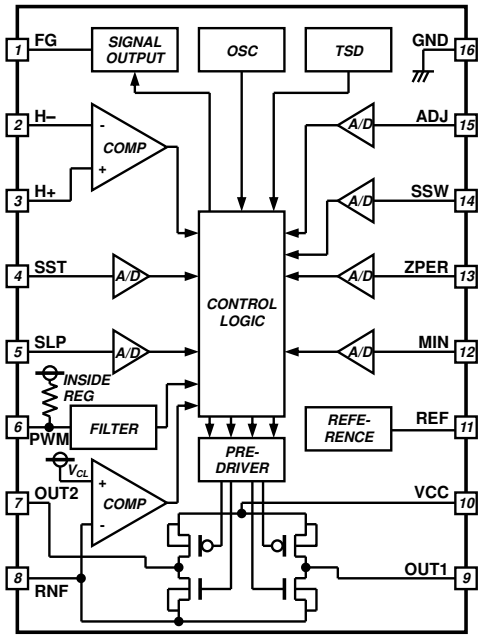
Figure 2. Application of DC Voltage Input

Pin Configuration

(TOP VIEW)



Block Diagram



Pin Description

Pin No.	Pin Name	Function
1	FG	Speed pulse signal output terminal
2	H–	Hall – input terminal
3	H+	Hall + input terminal
4	SST	Soft start setting terminal
5	SLP	I/O duty slope setting terminal
6	PWM	PWM input duty terminal
7	OUT2	Motor output terminal 2
8	RNF	Output current detecting resistor connecting terminal (motor ground)
9	OUT1	Motor output terminal 1
10	VCC	Power supply terminal
11	REF	Reference voltage output terminal
12	MIN	Minimum output duty setting terminal
13	ZPER	Re-circulate period setting terminal
14	SSW	Soft switching setting terminal
15	ADJ	Output duty correction setting terminal
16	GND	Ground terminal (signal ground)

I/O Truth Table

Hall Input		Driver Output		
H+	H–	OUT1	OUT2	FG
H	L	L	H	Hi-Z
L	H	H	L	L

H; High, L; Low, Hi-Z; High impedance
FG output is open-drain type.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	Pd	0.95 *(Note 1)*	W
Operating Temperature Range	Topr	–40 to +105	°C
Storage Temperature Range	Tstg	–55 to +150	°C
Output Voltage	V_{OMAX}	18	V
Output Current	I_{OMAX}	1.8 *(Note 2)*	A
Rotation Speed Pulse Signal (FG) Output Voltage	V_{FG}	18	V
Rotation Speed Pulse Signal (FG) Output Current	I_{FG}	10	mA
Reference Voltage (REF) Output Current	I_{REF}	10	mA
Input Voltage1 (H+,H–,MIN,SSW,SST,ZPER,SLP,ADJ)	V_{IN1}	2.6	V
Input Voltage2 (PWM)	V_{IN2}	6.5	V
Junction Temperature	Tj	150	°C

(Note 1) Derate by 7.6mW/°C when operating over Ta=25°C.
(Note 2) Do not exceed Pd and Tj=150°C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
HTSSOP-B16				
Junction to Ambient	θ_{JA}	131.5	30.8	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	9	3	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers..

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}	4	12	16	V
Hall Input Voltage	V_H	0	-	2	V
PWM Input Frequency	f_{PWM}	15	-	50	kHz

Electrical Characteristics (Unless otherwise specified Ta=25°C, V_{CC}=12V)

Parameter	Symbol	Limit			Unit	Conditions	Characteristic Data
		Min	Typ	Max			
Circuit Current	I_{CC}	1.8	3.3	4.8	mA		Figure 3
Output Voltage	V_O	-	0.2	0.44	V	I_O=±400mA, High and low side total	Figure 4 to Figure 7
Lock Detection ON Time	t_{ON}	0.3	0.5	0.7	s		Figure 8
Lock Detection OFF Time	t_{OFF}	3.0	5.0	7.0	s		Figure 9
Lock Detection OFF/ON Ratio	r_{LCK}	8	10	12	-	$r_{LCK}=t_{OFF}/t_{ON}$	Figure 10
Hall Input Hysteresis Voltage	V_{HYS+}	±7	±12	±17	mV		Figure 11
FG Output Low Voltage	V_{FGL}	-	-	0.3	V	I_{FG}=5mA	Figure 12 to Figure 13
FG Output Leak Current	I_{FGL}	-	-	10	μA	V_{FG}=16V	Figure 14
PWM Input High Level Voltage	V_{PWMH}	2.5	-	5.0	V		-
PWM Input Low Level Voltage	V_{PWML}	-0.3	-	1.0	V		-
PWM Input Current	I_{PWMH}	-10	0	10	μA	V_{PWM}=5V	Figure 15 to Figure 16
	I_{PWML}	-50	-25	-12	μA	V_{PWM}=0V	
Reference Voltage	V_{REF}	2.2	2.4	2.6	V	I_{REF}=-1mA	Figure 17 to Figure 18
Current Limit Setting Voltage	V_{CL}	120	150	180	mV		Figure 19

For parameters involving current, positive notation means inflow of current to IC while negative notation means outflow of current from IC.

Typical Performance Curves (Reference Data)

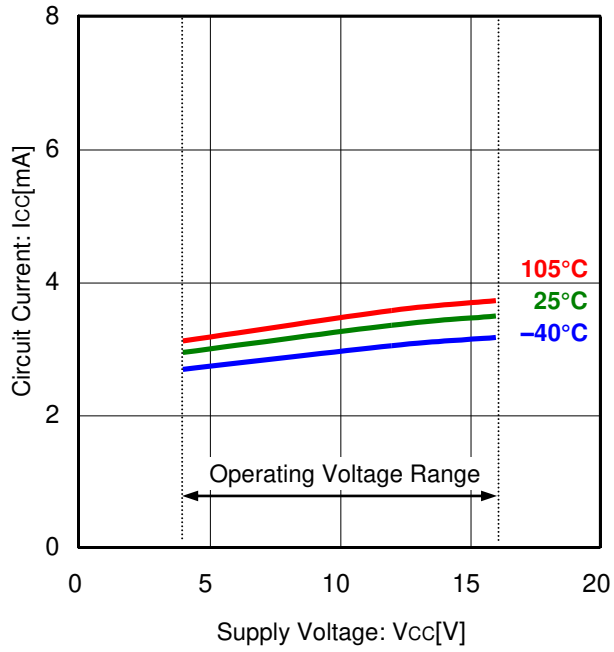


Figure 3. Circuit Current vs Supply Voltage

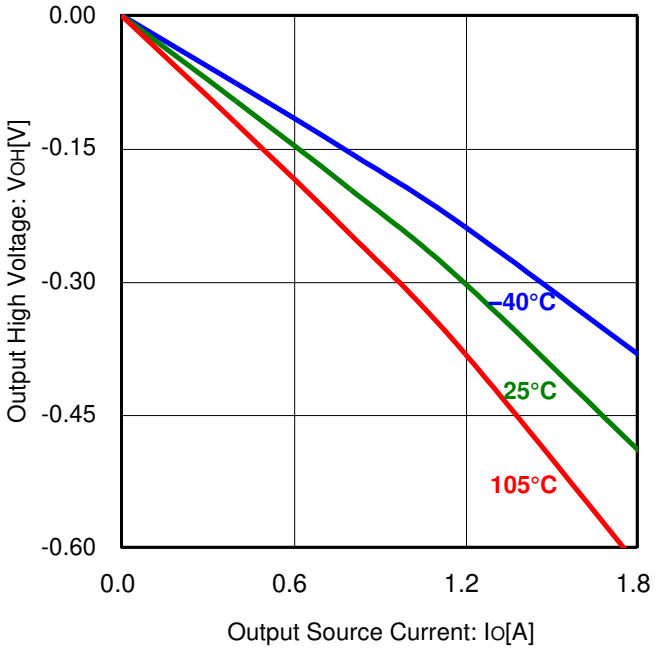


Figure 4. Output High Voltage vs Output Source Current (V_{CC}=12V)

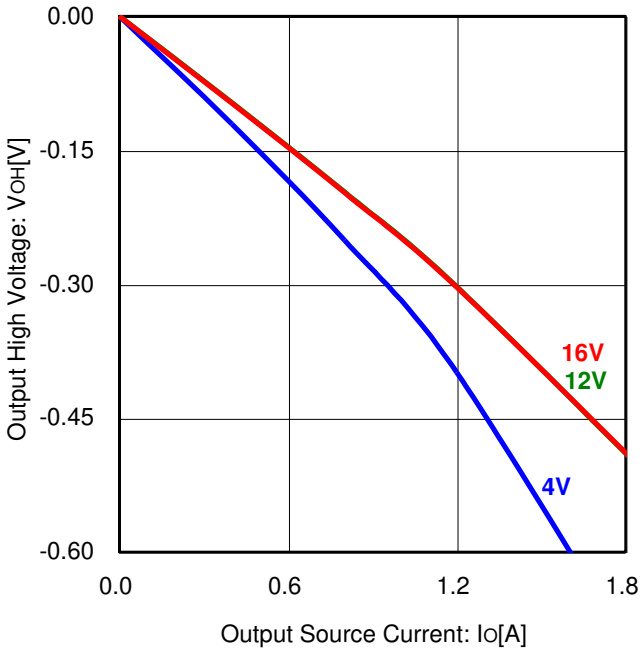


Figure 5. Output High Voltage vs Output Source Current (Ta=25°C)

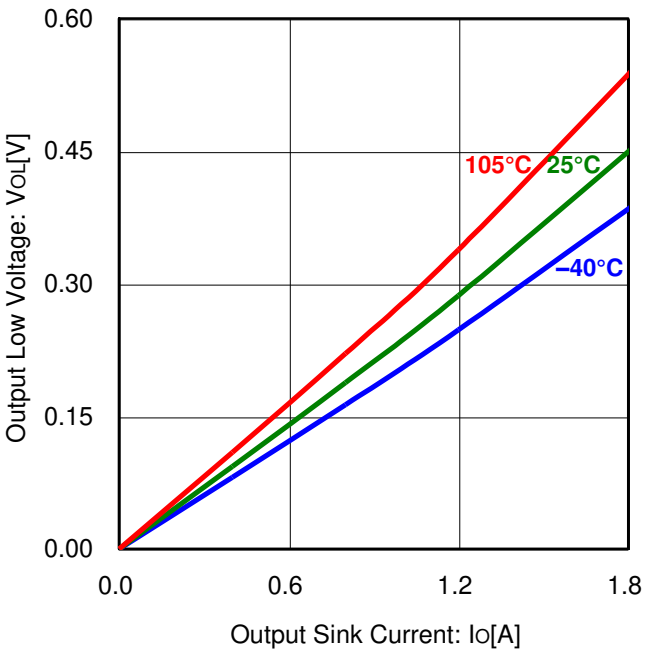


Figure 6. Output Low Voltage vs Output Sink Current (V_{CC}=12V)

Typical Performance Curves (Reference Data) – continued

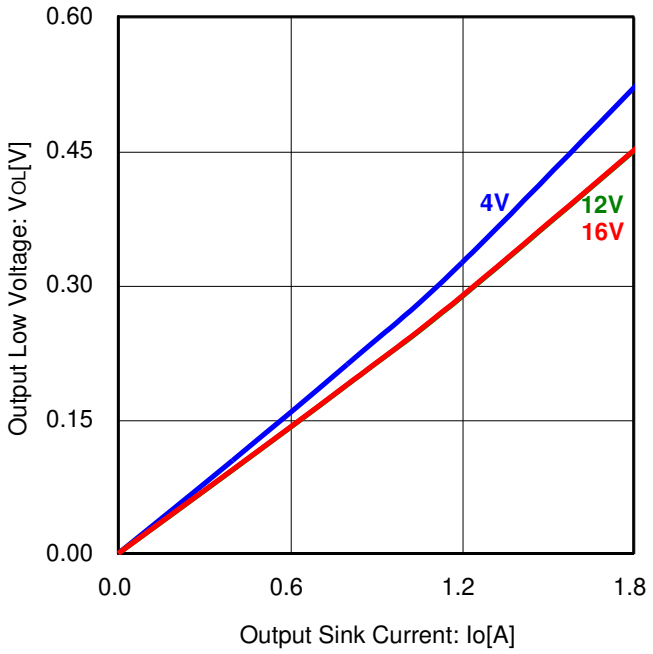


Figure 7. Output Low Voltage vs Output Sink Current (Ta=25°C)

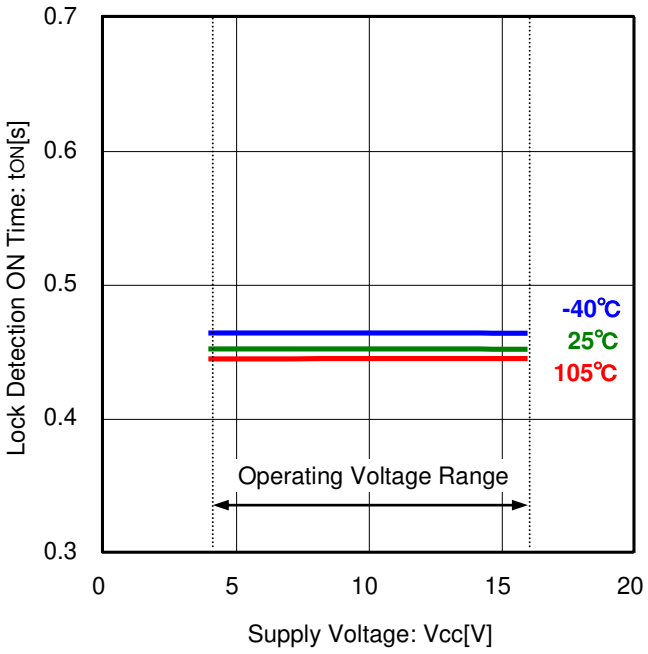


Figure 8. Lock Detection ON Time vs Supply Voltage

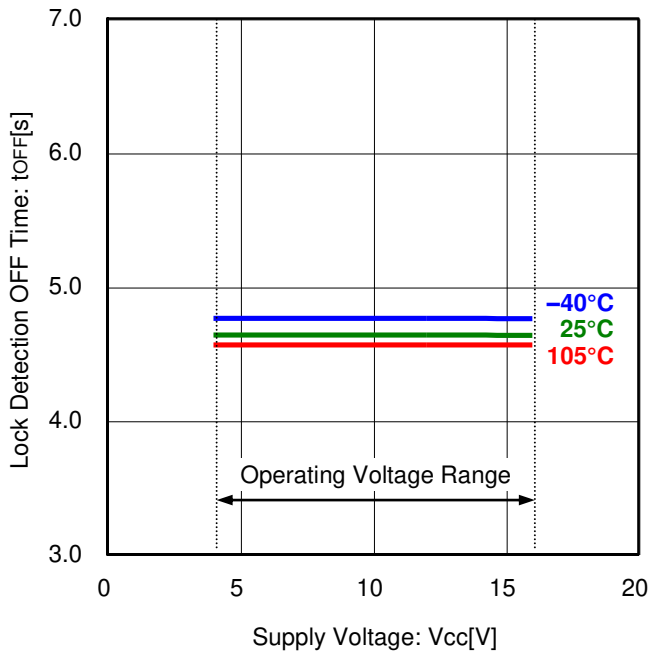


Figure 9. Lock Detection OFF Time vs Supply Voltage

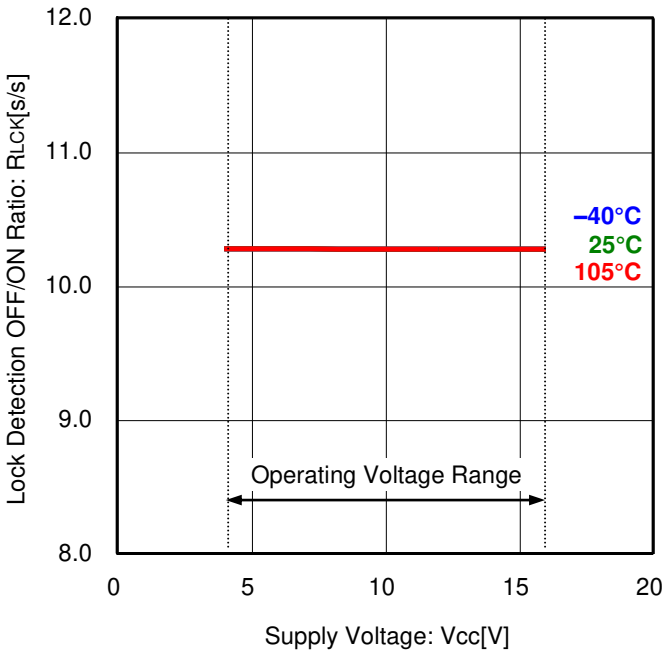


Figure 10. Lock Detection OFF/ON Ratio vs Supply Voltage

Typical Performance Curves (Reference Data) – continued

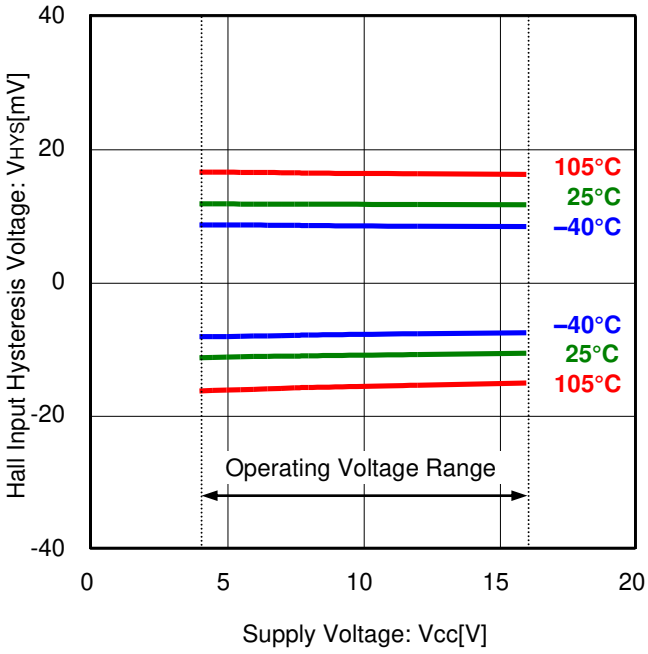


Figure 11. Hall Input Hysteresis Voltage vs Supply Voltage

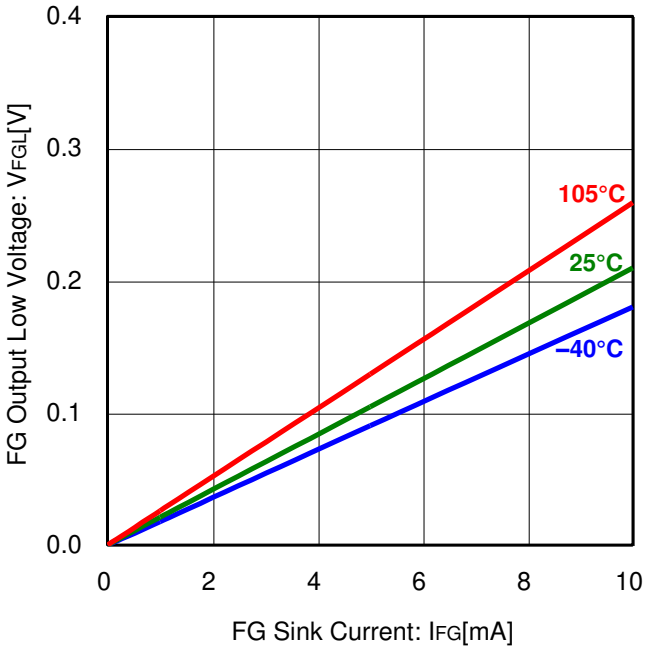


Figure 12. FG Output Low Voltage vs FG Sink Current (VCC=12V)

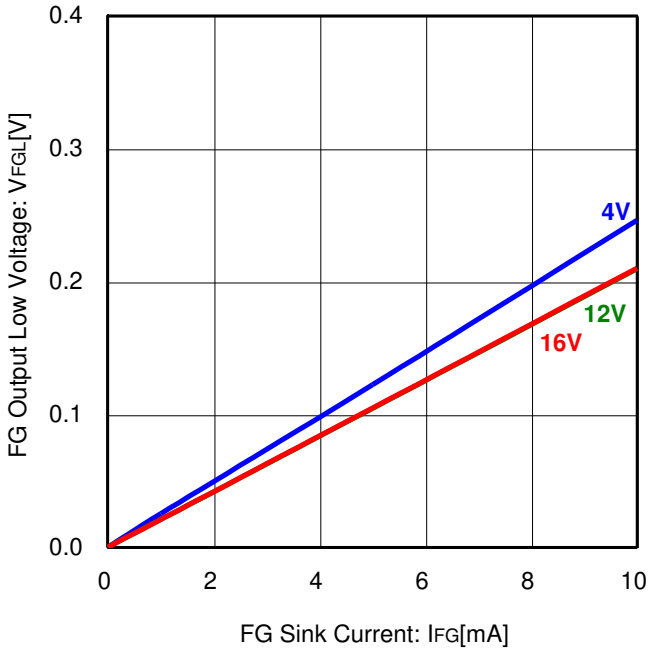


Figure 13. FG Output Voltage vs FG Sink Current (Ta=25°C)

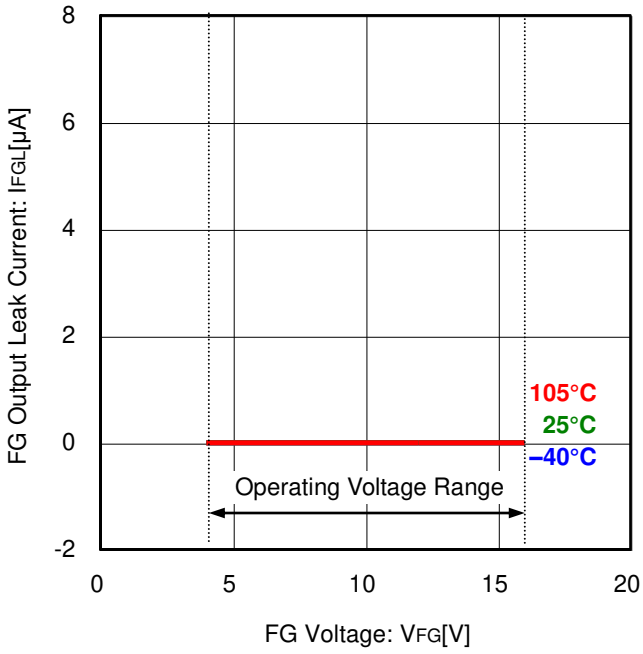


Figure 14. FG Output Leak Current vs FG Voltage

Typical Performance Curves (Reference Data) – continued

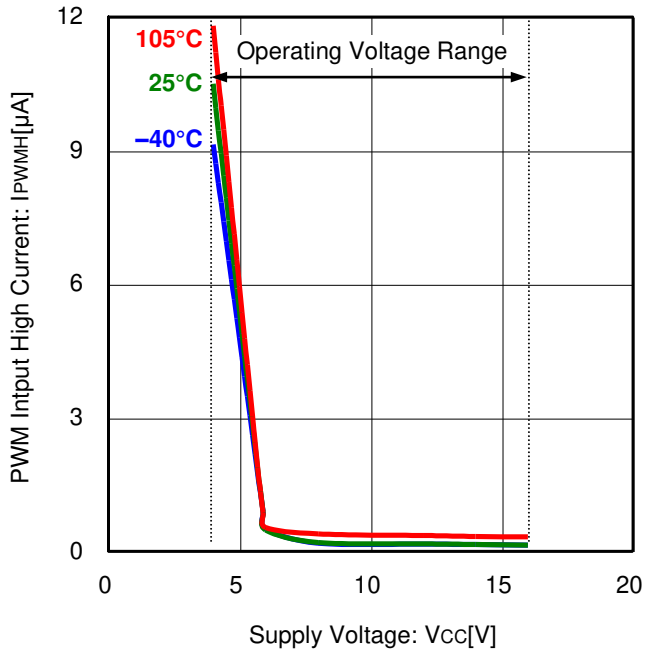


Figure 15. PWM Input High Current vs Supply Voltage
(V_{PWM}=5V)

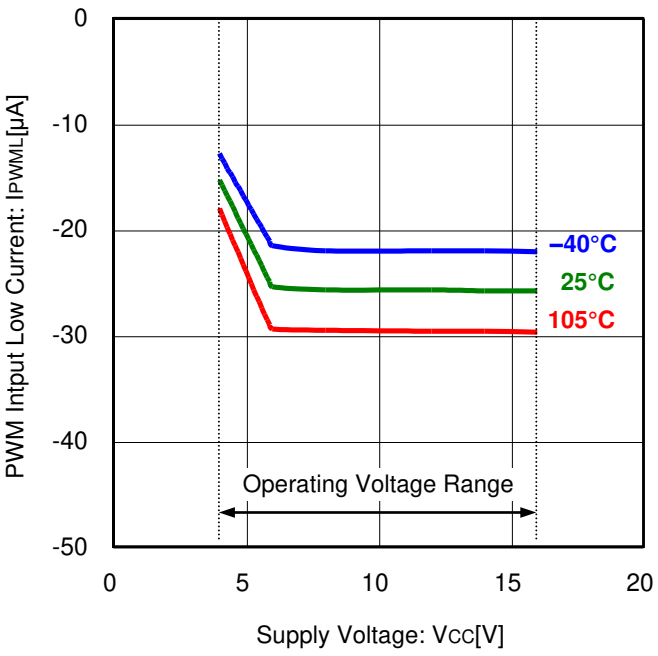


Figure 16. PWM Input Low Current vs Supply Voltage
(V_{PWM}=0V)

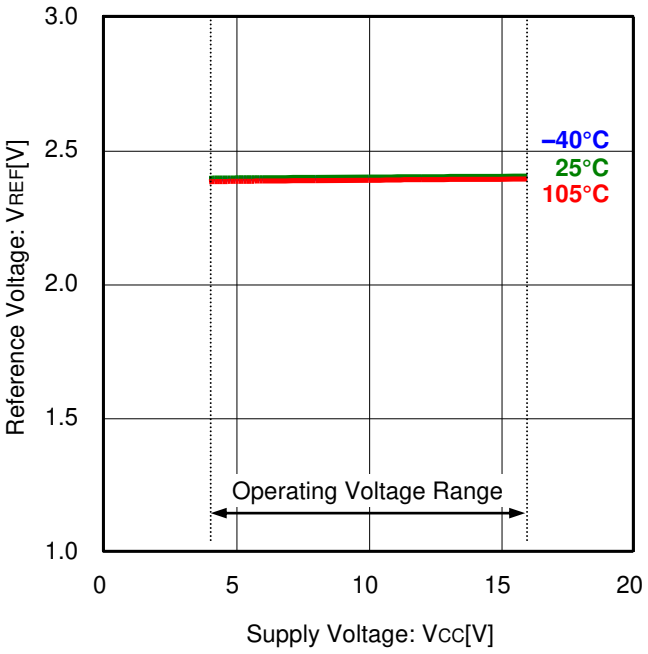


Figure 17. Reference Voltage vs Supply Voltage
(V_{CC}=12V)

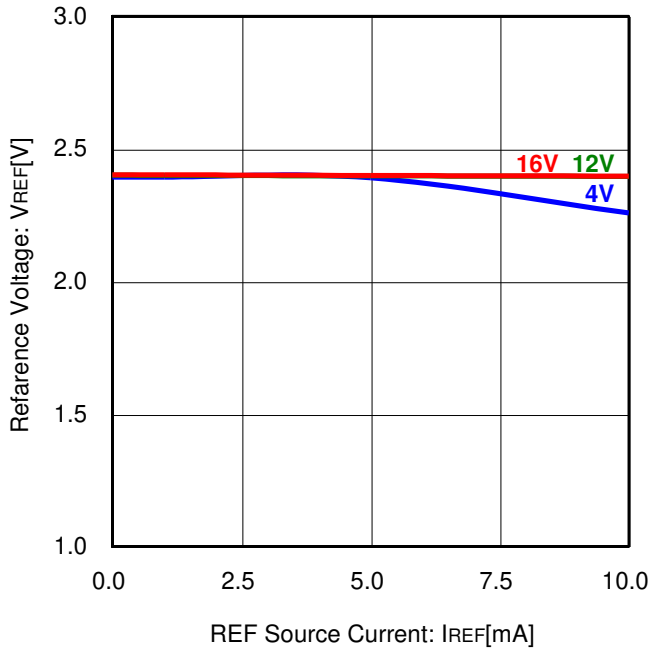


Figure 18. Reference Voltage vs REF Source Current
(Ta=25°C)

Typical Performance Curves (Reference Data) – continued

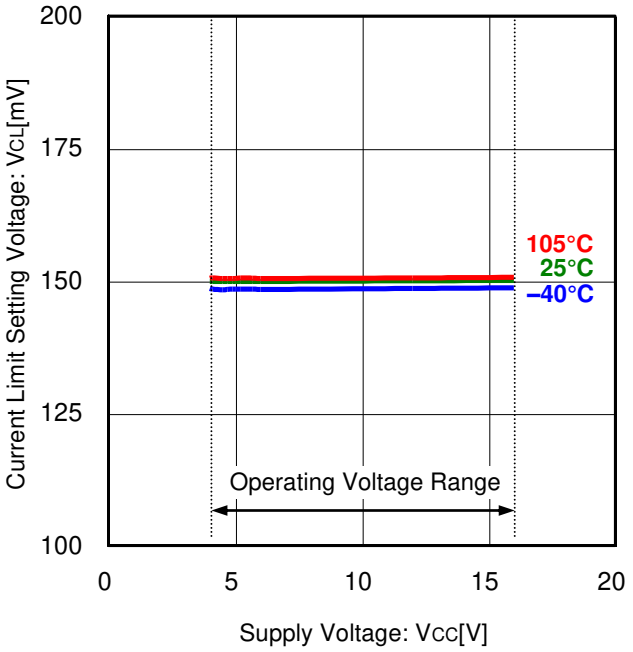


Figure 19. Current Limit Setting Voltage vs Supply Voltage

Application Circuit Examples (Constant Values are for Reference)

1. PWM Input Application

This is the application example of direct PWM input into PWM terminal. Minimum rotational speed is set in MIN terminal voltage.

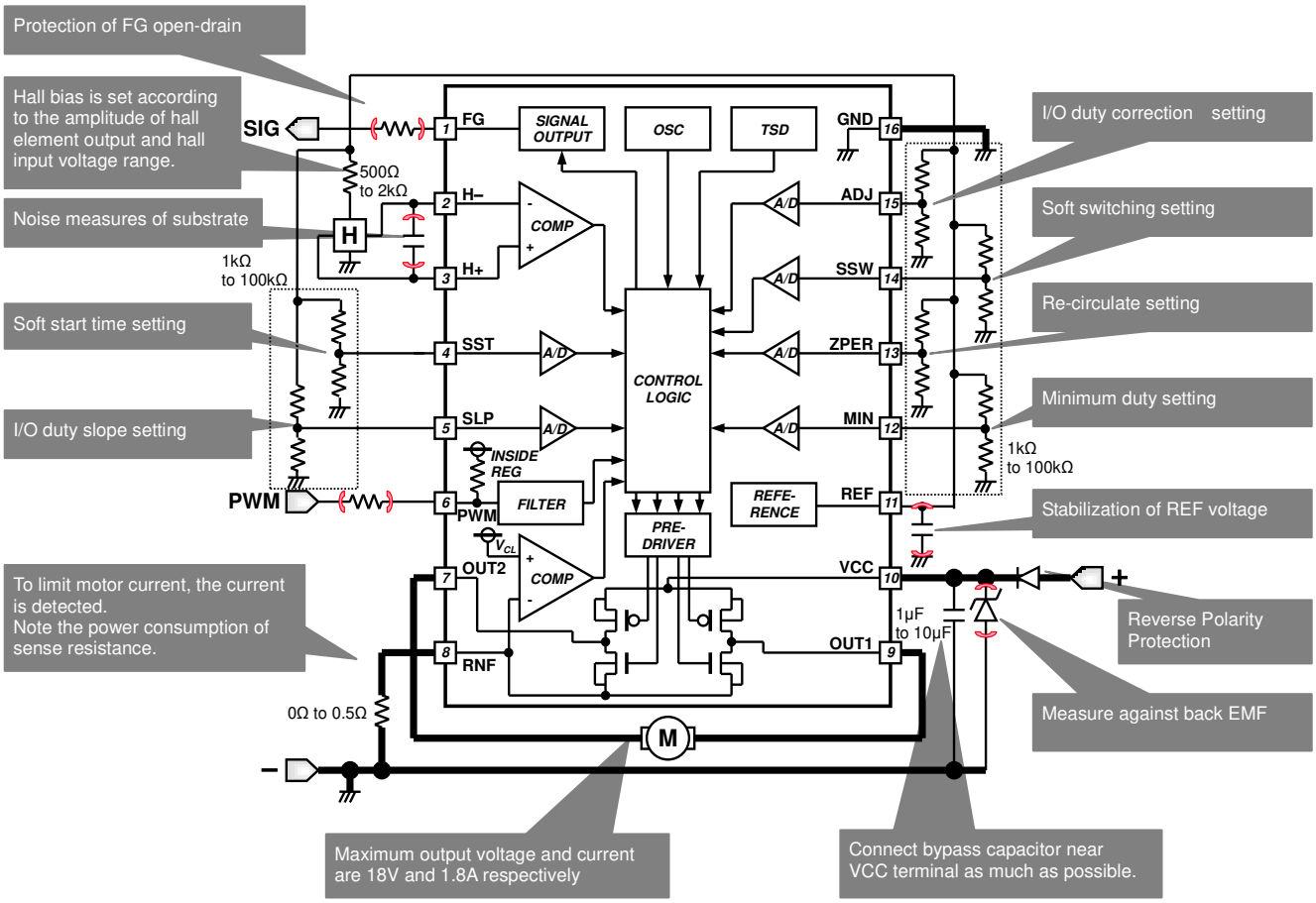
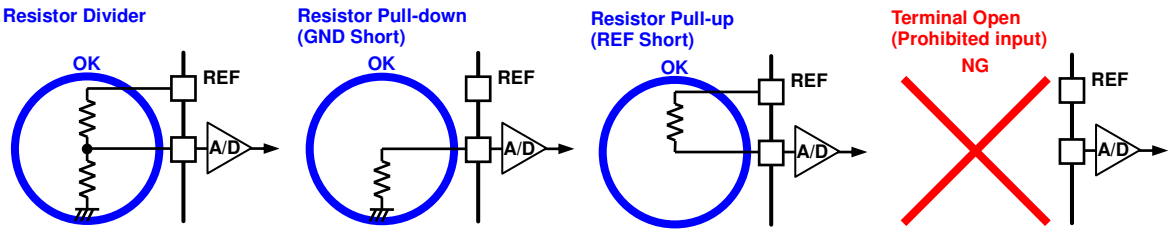


Figure 20. PWM Input Application

When a function is not used, do not let the A/D converter input terminal open.



Application Design Note

(1) Please connect the bypass capacitor with reference to the value mentioned above. Because there is a possibility of the motor start-up failure etc. due to IC malfunction.

Substrate Design Note

(1) IC power(Vcc), and motor outputs(OUT1, 2) lines are made as wide as possible.
(2) IC ground (GND) line is common with the application ground except motor ground (i.e. hall ground etc.), and arranged near to (–) land.
(3) The bypass capacitor and/or Zener diode are placed near to VCC pin.
(4) H+ and H– lines are arranged side by side and made from the hall element to IC as short as possible, because it is easy for the noise to influence the hall lines.

Application Circuit Examples (Constant Values are for Reference) – continued

2. DC Voltage Input Application

This is the application example of DC voltage into MIN terminal. Minimum rotational speed setting is disable.

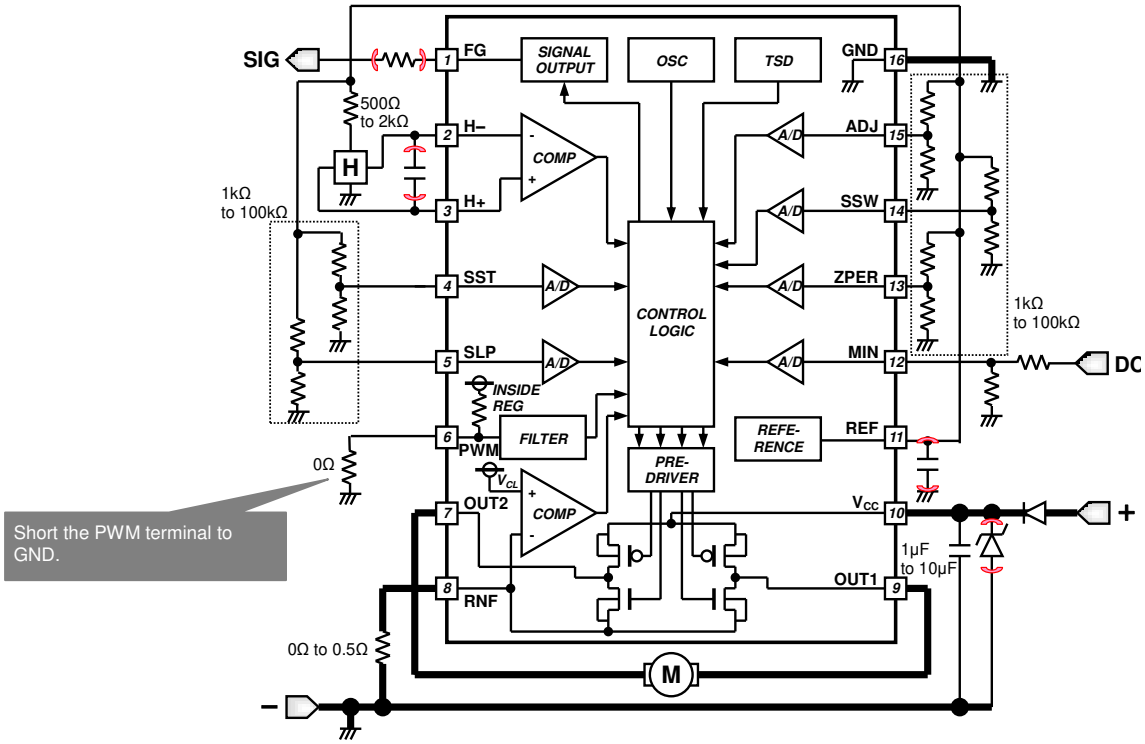
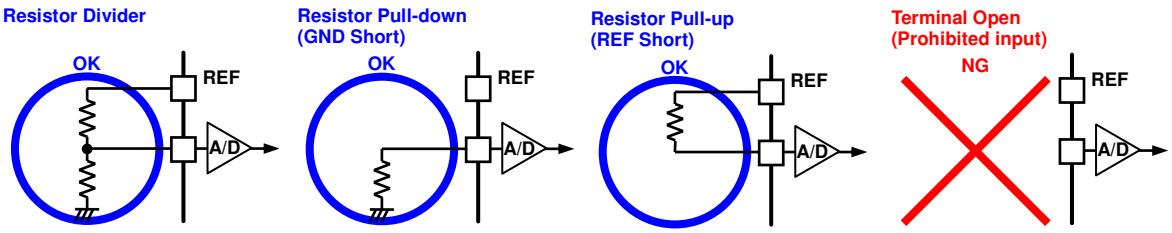


Figure 21. DC Voltage Input Application

When a function is not used, do not let the A/D converter input terminal open.



Functional Descriptions

1. Variable Speed Operation

There are 2 ways to control the speed of motor.
(1) PWM Control (Input PWM pulse into PWM terminal)
(2) Voltage Control (Input DC voltage into MIN terminal)

Both (1) and (2), output PWM frequency is 50kHz. When computed duty is less than 5%, a driving signal is not output.

(1) PWM Operation by Pulse Input in PWM Terminal

The PWM signal from the controller can be input directly to IC in Figure 22. The output duty is controlled by the input PWM duty (Figure 23). Refer to recommended operating conditions and electrical characteristics (P.4) for the input condition.

Internal power-supply voltage (INTERNAL REG; typ 5.0V) is impressed when the PWM terminal is open, it becomes 100% input of the duty and equivalent, and a full torque is driven. There must be a pull- down resistance outside of IC to make it to torque 0 when the PWM terminal opens (However, only at the controller of the complimentary output type.). Insert the protective resistance if necessary.

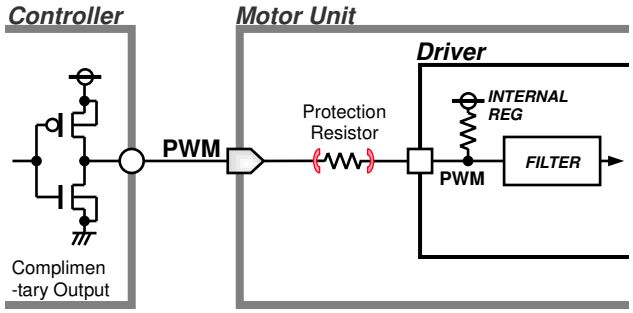


Figure 22. PWM Input Application

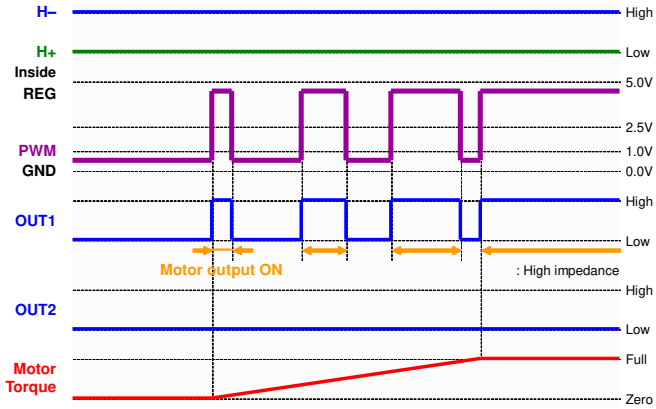


Figure 23. PWM Input Operation Timing Chart

○Setting of Minimum Output Duty (MIN)

The voltage which divided REF terminal voltage by resistance is input into MIN terminal, and minimum output duty is set like Figure 24. When input duty from a PWM terminal is lower than minimum output duty which is set by MIN terminal, the output duty does not fall to lower than minimum output duty.

The MIN terminal is the input terminal of the analog-digital converter to have an input voltage range of the REF voltage, and the resolution is 128 steps (0.78% per step). When minimum output duty is not set, please perform resistance pull-down of MIN terminal.

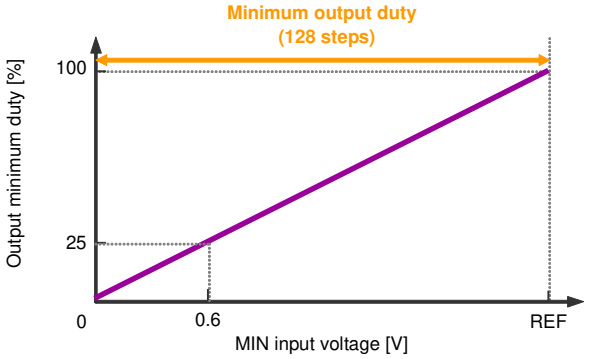


Figure 24. Relation of MIN terminal Voltage and Output

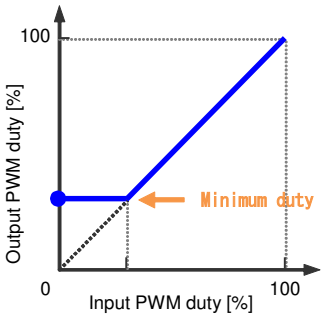


Figure 25. Setting of Minimum Output Duty

Functional Descriptions – continued

(2) PWM Operation by DC Input in MIN Terminal

Output duty is controlled by input voltage from MIN terminal. Output duty is 100% when MIN terminal voltage is 2.4V (Typ), output duty is 0% when MIN terminal voltage is 0V. (If using SLP function, it is not like this.)

In voltage control mode, short the PWM terminal to GND.

Please refer to input voltage 1(P.3) for the input condition of the MIN terminal. Because terminal voltage becomes unsettled when MIN terminal is in an open state, like application of Figure 26, please be applied some voltage to MIN terminal.

Minimum output duty cannot be set in voltage control.

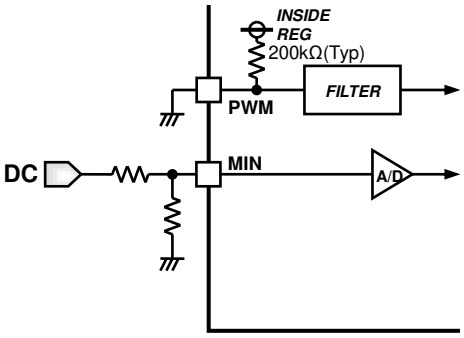


Figure 26. DC Input Application

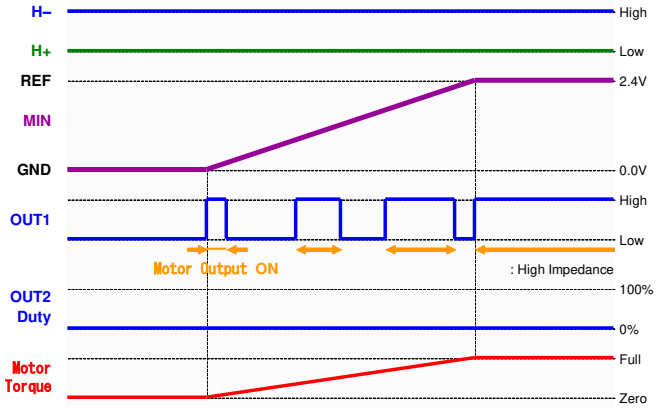


Figure 27. DC Input Operation Timing Chart

2. Input-output Duty Slope Setting (SLP)

Slope properties of input duty and output duty can be set with SLP terminal like Figure 28. SLP setting work in both mode, PWM control and voltage control. The resolution is 7bit (128 steps).

The voltage of SLP terminal is less than 0.3V (Typ), slope of input-output duty characteristic is fixed to 1. And fixed to 0.5 in 0.3V to 0.6V (Typ) (refer to Figure 29). When slope setting is not set, pull-down SLP terminal.

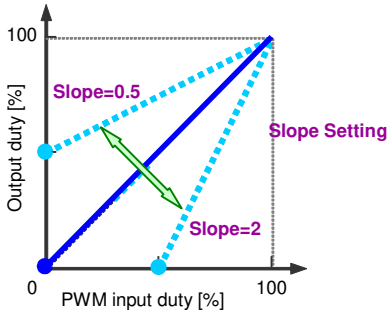


Figure 28. Adjust of Slope of I/O Duty

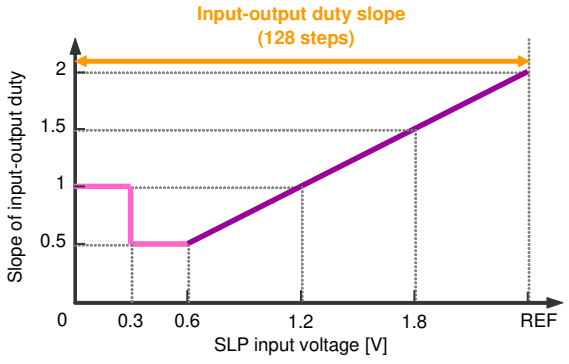


Figure 29. Relations of SLP terminal voltage and the input-output duty slope characteristics

Functional Descriptions – continued

3. Input and Output Duty Properties Adjustment Function (ADJ)

When input duty vs output duty shows the characteristic of the straight line, rotational speed may become the characteristics that middle duty area swells by the characteristic of fan motor. (Figure 30)

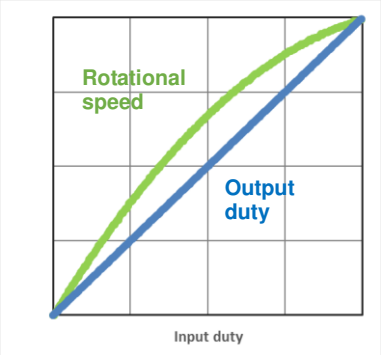


Figure 30. Properties curve of input PWM duty vs rotational speed

This IC reduces duty in the middle duty area and can adjust rotational speed characteristics of the motor with a straight line.

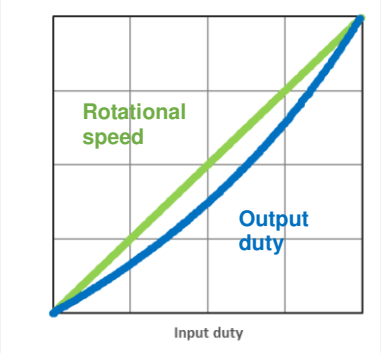


Figure 31. Properties curve of input PWM duty vs rotational speed after adjusting

The adjustment to reduce duty is performed by ADJ terminal input voltage. The ADJ terminal is input terminal of A/D converter and the resolution is 7bit. By input 0 (ADJ=GND) of the ADJ terminal, the characteristic of input duty vs. output duty becomes straight line (no adjustment). The adjustment become maximum by input 127(ADJ=REF), and output duty in input duty 50% decreases to about 25%.

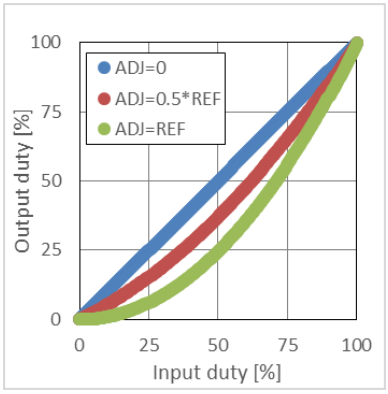


Figure 32. Input duty vs output duty characteristics

Please set the voltage of ADJ terminal so that motor rotation speed in input duty 50% is on the diagonal which links the rotation speed of 0% to 100%. IC corrects output duty so that overall rotation speed properties match a straight line.

When it is used together with SLP function, at first ADJ adjustment is performed in slope=1, and please adjust SLP after adjusting input duty vs. rotation speed property.

Functional Descriptions – continued

4. About Setting of Phase Switching of Output

The period of Soft switching and re-circulate can be adjusted by SSW and ZPER setting.

(1) Soft Switching Period Setting (SSW)

Angle of the soft switching can be set by the input voltage of SSW terminal. When one period of the hall signal is assumed 360°, the angle of the soft switching can be set from 22.5° to 90° by the input voltage of SSW terminal (refer to Figure 33). Resolution of SSW terminal is 128 steps. Operational image is shown in Figure 34.

*Soft switching angle means the section where output duty changes between 0% and setting duty at the timing of output phase change. To smooth off the current waveform, the coefficient table that duty gradually changes is set inside IC, and the step is 16.

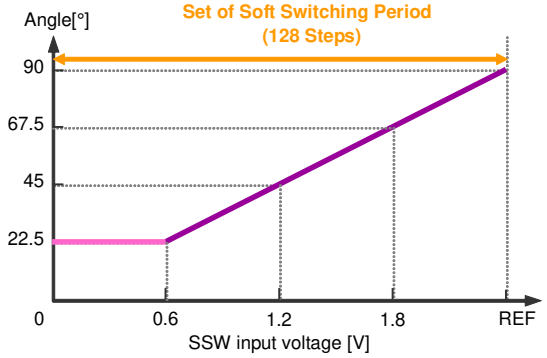


Figure 33. Relation of SSW terminal Voltage and Soft Switching Period

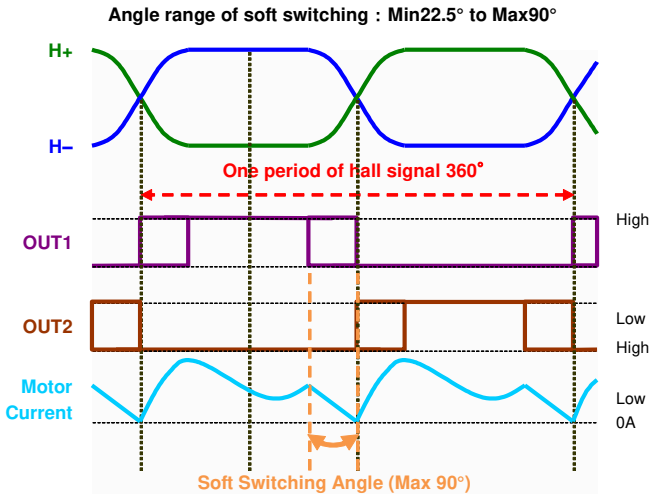


Figure 34. Soft switching angle

(2) Re-circulate Period Setting (ZPER)

Re-circulate angle at the timing of output phase changes can be set by the input voltage of ZPER terminal. When one period of the hall signal is assumed 360°, the angle of the re-circulate can be set from 0° to 90° by the input voltage of ZPER terminal (refer to Figure 35). Resolution of ZPER terminal is 128steps. Operational image is shown in Figure 36.

When angular degree to regenerate is bigger than soft switching angular degree, a soft switching section for 5.6 degrees enters.

*Re-circulate angle means the section where the coil current re-circulate before the timing of output phase change. If it is set appropriately, it is effective to suppress leaping up of voltage by BEMF, and reduce invalid electricity consumption. The logic of the output transistor in the section is decided depending on the hall input logic. As for the output of the H logic, the logic of the motor output in high impedance (Hi-Z). The output of the L logic remains L.

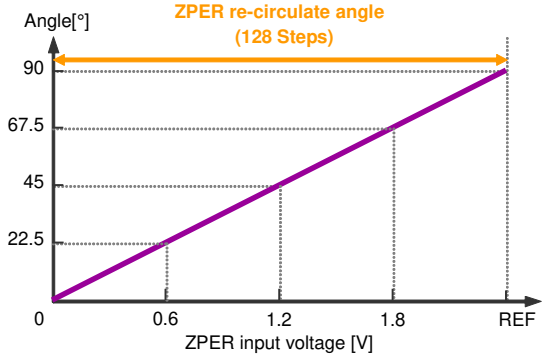


Figure 35. Relation of ZPER terminal Voltage and Re-circulate Period

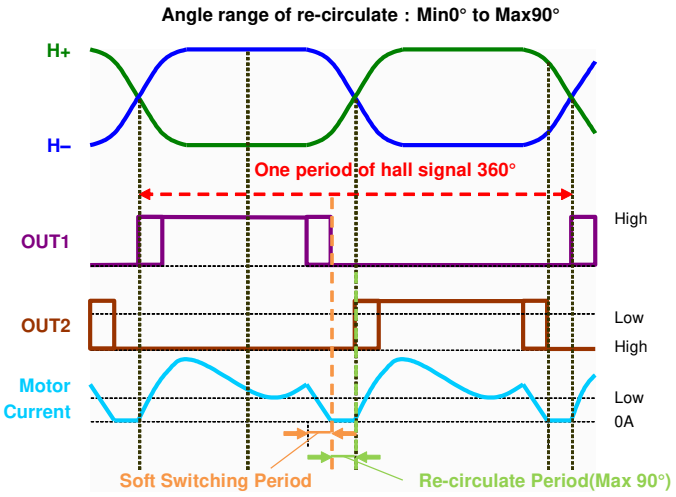


Figure 36. Re-circulate angle

Functional Descriptions – continued

(3) Kickback Restraint Function

When there is induced current to the motor coil , regenerative current flows to the power supply.
However, when reverse connection protection diode is connected, V_{CC} voltage rises because the diode prevents current flow to power supply. (Figure 37)

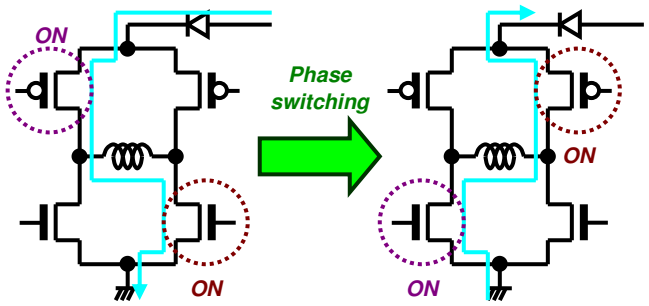


Figure 37. V_{CC} Voltage Rise by Back Electromotive Force

The kickback restraint function is a supporting function to reduce induced current in a motor coil.

To the specifications of the motor, please adjust soft switching period (SSW) and re-circulate period (ZPER) to reduce leaping up of the output voltage.

By specifications and how to use motor, it may not reduce this induced current.
For example, it becomes the severe condition in the motor startup.
In this case leaping up of the voltage decreases when it sets soft start time for a long time.

Functional Descriptions – continued

5. Soft Start

Soft start function gradually change drive duty to suppress sound noise and peak current when the motor start up etc. PWM duty resolution is 7bit (128steps, 0.78% per step). SST terminal sets the step up time of duty increment.

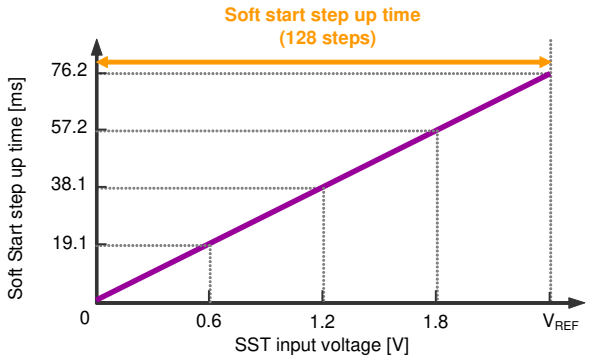
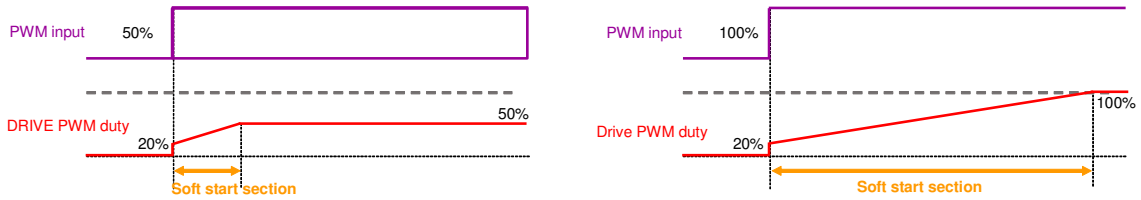


Figure 38. Relations of SST terminal voltage and soft start step up time

Duty transition time is
(Difference of current duty and Target duty (output duty after SLP/ADJ calculation)) x (step time)

When soft start time is set for a long time, lock protection may be detected without enough motor torque when motor start up from 0% duty. Therefore start up duty is set to approximately 20% (25/128).



Start with input duty 50% Start with input duty 100%

Figure 39. Soft start operation image from motor stop condition

When SST terminal voltage = REF terminal voltage, and 100% duty is input on motor stop condition, output duty arrives at 100% after progress the time of 76.2ms x (128-25step) = 7.84 seconds

Soft start functions always work when the change of input duty as well as motor start up. In addition, it works when duty goes down from high duty. Duty step down time is the half of duty step up time.

6. Start duty assist

It is the function that enable the motor to start even if drive duty output is low, when the soft start function is not used. When input duty is within 50% at motor stop condition, 50% duty is output till three times of hall signal change are detected. Operational image is shown in Figure 40.

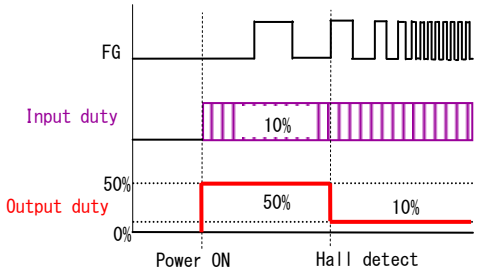


Figure 40. Start duty assist operation at input duty 10%

Functional Descriptions – continued

7. Current Limit

Current limit function turns off the output when the current flow through the motor coil is detected exceeding a set value. The working current value of the limit is determined by current limit voltage V_{CL} and RNF terminal voltage.
The value of the current sense resistor is included in not only the R_{NF} resistor but also wire resistance in the IC (Rwire=Approximately 10mΩ) or the resistance of the substrate pattern line (Rline).
In Figure 41, current flow in motor coil is Io, resistor to detect Io is R_{NF}=50mΩ (@1/2W), wire resistance in the IC is Rwire=10mΩ, the resistance of the substrate pattern line is Rline=40mΩ, power consumption of RNF is P_R, current limit voltage V_{CL}=150mV (Typ), current limit value and power consumption of RNF can be calculated below expression.

About current limit value, when motor current is big, it is affected by Rwire and Rline.
Please decide the RNF resistor value in considering a real substrate.
When current limit function is not used, please short RNF terminal to GND.

$$I_O[A] = V_{CL}[V] / (Rwire + Rline + R_{NF}) [\Omega]$$
$$= 150[mV] / (10 + 40 + 50)[m\Omega]$$
$$= 150[mV] / 100[m\Omega]$$
$$= 1.5[A]$$

$$P_{RMAX}[W] = V_{CL}[V] \times I_O[A]$$
$$= 150[mV] \times 1.5[A]$$
$$= 0.225[W] *$$

*This calculation ignores Rwire and Rline.

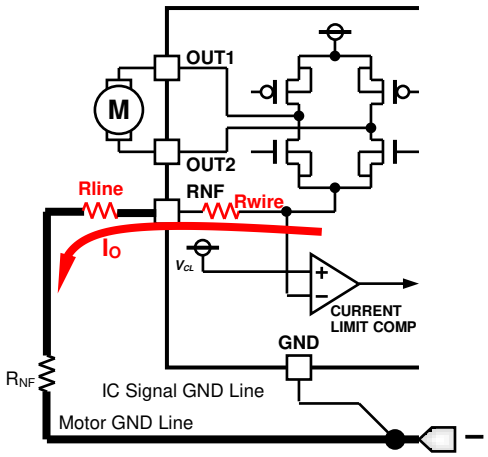


Figure 41. Current limit setting and GND line

8. Lock Protection and Automatic Restart

Motor rotation is detected by hall signal period. IC detects motor rotation is stop when the period becomes longer than the time set up at the internal counter, and IC turns off the output. Lock detection ON time (t_{ON}) and lock detection OFF time (t_{OFF}) are set by the digital counter based on internal oscillator. Therefore the ratio of ON/OFF time is always constant. Timing chart is shown in Figure 42.

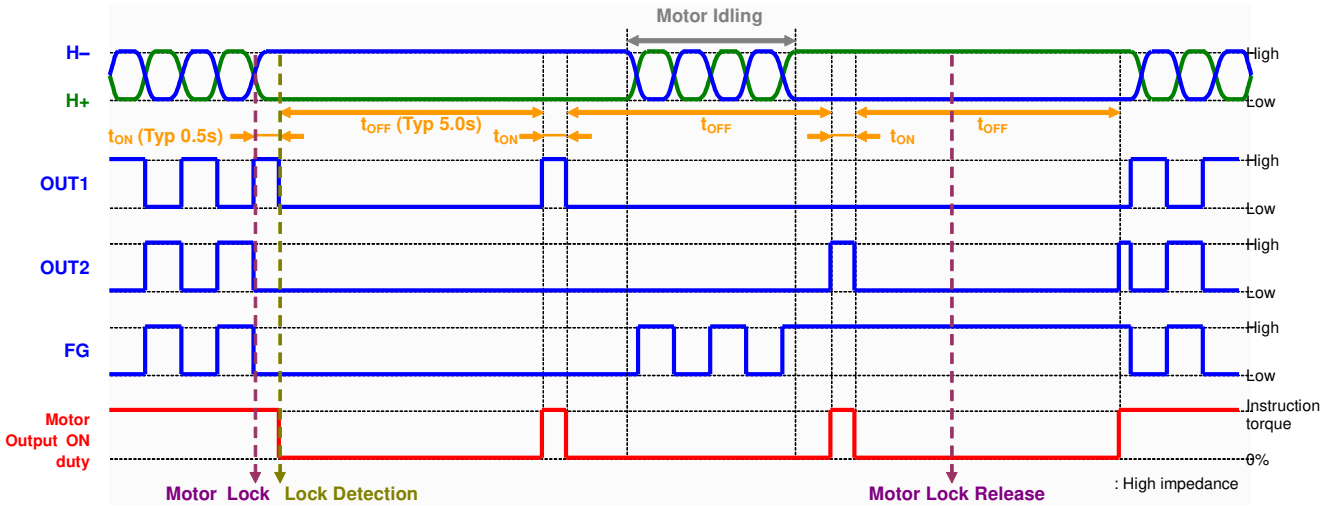


Figure 42. Lock Protection Timing Chart

Functional Descriptions – continued

9. Quick Start

When torque off logic is input by the control signal over a fixed time, the lock protection function is disabled. The motor can restart quickly once the control signal is applied.

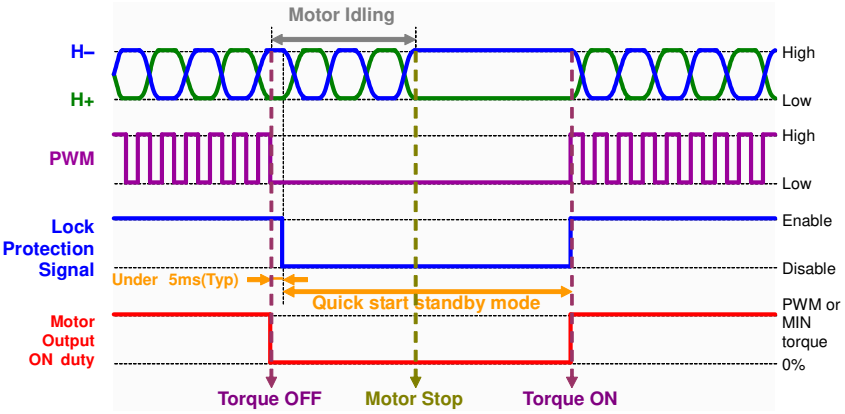


Figure 43. Quick Start Timing Chart (PWM Input Application)

10. Hall Input Setting

The input voltage of a hall signal is input in "Hall Input Voltage" in P.4 including signal amplitude. In order to detect rotation of a motor, the amplitude of hall signal more than "Hall Input Hysteresis Voltage" is required. Input the hall signal more than 34mVpp at least.

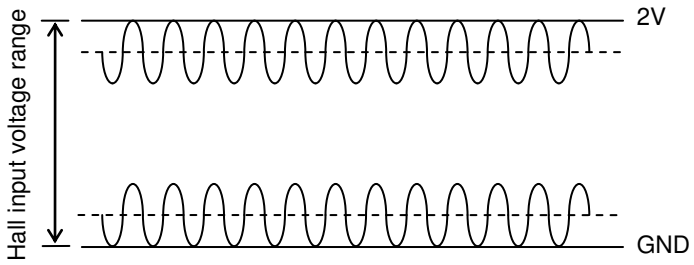


Figure 44. Hall Input Voltage Range

○Reducing the Noise of Hall Signal

Hall element may be affected by V_{CC} noise or the like depending on the wiring pattern of board. In this case, place a capacitor like C1 in Figure 45. In addition, when wiring from the hall element output to IC hall input is long, noise may be loaded on wiring. In this case, place a capacitor like C2 in Figure 45.

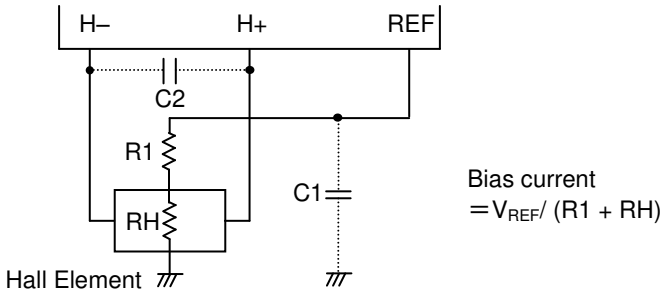


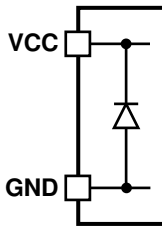
Figure 45. Application near of Hall Signal

11. High-speed detection protection

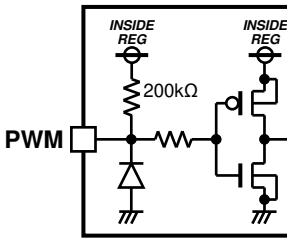
High-speed detection protection begin lock protection action when it detects that the hall input signal is in an abnormal state (more than Typ 2.5kHz). Noise may be induced on wiring. In this case, place a capacitor like C2 in Figure 45.

I/O Equivalence Circuit (Resistance Values are Typical)

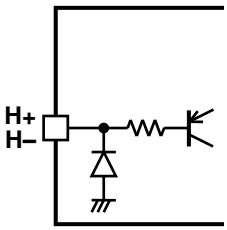
1. Power supply terminal



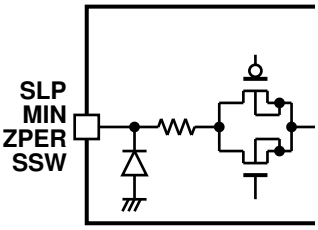
2. PWM input duty terminal



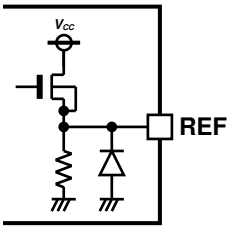
3. Hall input terminal



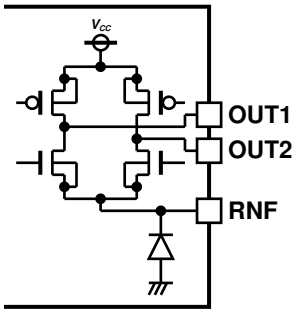
4. A/D converter input terminal



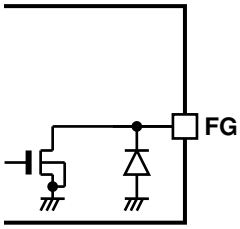
5. Reference voltage output terminal



6. Motor output terminal
Output current detecting resistor connecting terminal



7. Rotation speed pulse signal output terminal



Safety Measure

1. Reverse Connection Protection Diode

Reverse connection of power results in IC destruction as shown in Figure 46. When reverse connection is possible, reverse connection protection diode must be added between power supply and V_{CC}.

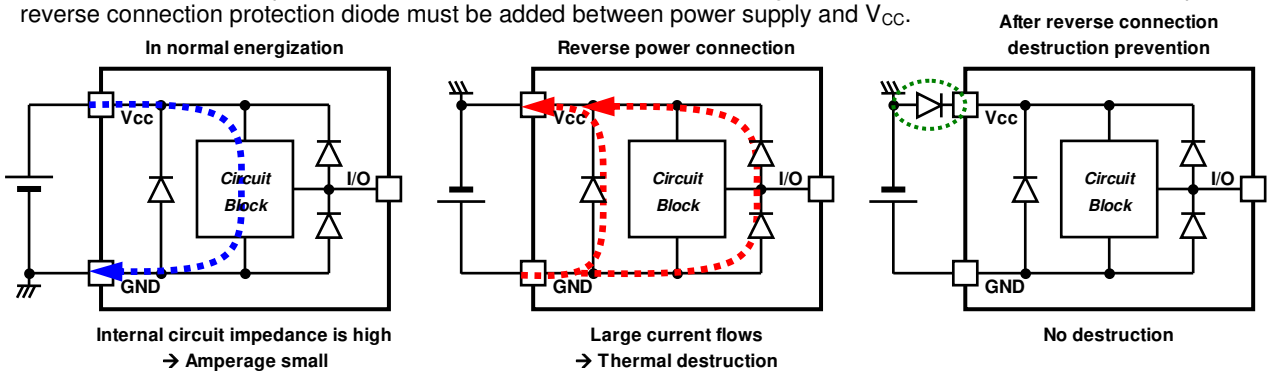


Figure 46. Flow of Current When Power is Connected Reversely

2. Protection against V_{CC} Voltage Rise by Back Electromotive Force

Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected, V_{CC} voltage rises because the diode prevents current flow to power supply.

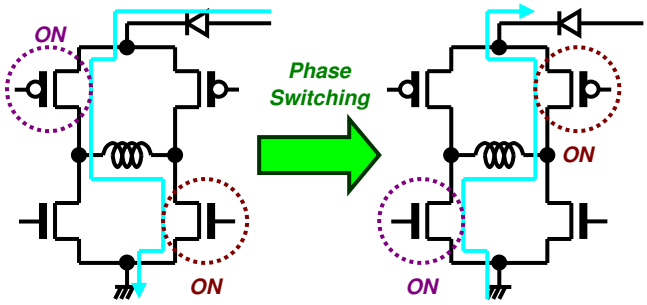


Figure 47. V_{CC} Voltage Rise by Back Electromotive Force

When the absolute maximum rated voltage may be exceeded due to voltage rise by back electromotive force, place (A) Capacitor or (B) Zener diode between V_{CC} and GND. If necessary, add both (C).

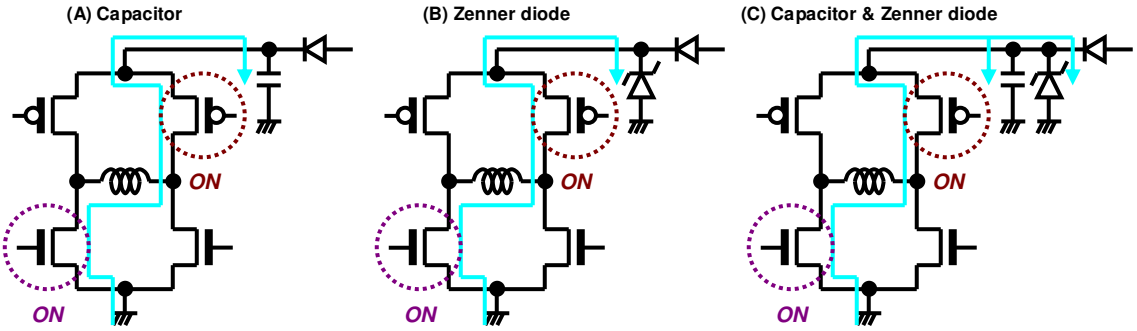


Figure 48. Measure against V_{CC} and Motor Driving Outputs Voltage

3. Problem of GND line PWM Switching

Do not perform PWM switching of GND line because GND terminal potential cannot be kept to a minimum.

4. Protection of Rotation Speed Pulse (FG) Open-Drain Output

FG output is an open drain and requires pull-up resistor. Adding resistor can protect the IC. Exceeding the absolute maximum rating, when FG terminal is directly connected to power supply, could damage the IC.

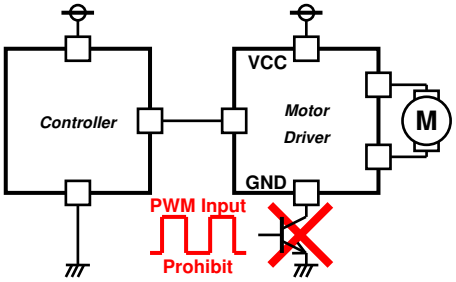


Figure 49. GND Line PWM Switching Prohibited

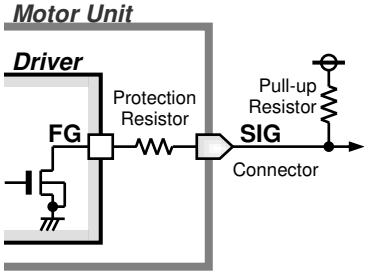


Figure 50. Protection of FG Terminal

Power Dissipation

1. Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C (normal temperature). IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip into the package, that is junction temperature of the absolute maximum rating, depends on circuit configuration, manufacturing process, etc. Power dissipation is determined by this maximum joint temperature, the thermal resistance in the state of the substrate mounting, and the ambient temperature. Therefore, when the power dissipation exceeds the absolute maximum rating, the operating temperature range is not a guarantee. The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

2. Thermal Resistance

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance. In the state of the substrate mounting, thermal resistance from the chip junction to the ambience is shown in θ_{JA} [°C/W], and thermal characterization parameter from junction to the top center of the outside surface of the component package is shown in Ψ_{JT} [°C/W]. Thermal resistance is classified into the package part and the substrate part, and thermal resistance in the package part depends on the composition materials such as the mold resins and the lead frames. On the other hand, thermal resistance in the substrate part depends on the substrate heat dissipation capability of the material, the size, and the copper foil area etc. Therefore, thermal resistance can be decreased by the heat radiation measures like installing a heat sink etc. in the mounting substrate.
The thermal resistance model is shown in Figure 51, and Equation is shown below.

$\theta_{JA} = (Tj - Ta) / P$ [ºC/W]
$\Psi_{JT} = (Tj - Tt) / P$ [ºC/W]

where:
θ_{JA} is the thermal resistance from junction to ambient [ºC/W]
Ψ_{JT} is the thermal characterization parameter from junction to the top center of the outside surface of the component package [ºC/W]
Tj is the junction temperature [ºC]
Ta is the ambient temperature [ºC]
Tt is the package outside surface (top center) temperature [ºC]
P is the power consumption [W]

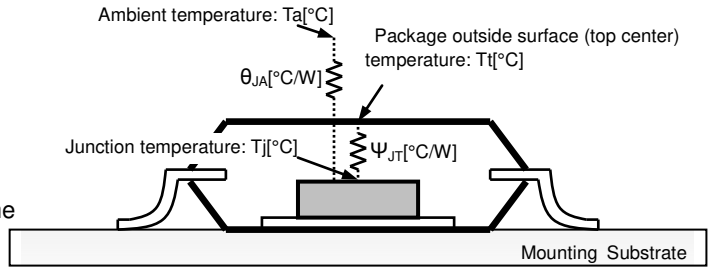


Figure 51. Thermal Resistance Model of Surface Mount

Even if it uses the same package, θ_{JA} and Ψ_{JT} are changed depending on the chip size, power consumption, and the measurement environments of the ambient temperature, the mounting condition, and the wind velocity, etc.

3. Thermal De-rating Curve

Thermal de-rating curve indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature (25°C), and becomes 0W at the maximum joint temperature (150°C). The inclination is reduced by the reciprocal of thermal resistance θja. The thermal de-rating curve under a condition of thermal resistance (P.3) is shown in Figure 52.

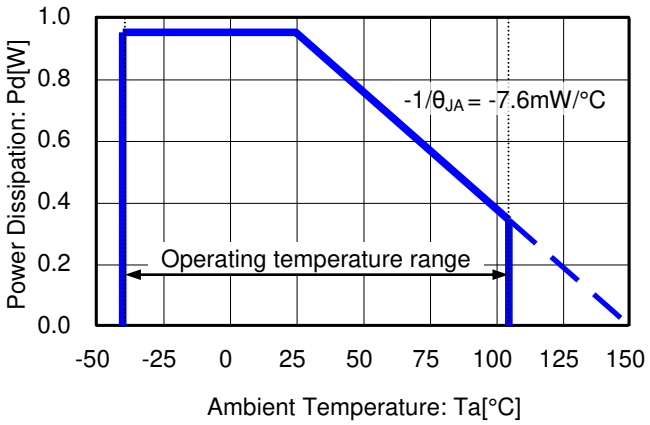


Figure 52. Power Dissipation vs Ambient Temperature

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

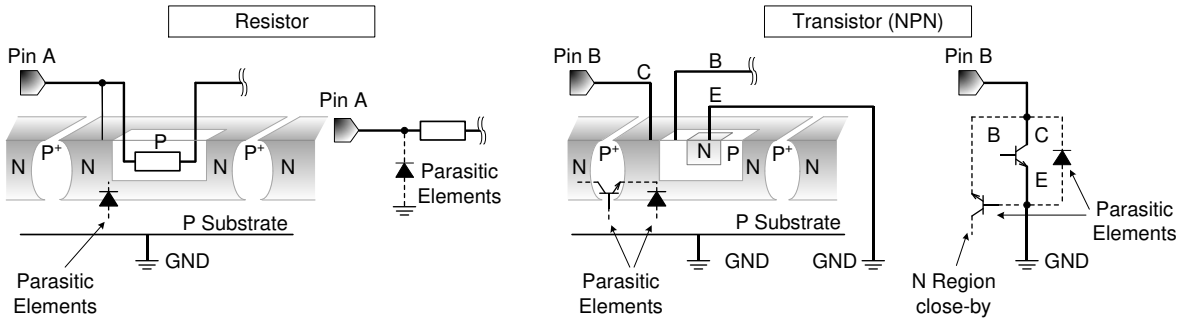


Figure 53. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

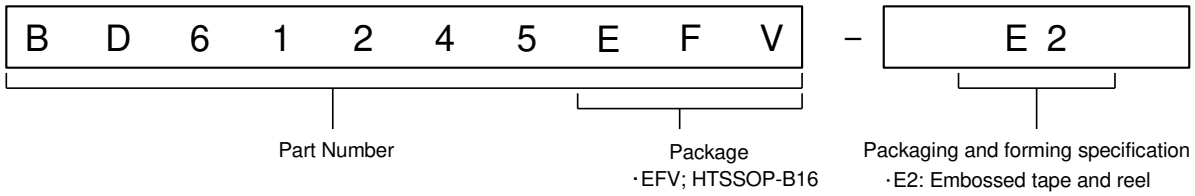
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown (TSD) Circuit

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature will rise which will activate the TSD circuit that will turn OFF all output pins. When the junction temperature falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information



Marking Diagram