5A, 18V, 700kHz ACOT™ Synchronous Step-Down Converter with VID Control

General Description

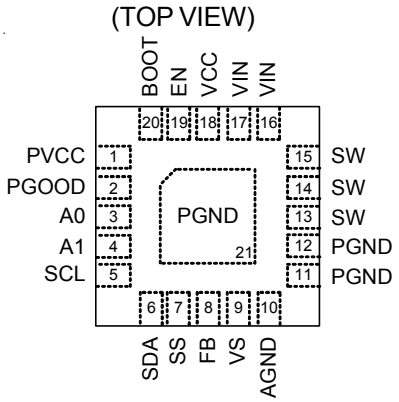
The RT6203B is an adaptive on-time mode synchronous Buck converter. The main control loop of the RT6203B uses an adaptive on-time mode control which provides a very fast transient response with no external components. The RT6203B operates from 4.5V to 18V VIN input. After the initial power-up, the output voltage can be changed by codes sent into the IC via an I²C compatible VID control bus. There are special codes which can be used to program current limit level and thermal shutdown level. Shutdown and startup can be also programmed by special codes. The device also features an adjustable soft-start time. Output voltage is adjustable by resistor divider through the FB pin between 0.8V to 8V.

Features

- **VID Control Range Via I²C Compatitable Interface : 0.72V to 1.48V in 10mV Steps**
- **Adjustable Current Limit**
- **Adjustable Thermal Shutdown**
- **Fast Transient Response**
- **Adjustable Output Voltage from 0.8V to 8V**
- **Steady 700kHz Switching Frequency**
- **Optimized for All Ceramic Capacitors**
- **Externally-Adjustable, Pre-Biased Compatible Soft-Start**
- **Input Under-Voltage Lockout**
- **Output Over- and Under-Voltage Protection**
- **Power Good Output**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Pin Configuration

(TOP VIEW)

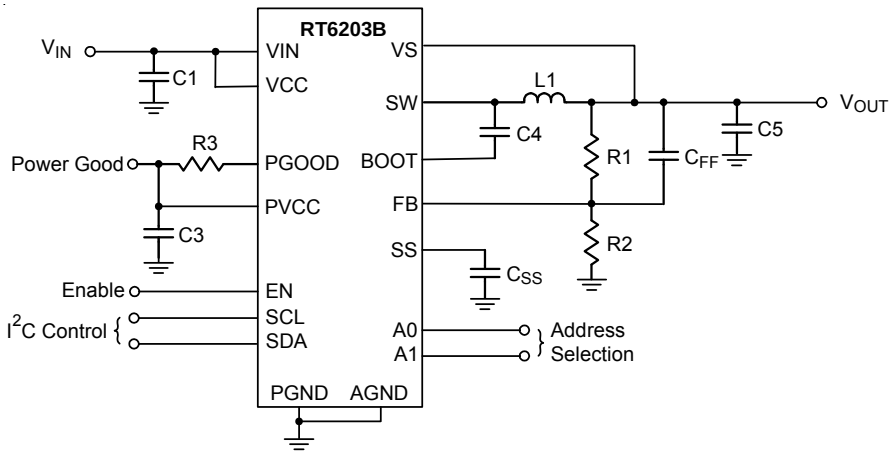


WQFN-20L 4x4

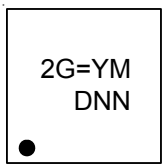
Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

Simplified Application Circuit



Marking Information



2G= : Product Code

YMDNN : Date Code

Ordering Information

RT6203B□□□

- Package Type
  QW : WQFN-20L 4x4 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Trim Operation
  L : Latch-off
- PWM/PSM Mode
  B : PWM Mode

Note :

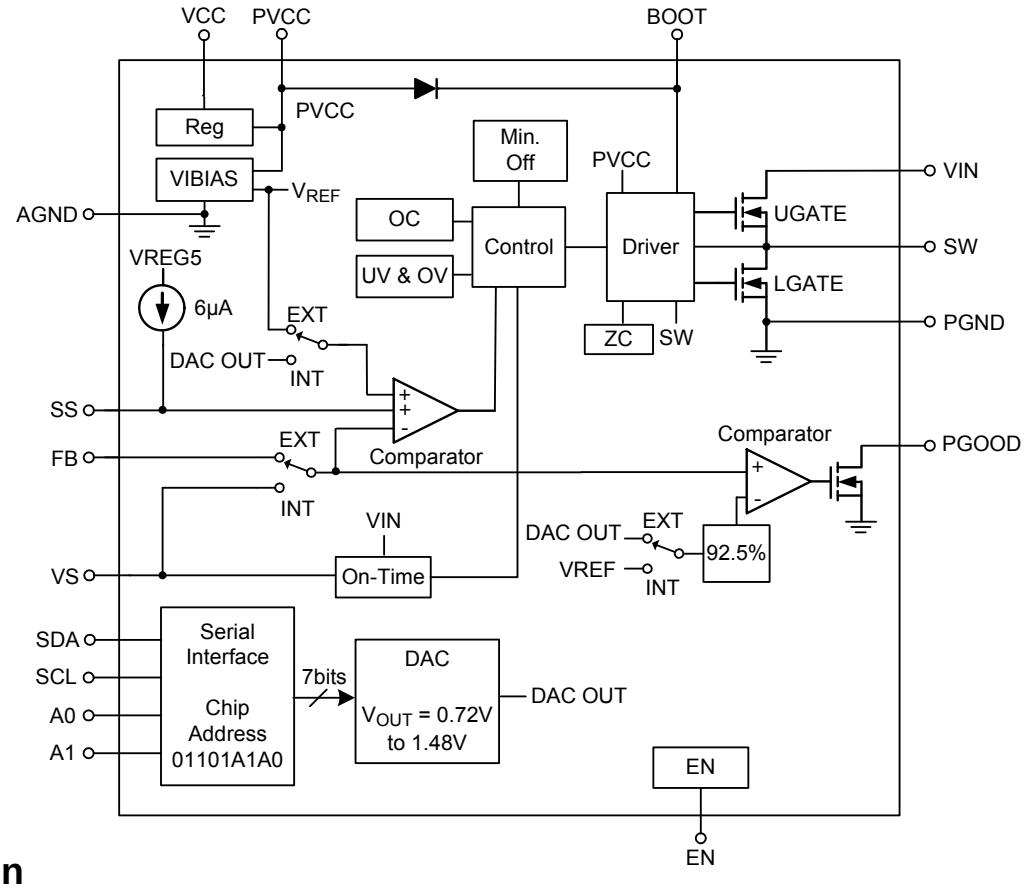
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PVCC	5V power supply output. Connect a capacitor (typical 1μF) to AGND.
2	PGOOD	Open-drain power good indicator output.
3	A0	LSB of chip address. Tie to GND for 0, pull high for 1.
4	A1	LSB+1 of chip address. Tie to GND for 0, pull high for 1.
5	SCL	I^2C clock input.
6	SDA	I^2C data input.
7	SS	Soft-start time setting. Connect an external capacitor to GND.
8	FB	Feedback voltage input. Connect to output voltage feedback resistor divider.
9	VS	Output voltage controlled by VID.
10	AGND	Analog ground.
11, 12, 21 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
13, 14, 15	SW	Switch node.
16, 17	VIN	Power input. Connect to high-side MOSFET Drain.
18	VCC	Power input for internal circuit.
19	EN	Enable control Input.
20	BOOT	Bootstrap supply for high-side gate driver. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BS pins to form a floating supply across the power switch driver. A 0.1μF capacitor is recommended for use.

Functional Block Diagram



Operation

The RT6203B is a high-performance 700kHz 5A step-down regulator with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with ceramic output capacitors without complicated external compensation, among other benefits. The ACOT™ control mode also provides fast transient response, especially for low output voltages and low duty cycles. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.8V to 8V. The proprietary ACOT™ control scheme improves upon other constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. The RT6203B are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

Constant On-Time (COT) Control

The heart of any COT architecture is the on-time one shot. Each on-time is a pre-determined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions can be considered. This arrangement avoids the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays. Traditional current mode or voltage mode control schemes typically must monitor the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine when to turn off the high-side switch

and turn on the synchronous rectifier. Weighing these small signals in a switching environment is difficult to do just after switching large currents, making those architectures problematic at low duty cycles and in less than ideal board layouts. Because no switching decisions are made during noisy time periods, COT architectures are preferable in low duty cycle and noisy applications. However, traditional COT control schemes suffer from some disadvantages that preclude their use in many cases. Many applications require a known switching frequency range to avoid interference with other sensitive circuitry. True constant on-time control, where the on-time is actually fixed, exhibits variable switching frequency. In a step-down converter, the duty factor is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage. Modern pseudo-fixed frequency COT architectures greatly improve COT by making the one-shot on-time proportional to V_{OUT} and inversely proportional to V_{IN}. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions. The result is a big improvement but the switching frequency still varies considerably over line and load due to losses in the switches and inductor and other parasitic effects. Another problem with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly-desirable, small, low-cost, but low-ESR ceramic capacitors. Most COT architectures use AC current information from the output capacitor, generated by the inductor current passing through the ESR, to function in a way like a current mode control system. With ceramic capacitors the inductor current information is too small to keep the control loop stable, like a current mode system with no current information.

ACOT™ Control Architecture

Making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage. As the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on time and causes the switching frequency to drop noticeably. One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range. To achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT™ One-Shot Operation

The RT6203B control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference and the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (230ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Shutdown, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When V_{EN} is below this level the IC enters shutdown mode and supply current drops to less than 10μA. When V_{EN} exceeds its logic-high level of 2V the IC is fully operational. Unlike many competing devices, EN is a high voltage input that can be safely connected to V_{IN} (up to 18V) for automatic start-up.

Input Under-Voltage Lockout

In addition to the enable function, the RT6203B feature an Under-Voltage Lockout (UVLO) function that monitors the internal linear regulator output (PVCC). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when V_{CC} drops below the UVLO falling threshold. The IC resumes switching when V_{CC} exceeds the UVLO rising threshold.

Soft-Start (SS)

The RT6203B soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After V_{EN} is high and V_{IN} exceeds its UVLO threshold, the IC begins to source 6μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. Following below equation to get the minimum capacitance range in order to avoid UV occurs.

$$t = \frac{C_{OUT} \times V_{OUT} \times 0.75 \times 1.2}{(I_{LIM} - \text{Load Current}) \times 0.8}$$

$$C_{SS} \geq \frac{t \times 6\mu A}{V_{REF}}$$

Do not leave SS unconnected. During start-up the SS capacitor is charged and the RT6203B operates in discontinuous switching mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to some positive level before start-up. Once the V_{SS} ramp charges enough to raise the internal reference above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated level. After V_{SS} rises above about 2.2V output over- and under-voltage protections are enabled and the RT6203B begins continuous-switching operation.

Internal Regulator (PVCC)

An internal linear regulator (PVCC) produces a 5V supply from V_{IN}. The 5V power supplies the internal control circuit, such as internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. 1μF ceramic capacitor for decoupling and stability is required.

Over-Temperature Protection

The RT6203B includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 20V
- Switch Voltage, SW ---------- –0.3V to 20.3V
- BOOT Voltage ---------- – 0.3V to 26.3V
- Enable Voltage, EN ---------- –0.3V to 20V
- Boot to Switch Voltage, Boot – SW ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 4x4 ---------- 3.57W
- Package Thermal Resistance (Note 2)
  WQFN-20L 4x4, θ_{JA} ---------- 28°C/W
  WQFN-20L 4x4, θ_{Jc} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

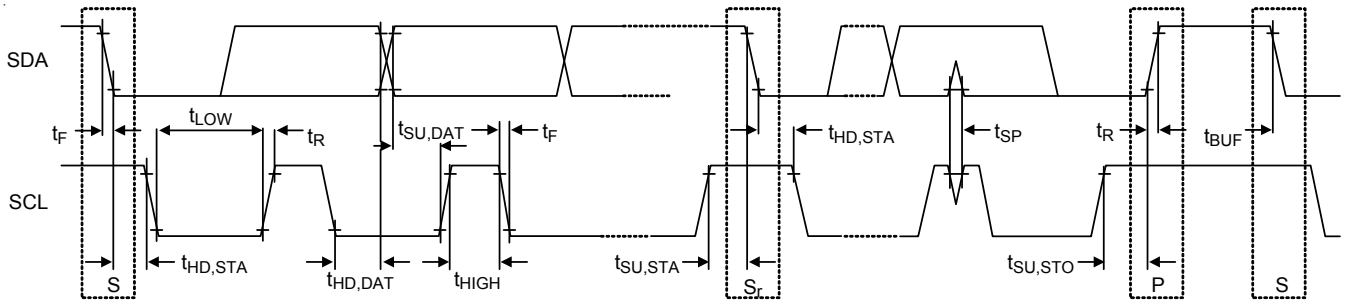
Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.5	10	μA
Shutdown Current by VID		I_{SHDN_VID}	Special code = 1110110	--	75	105	μA
Quiescent Current		I_Q	V_{EN} = 2V, V_{FB} = 1V	--	0.55	1.2	mA
Logic Threshold							
EN Input Voltage	Logic-Low	V_{IL}		--	--	0.4	V
	Logic-High	V_{IH}		2	--	--	
EN Pull-High Current				--	1	--	μA
V_{FB} Voltage and Discharge Resistance							
Feedback Voltage		V_{FB}	Regulation mode	0.792	0.8	0.808	V
Output Voltage		V_{OUT}	I^2C mode	Ideal V_{OUT} –1.5%	Ideal V_{OUT}	Ideal V_{OUT} +1.5%	V
Minimum Output Voltage Rising Time per 10mV			Special code = 1100001 (default)	--	1	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Output Voltage Rising Time per 10mV		Special code = 1101000	--	8	--	μs
V_{PVCC} Output						
V_{PVCC} Output Voltage	V_{PVCC}	6V = V_{IN} = 18V, 0 < I_{PVCC} < 5mA	4.8	5	5.2	V
Line Regulation	ΔV_{LINE}	6V = V_{IN} = 18V, I_{PVCC} = 5mA	--	--	20	mV
Load Regulation	ΔV_{LOAD}	0 < I_{PVCC} < 5mA	--	--	30	mV
Output Current	I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	100	210	--	mA
$R_{DS(ON)}$						
Switch-On Resistance	$R_{DS(ON)\_H}$	V_{BOOT} – V_{SW} = 5V	--	60	100	mΩ
	$R_{DS(ON)\_L}$		--	30	50	
Current Limit						
Current Limit	I_{LIM}	Special code = 1110000 (default)	5.8	7	8.2	A
		Special code = 1110001	4.15	5	5.85	
		Special code = 1110010	2.4	3	3.6	
On-Time Timer Control						
Switching Frequency	f_{SW}		--	700	--	kHz
Minimum Off-Time	$t_{OFF(MIN)}$		--	230	--	ns
Soft-Start						
SS Charge Current		V_{SS} = 0V	5	6	7	μA
UVLO						
UVLO Threshold		Wake Up V_{PVCC}	3.55	3.85	4.15	V
		Hysteresis	--	0.4	--	
Power Good						
PGOOD Threshold		FB rising	90	92.5	95	%
		FB falling	--	87.5	--	%
PGOOD Fault Delay		Special code = 1111001 (default)	--	10	--	μs
PGOOD Sink Current		PGOOD = 0.5V	5	--	--	mA
Output Under-Voltage and Over-Voltage Protection						
OVP Trip Threshold		OVP detect	120	125	130	%
OVP Prop Delay			--	120	--	μs
UVP Trip Threshold		OVP detect	70	75	80	%
UVP Prop Delay			--	250	--	μs
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Special Code = 1110011 (default)	--	150	--	°C
		Special Code = 1110100	--	130	--	
		Special Code = 1110101	--	110	--	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Serial Interface (SDA AND SCL pins) Note 5							
Low Level Input Voltage	Low-Level	V_{IL}		--	--	0.9	V
	High-Level	V_{IH}		2.5	--	--	
Hysteresis of Schmitt Trigger Inputs		V_{HYS}		0.16	--	--	V
Low Level SDA Output Voltage (Open drain, 3mA sink current)		V_{OL1}		--	--	0.4	V
Pulse Width of Spikes Suppressed by Input Filter		t_{SP}		50	--	--	ns
SCL Clock Frequency		f_{SCL}		--	--	400	kHz
Hold Time (repeated) Start Condition		$t_{HD;STA}$		0.6	--	--	μs
Low Period of SCL Clock		t_{LOW}		1.3	--	--	μs
High Period of SCL Clock		t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated Start Condition		$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time		$t_{HD;DAT}$		50	--	900	ns
Data Set-Up Time		$t_{SU;DAT}$		100	--	--	ns
Rise Time (SDA or SCL)		t_R		20 + 0.1C_b	--	300	ns
Fall time (SDA or SCL)		t_F		20 + 0.1C_b	--	300	ns
Set-Up Time for STOP Condition		$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between STOP and START Condition		t_{BUF}		1.3	--	--	μs
Capacitive Load for Each Bus Line		C_b		--	--	400	pF



Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

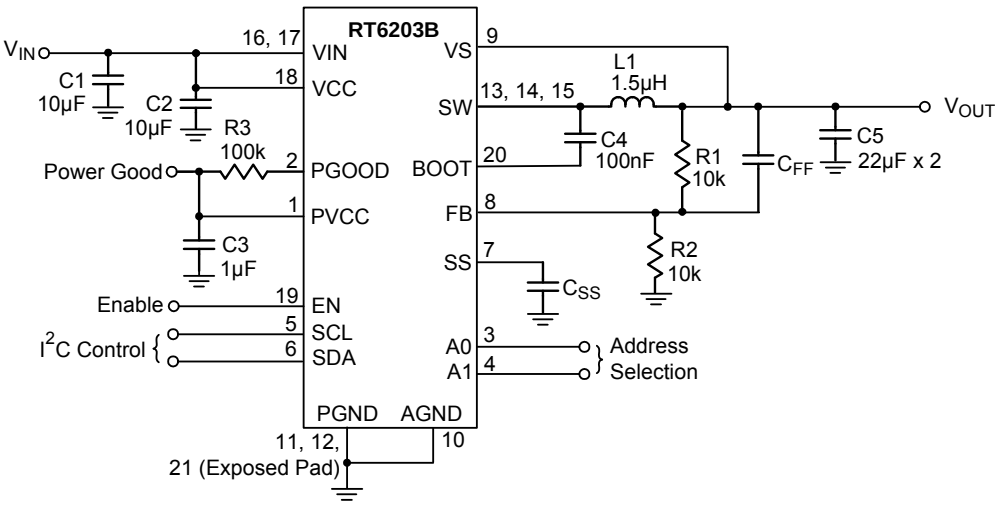
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

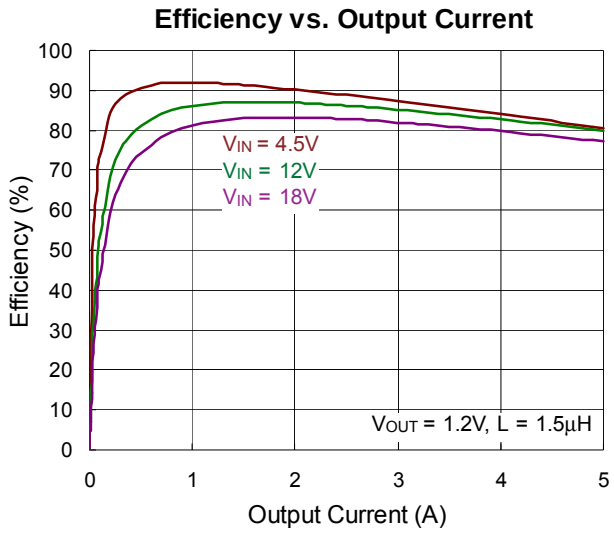
Note 4. The device is not guaranteed to function outside its operating conditions.

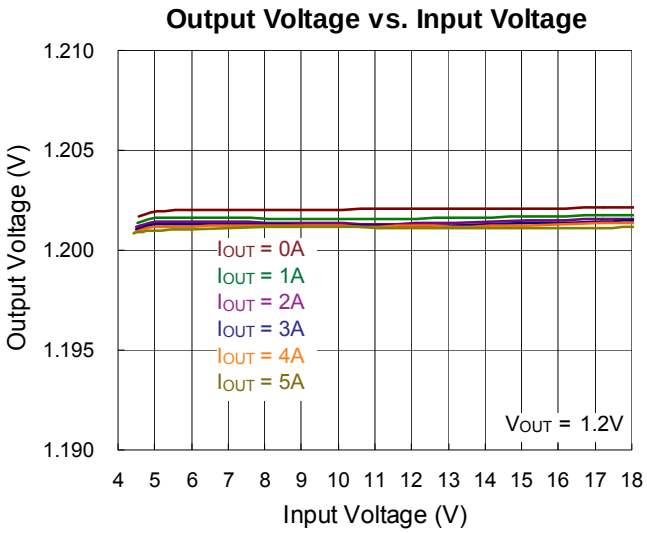
Note 5. Guaranteed by design and characterized.

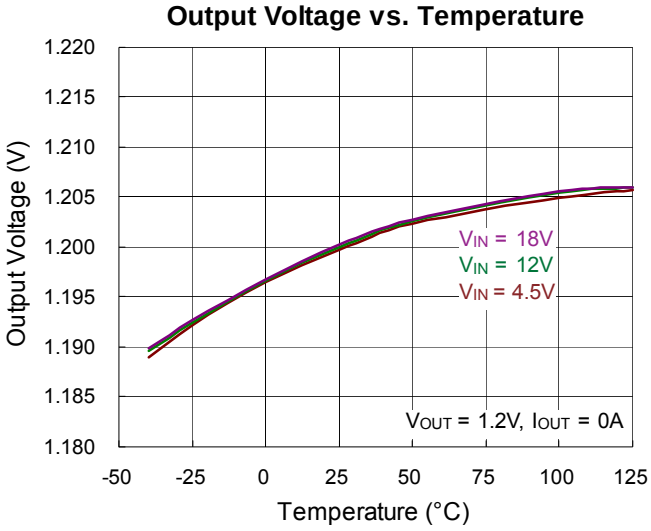
Typical Application Circuit

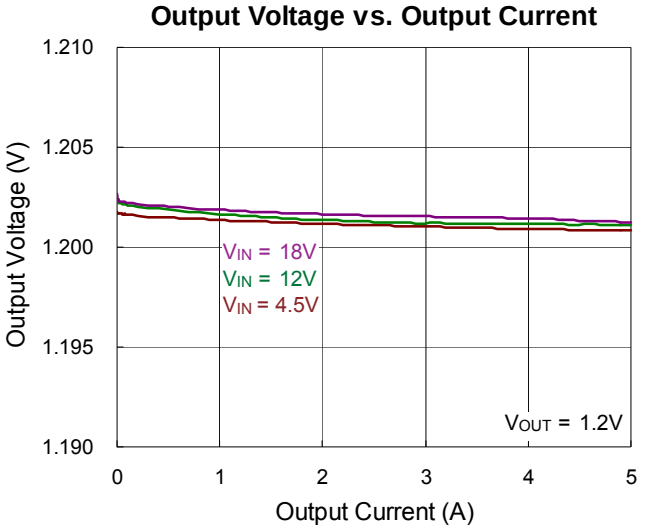


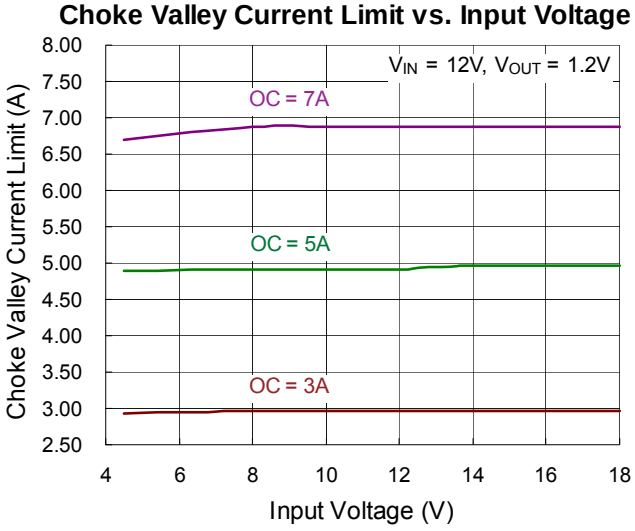
Typical Operating Characteristics

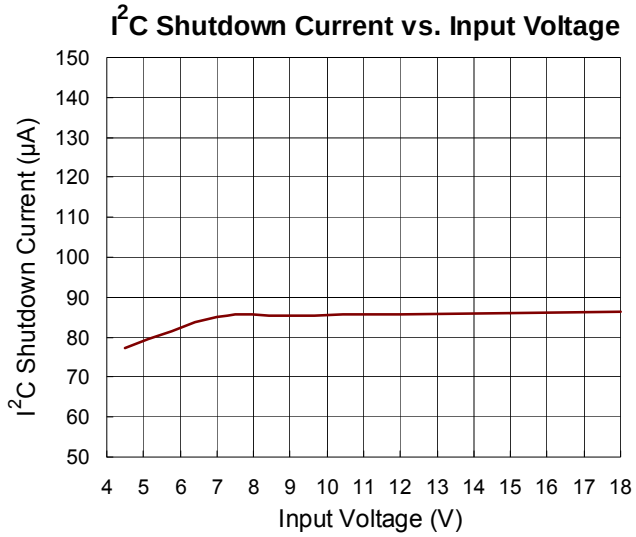




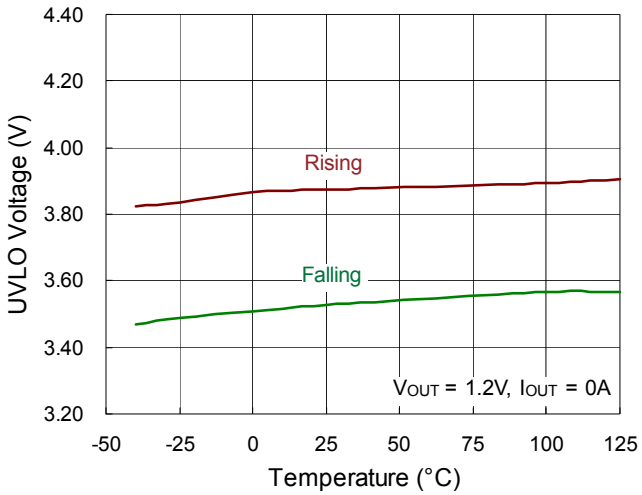




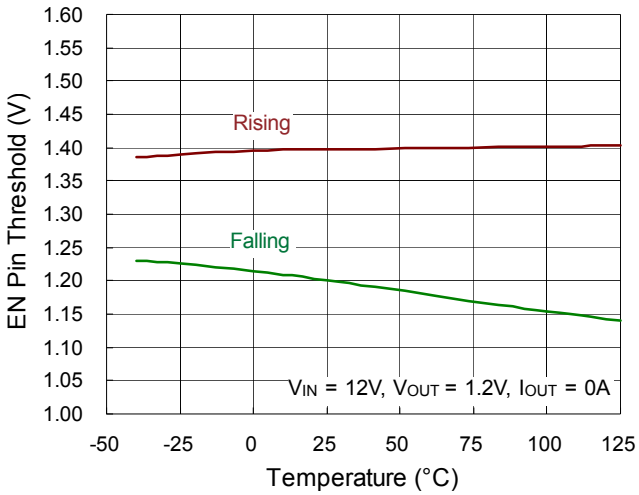




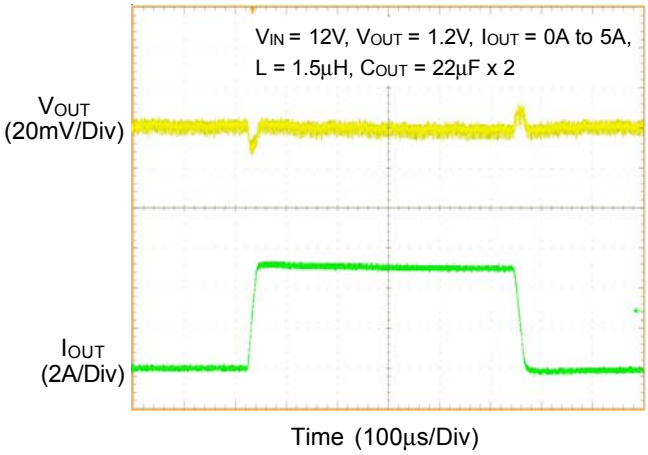
UVLO Voltage vs. Temperature



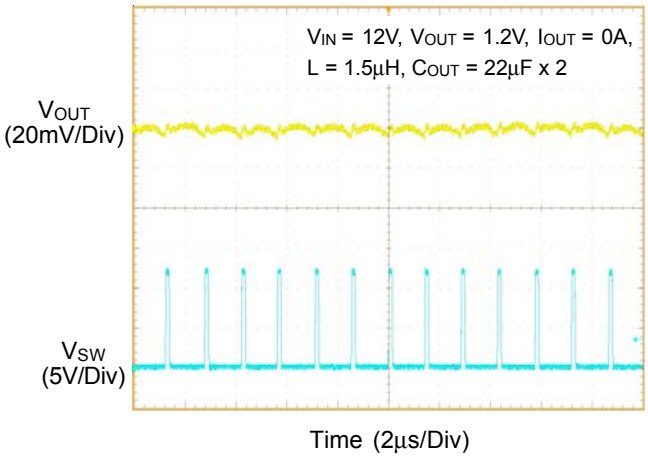
EN Pin Threshold vs. Temperature



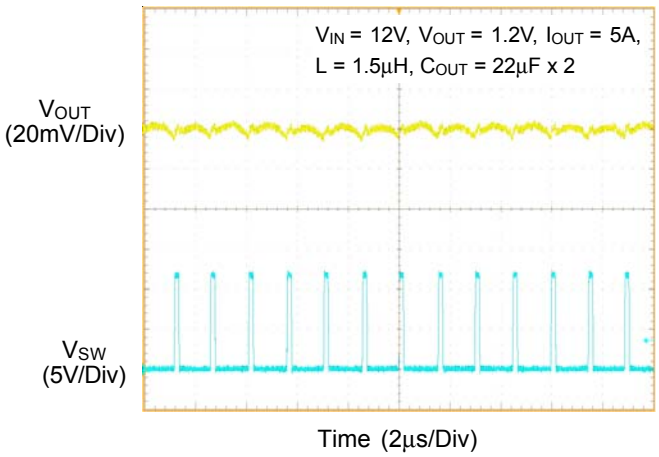
Load Transient Response



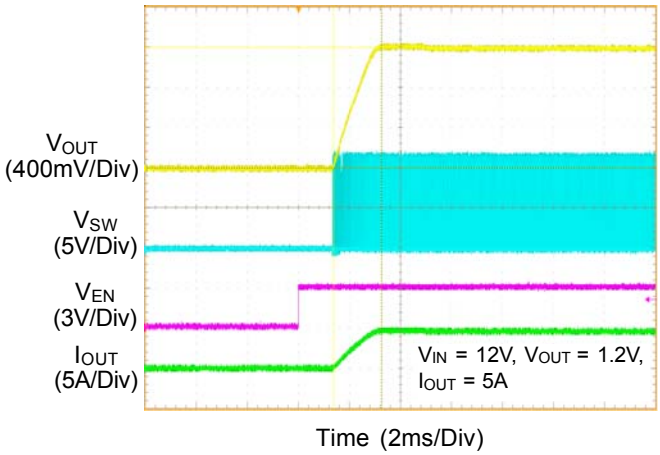
Output Ripple Voltage



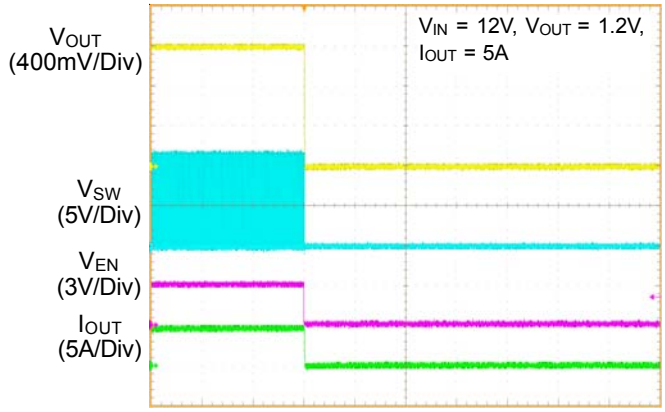
Output Ripple Voltage



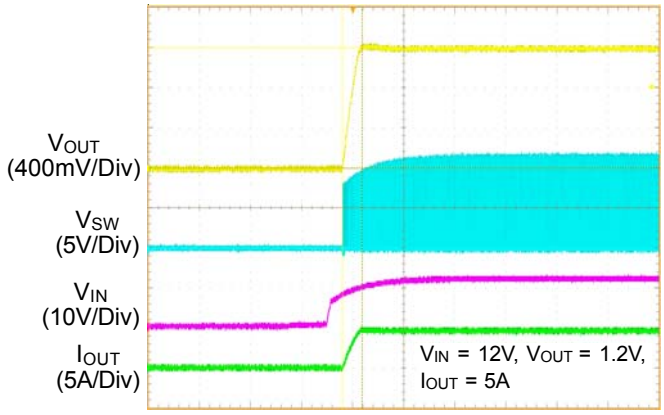
Power On from EN



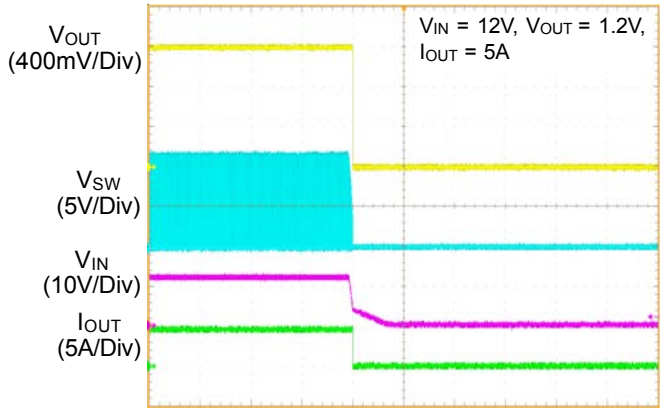
Power Off from EN



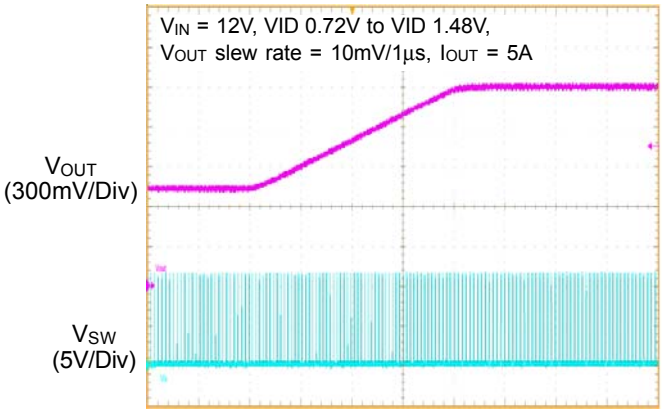
Power On from VIN



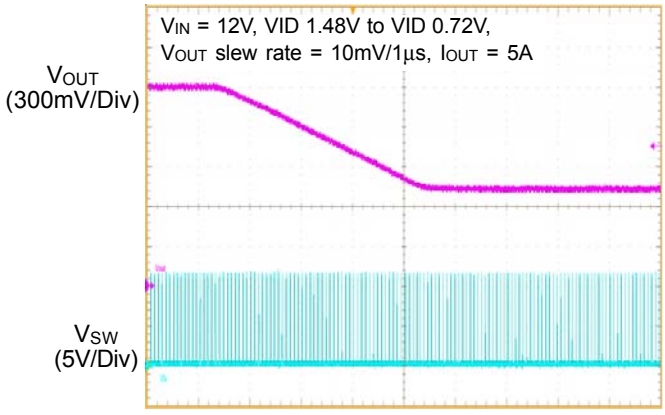
Power Off from VIN



VID Rising



VID Falling



Application Information

I²C Interface Function

The 7-bit address of the RT6203B with a WRITE operation bit can become an 8 bits I²C address byte. By using user-selectable A1 and A0 pins, there will be up to 4 the RT6203Bs been controlled on the same serial bus. Table 1 explains how to use A1/A0 and the range of the RT6203B address.

Table 1. Selectable RT6203B Address by using A1 and A0 pins

A1	A0	RT6203 Address (Binary)	RT6203 Address (Hex)
GND (0)	GND (0)	01101000	68h
GND (0)	Pull high (1)	01101010	6Ah
Pull high (1)	GND (0)	01101100	6Ch
Pull high (1)	Pull high (1)	01101110	6Eh

Table 2 is the structure of the RT6203B Data Byte. Bit0 to Bit6 are the 7-bit code for one of 77 output voltage and special function. After the soft-start time, Master can sent 8 bits data to control the V_{OUT} of the RT6203B. The voltages can be selected from table 3 and table 4 shows how to use special function. The bit7 is check-sum bit and Master should set this bit to be the Exclusive-OR of [Bit6:Bit0]. In other words, the sum is even. If not, the RT6203B will not send an ACK bit.

Table 2. Structure of RT6203B Data Byte

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ChkSum	D6	D5	D4	D3	D2	D1	D0

Table 3. VID Function

Code	Binary	V_{OUT}	Code	Binary	V_{OUT}	Code	Binary	V_{OUT}
0	0000000	0.720	26	0011010	0.980	52	0110100	1.240
1	0000001	0.730	27	0011011	0.990	53	0110101	1.250
2	0000010	0.740	28	0011100	1.000	54	0110110	1.260
3	0000011	0.750	29	0011101	1.010	55	0110111	1.270
4	0000100	0.760	30	0011110	1.020	56	0111000	1.280
5	0000101	0.770	31	0011111	1.030	57	0111001	1.290
6	0000110	0.780	32	0100000	1.040	58	0111010	1.300
7	0000111	0.790	33	0100001	1.050	59	0111011	1.310
8	0001000	0.800	34	0100010	1.060	60	0111100	1.320
9	0001001	0.810	35	0100011	1.070	61	0111101	1.330
10	0001010	0.820	36	0100100	1.080	62	0111110	1.340
11	0001011	0.830	37	0100101	1.090	63	0111111	1.350
12	0001100	0.840	38	0100110	1.100	64	1000000	1.360
13	0001101	0.850	39	0100111	1.110	65	1000001	1.370
14	0001110	0.860	40	0101000	1.120	66	1000010	1.380
15	0001111	0.870	41	0101001	1.130	67	1000011	1.390
16	0010000	0.880	42	0101010	1.140	68	1000100	1.400
17	0010001	0.890	43	0101011	1.150	69	1000101	1.410
18	0010010	0.900	44	0101100	1.160	70	1000110	1.420
19	0010011	0.910	45	0101101	1.170	71	1000111	1.430
20	0010100	0.920	46	0101110	1.180	72	1001000	1.440
21	0010101	0.930	47	0101111	1.190	73	1001001	1.450
22	0010110	0.940	48	0110000	1.200	74	1001010	1.460
23	0010111	0.950	49	0110001	1.210	75	1001011	1.470
24	0011000	0.960	50	0110010	1.220	76	1001100	1.480
25	0011001	0.970	51	0110011	1.230	>76	>1001100	Illegal / Special

Table 4 shows special codes and relative function. Special codes are valid during the soft-start time.

1111111 : The V_{OUT} is controlled by I2C codes. If users want V_{OUT} to be controlled by external resistor divider, it can be done by sending the special code.

1110000 to 1110010 : To change the over current limit level.

1110011 to 1110101 : To change the over temperature protection level.

1110110 to 1110111 : To shut down and start up IC.

1111000 to 1111011 : When V_{OUT} is changed for a large step, especially at light load conditions, it maybe need a long setting time. It is easy to trig UV/OV function and will cause the fault power good signal. Users can use the special codes to set the PGOOD delay time to avoid undesired behavior.

1100001 to 1101000 : To change the V_{OUT} slew rate when it is controlled from low level voltage to high level voltage.

Table 4. Special Function

Special Codes	Function
1111111	Disable VID, return to FB control
1110000	OC = 7A (default)
1110001	OC = 5A
1110010	OC = 3A
1110011	OT = 150°C (default)
1110100	OT = 130°C
1110101	OT = 110°C
1110110	Shutdown code
1110111	Start-up code
1111000	PGOOD fault delay set to 0μs
1111001	PGOOD fault delay set to 10μs (default)
1111010	PGOOD fault delay set to 20μs
1111011	PGOOD fault delay set to 40μs
1100001	V_{OUT} slew rate = 10mV/1μs (default)
1100010	V_{OUT} slew rate = 10mV/2μs
1100011	V_{OUT} slew rate = 10mV/3μs
1100100	V_{OUT} slew rate = 10mV/4μs
1100101	V_{OUT} slew rate = 10mV/5μs
1100110	V_{OUT} slew rate = 10mV/6μs
1100111	V_{OUT} slew rate = 10mV/7μs
1101000	V_{OUT} slew rate = 10mV/8μs

Inductor Selection

The consideration of inductor selection includes inductance, RMS current rating and, saturation current rating. The inductance selection is generally flexible and is optimized for the low cost, low physical size, and high system performance.

Choosing lower inductance to reduce physical size and cost, and it is useful to improve the transient response. However, it causes the higher inductor peak current and output ripple voltage to decrease system efficiency. Conversely, higher inductance increase system efficiency, but the physical size of inductor will become larger and transient response will be slow because more transient time is required to change current (up or down) by inductor. A good compromise between size, efficiency, and transient response is to set a inductor ripple current (ΔI_L) about 20% to 50% of the desired full output load current.

Calculate the approximate inductance by the input voltage, output voltage, switching frequency (f_{SW}), maximum rated output current ($I_{OUT(MAX)}$) and inductor ripple current (ΔI_L).

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current can be calculated.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} \Delta I_L$$

$$I_{L(VALLY)} = I_{OUT(MAX)} - \frac{1}{2} \Delta I_L$$

The typical operating circuit design for the RT6203B, the output voltage is 1.2V, maximum rated output current is 5A, input voltage is 12V, and inductor ripple current is 1A which is 20% of the maximum rated output current, the calculated inductance value is :

$$L = \frac{1.2 \times (12 - 1.2)}{12 \times 700 \times 10^3 \times 1} = 1.53\mu H$$

The inductor ripple current can be set larger than 1A and so we select 1.5µH inductance. The actual inductor ripple current and required peak current is shown as below :

$$\Delta I_L = \frac{1.2 \times (12 - 1.2)}{12 \times 700 \times 10^3 \times 1.5 \times 10^{-6}} = 1.02A$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{1}{2} \Delta I_L = 5 + \frac{1}{2} = 5.5A$$

Inductor saturation current should be chosen over IC's current limit. Set valley current limit of the RT6203B is 7A by I^2C. When touching current limit of the RT6203B, the peak inductor current is :

$I_{L(PEAK)} = I_{L(VALLEY)} + \Delta I_L = 7 + 1 = 8A$

It will be safe to choose inductor saturation current larger than 8.1A.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the RMS input ripple current drawn from the input power source and ripple voltage seen at the input of the converter. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It's also important to consider the ripple current capabilities of capacitors.

The RMS input ripple current (I_{RMS}) is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) :

$$I_{RMS} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The maximum RMS input ripple current occurs at maximum output load and it needs to be concerned about the ripple current capabilities of capacitors at maximum output load.

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. It should pay attention that value of capacitors change as temperature, bias voltage, and operating frequency change. For example the capacitance value of a capacitor decreases as the dc bias across the capacitor increases.

However, take care when these capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long and thin wires. Current surges through the inductive wires can induce ringing at the IC's power input which could potentially cause large, damaging voltage spikes at VIN pin. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors can be placed in parallel with other types such as tantalum, electrolytic, or polymer to

reduce voltage ringing and overshoot.

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application.

Output Capacitor Selection

The RT6203B is optimized for output terminal with ceramic capacitors application and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output ripple voltage level and transient response requirements for sag which is undershoot on positive load steps and soar which is overshoot on negative load steps.

Output Ripple Voltage

Output ripple voltage at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple.

Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Output Transient Undershoot and Overshoot

In addition to output ripple voltage at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT™ transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency.

But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Output Voltage Setting

The output voltage is set by a resistive divider from the output to ground with the midpoint connected to FB. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1, and the output voltage can be calculated by the following equation :

$$V_{OUT} = 0.8V \times (1 + \frac{R1}{R2})$$

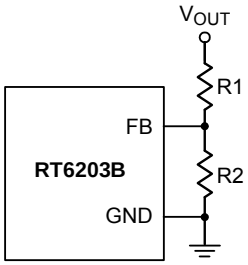


Figure 1. Output Voltage Setting

The placement of resistive divider components should be within 5mm of the FB pin. In order to minimize the power consumption at light loads and reduce the noise injected from FB pin, The suggested value of R2 is between 10kΩ and 100kΩ. For output voltage accuracy, use divider resistors with 1% or better tolerance.

Enable Operation (EN)

EN is a high voltage input pin. For automatic start-up, the EN pin can be connected to VIN directly. The inherent hysteresis makes EN useful as a simple timing delay. To add an additional time delay, the EN pin can be connected to GND through a capacitor C_{EN}, as shown in Figure 2. The additional time delay for switching operation to start can be calculated with the EN's internal logic threshold. (typically 2V).

An external MOSFET can be added to implement an logic-controlled EN pin, as shown in Figure 3. The MOSFET Q1 can provide the logic control on the EN pin, pulling it down. To prevent enabling circuit when V_{IN} is smaller than the V_{OUT} target value or some other desired voltage level, a resistive divider can be placed to control the EN voltage as the additional input under voltage lockout function, as shown in Figure 4.

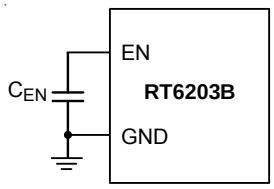


Figure 2. Enable Timing Control

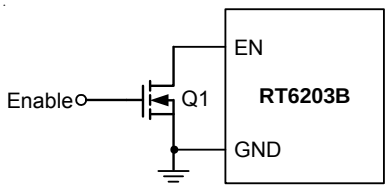


Figure 3. Logic Control for the EN Pin

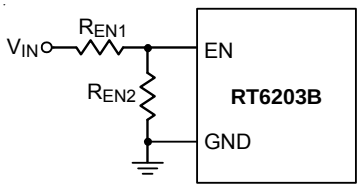


Figure 4. Resistor Divider for Lockout Threshold Setting

External Soft-Start Function

The RT6203B provides an adjustable soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The soft-start timing is the output voltage rising time from 0V to settled level and can be programmed by the external capacitor between the SS and GND pins. An internal current source I_{SS} (typically, 6μA) charges the external capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start. The typical soft-start time can be calculated as follows :

$$\text{Soft-Start Time } t_{SS}(ms) = \frac{C_{SS}(nF) \times V_T}{I_{SS}\ (\mu A)}$$

$$= \frac{C_{SS}(nF) \times 1.3}{6\mu A}$$

For example, If a 10nF capacitor is used, the typical soft-start will be 2.16ms. Do not leave SS unconnected.

Power-Good Output

The PGOOD pin is an open-drain power-good output and requires an external pull-up resistor, connected to an external supply or the on-chip PVCC output. When the

output voltage drops below 87.5% of its nominal voltage, PGOOD will be pulled low. It will be held low until the output voltage rises to 92.5% of the nominal voltage. During soft-start and in shutdown mode (EN pin pull low), PGOOD is actively held low. When the output voltage has reached 90% of its nominal voltage and the soft-start sequence is finished, PGOOD is high impedance and will be pulled high by the external pull-up resistor.

External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high-side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V. The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT6203B Note that the external boot voltage must be lower than 5.5V.

External BOOT Capacitor Series Resistor

The internal power MOSFET gate driver is not only optimized to turn the switch on fast enough to minimize switching loss, but also slow enough to reduce EMI. Since the switch rapidly turn-on will induce high di/dt noise which let EMI issue much worse. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead time between high-side and low-side switch on-times. In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<47Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on speed and V_{SW}'s rise. The recommended external diode connection is shown in Figure 5, using external diode to charge the BOOT capacitor, and place a resistor between BOOT and the capacitor/diode connection to reduce turn-on speed for any EMI issue consideration.

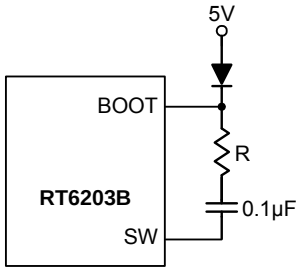


Figure 5. External Bootstrap Diode and BOOT Capacitor Series Resistor

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 4x4 package, the thermal resistance, θ_{JA}, is 28°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28°C/W) = 3.57W for a WQFN-20L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

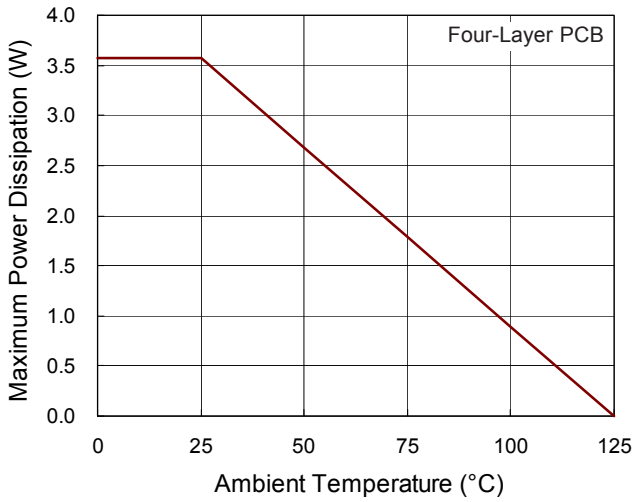
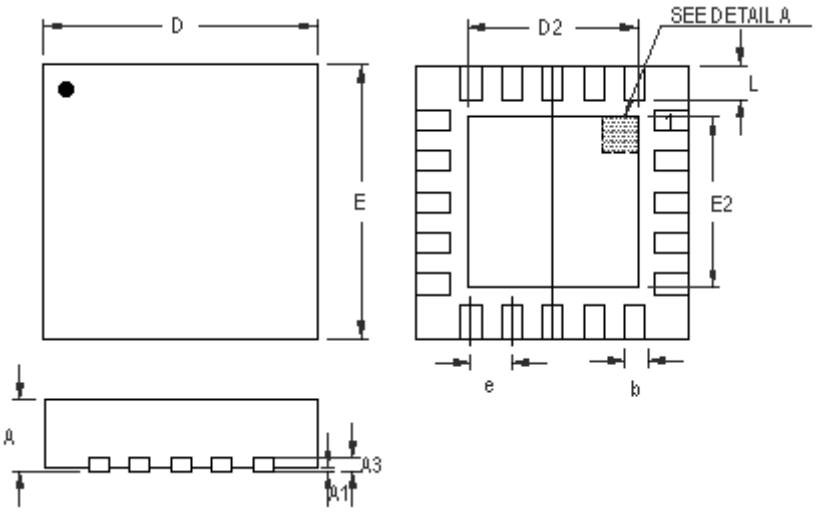
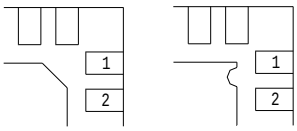


Figure 6. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.300	0.006	0.012
D		3.900	4.100	0.154	0.161
D2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
E		3.900	4.100	0.154	0.161
E2	Option 1	2.650	2.750	0.104	0.108
	Option 2	2.100	2.200	0.083	0.087
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 20L QFN 4x4 Package

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