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14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC)

Data Sheet **AD9643**

FEATURES

- SNR = 70.6 dBFS at 185 MHz A_{IN} and 250 MSPS
- SFDR = 85 dBc at 185 MHz A_{IN} and 250 MSPS
- −151.6 dBFS/Hz input noise at 185 MHz, −1 dBFS A_{IN} and 250 MSPS
- Total power consumption: 785 mW at 250 MSPS
- 1.8 V supply voltages
- LVDS (ANSI-644 levels) outputs
- Integer 1-to-8 input clock divider (625 MHz maximum input)
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal ADC voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMax, WCDMA, CDMA2000, GSM, EDGE, LTE
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Ultrasound equipment
- Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

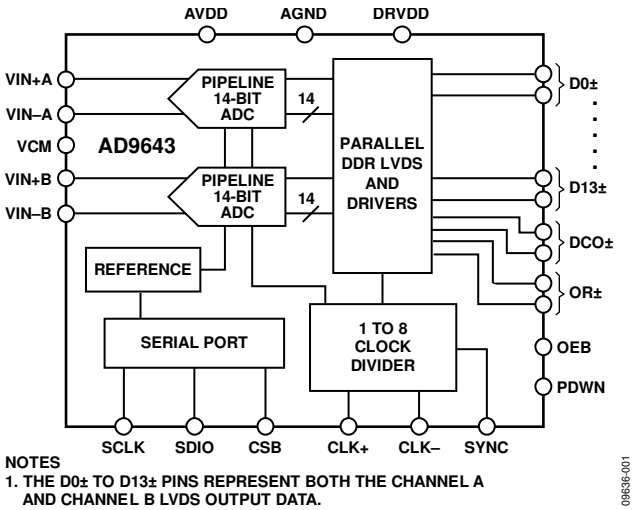

Figure 1.

GENERAL DESCRIPTION

The AD9643 is a dual, 14-bit analog-to-digital converter (ADC) with sampling speeds of up to 250 MSPS. The AD9643 is designed to support communications applications, where low cost, small size, wide bandwidth, and versatility are desired.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data is routed directly to the two external 14-bit LVDS output ports and formatted as either interleaved or channel multiplexed.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface.

The AD9643 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 170 MSPS/210 MSPS/250 MSPS ADCs.
2. Operation from a single 1.8 V supply and a separate digital output driver supply accommodating LVDS outputs.
3. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
4. SYNC input allows synchronization of multiple devices.
5. 3-pin, 1.8 V SPI port for register programming and register readback.
6. Pin compatibility with the AD9613, allowing a simple migration down from 14 bits to 12 bits. This part is also pin compatible with the AD6649 and the AD6643.

Rev. E

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AD9643* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9643 Evaluation Board
- FPGA Mezzanine Card for Wireless Communications

DOCUMENTATION

Application Notes

- AN-1142: Techniques for High Speed ADC PCB Layout
- AN-282: Fundamentals of Sampled Data Systems
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-501: Aperture Uncertainty and ADC System Performance
- AN-586: LVDS Outputs for High Speed A/D Converters
- AN-737: How ADIsimADC Models an ADC
- AN-741: Little Known Characteristics of Phase Noise
- AN-742: Frequency Domain Response of Switched-Capacitor ADCs
- AN-756: Sampled Systems and the Effects of Clock Phase Noise and Jitter
- AN-807: Multicarrier WCDMA Feasibility
- AN-808: Multicarrier CDMA2000 Feasibility
- AN-827: A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs
- AN-835: Understanding High Speed ADC Testing and Evaluation
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-877: Interfacing to High Speed ADCs via SPI
- AN-878: High Speed ADC SPI Control Software
- AN-905: Visual Analog Converter Evaluation Tool Version 1.0 User Manual
- AN-935: Designing an ADC Transformer-Coupled Front End

Data Sheet

- AD9643: 14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Dual Analog-to-Digital Converter (ADC) Data Sheet

Technical Books

- The Data Conversion Handbook, 2005

User Guides

- UG-293: Evaluating the AD9643/AD9613/AD6649/AD6643 Analog-to-Digital Converters

TOOLS AND SIMULATIONS

- Visual Analog
- AD9643 IBIS Model
- AD9643 LFCSP Analog Input S-Parameter

REFERENCE DESIGNS

- CN0242

REFERENCE MATERIALS

Press

- Avnet Electronics Marketing Americas and Analog Devices Introduce the Agile Zynq™- 7000 EPP/Analog Devices Software-Defined Radio Kit

Product Selection Guide

- RF Source Booklet

Technical Articles

- MS-1779: Nine Often Overlooked ADC Specifications
- MS-2124: Understanding AC Behaviors of High Speed ADCs
- MS-2210: Designing Power Supplies for High Speed ADC

Tutorials

- MT-001: Taking the Mystery out of the Infamous Formula, "SNR=6.02N + 1.76dB", and Why You Should Care
- MT-002: What the Nyquist Criterion Means to Your Sampled Data System Design
- MT-031: Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"
- MT-075: Differential Drivers for High Speed ADCs Overview
- MT-230: Noise Considerations in High Speed Converter Signal Chains

DESIGN RESOURCES

- AD9643 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9643 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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4/11—Revision 0: Initial Version

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, unless otherwise noted.

Table 1.

		AD9643-170			AD9643-210			AD9643-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full			±10			±10			±10	mV
Gain Error	Full			+2/−6			+3/−5			±4	%FSR
Differential Nonlinearity (DNL)	Full			±0.75			±0.75			±0.75	LSB
	25°C		±0.25			±0.25			±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±1.8			±2			±3.5	LSB
	25°C		±1.5			±1.5			±1.5		LSB
MATCHING CHARACTERISTIC											
Offset Error	Full			±13			±13			±13	mV
Gain Error	Full			±2.5/ +3.5			−2/ +3.5			−2.5/ +3.5	%FSR
TEMPERATURE DRIFT											
Offset Error	Full		±5			±5			±5		ppm/°C
Gain Error	Full		±70			±80			±100		ppm/°C
INPUT REFERRED NOISE											
VREF = 1.75 V	25°C		1.33			1.33			1.33		LSB rms
ANALOG INPUT											
Input Span	Full		1.75			1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5			2.5		pF
Input Resistance[3]	Full		20			20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current											
I_{AVDD}[1]	Full		196	250		217	265		256	275	mA
I_{DRVDD}[1]	Full		145	160		160	185		180	210	mA
POWER CONSUMPTION											
Sine Wave Input (DRVDD = 1.8 V)	Full		614			680			785		mW
Standby Power[4]	Full		90			90			90		mW
Power-Down Power	Full		10			10			10		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured with a dc input and the CLK pin inactive (that is, set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, unless otherwise noted.

Table 2.

		AD9643-170			AD9643-210			AD9643-250			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)											
f_{IN} = 30 MHz	25°C		72.6			72.6			72.0		dBFS
f_{IN} = 90 MHz	25°C		72.2			72.2			71.6		dBFS
	Full	70.8			70.6						dBFS
f_{IN} = 140 MHz	25°C		71.8			71.3			71.2		dBFS
f_{IN} = 185 MHz	25°C		71.2			70.6			70.6		dBFS
	Full							68.8			dBFS
f_{IN} = 220 MHz	25°C		70.7			69.9			69.9		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)											
f_{IN} = 30 MHz	25°C		71.6			71.5			70.9		dBFS
f_{IN} = 90 MHz	25°C		71.1			71.2			70.5		dBFS
	Full	70.4			69.9						dBFS
f_{IN} = 140 MHz	25°C		70.5			70.1			69.9		dBFS
f_{IN} = 185 MHz	25°C		69.6			69.2			69.4		dBFS
	Full							67.5			dBFS
f_{IN} = 220 MHz	25°C		69.1			68.1			68.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 30 MHz	25°C		11.6			11.6			11.5		Bits
f_{IN} = 90 MHz	25°C		11.5			11.5			11.4		Bits
f_{IN} = 140 MHz	25°C		11.4			11.4			11.3		Bits
f_{IN} = 185 MHz	25°C		11.3			11.2			11.2		Bits
f_{IN} = 220 MHz	25°C		11.2			11.0			11.1		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 30 MHz	25°C		−95			−90			−90		dBc
f_{IN} = 90 MHz	25°C		−92			−90			−88		dBc
	Full			−78			−80				dBc
f_{IN} = 140 MHz	25°C		−88			−88			−86		dBc
f_{IN} = 185 MHz	25°C		−83			−87			−85		dBc
	Full									−80	dBc
f_{IN} = 220 MHz	25°C		−83			−85			−85		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 30 MHz	25°C		95			90			90		dBc
f_{IN} = 90 MHz	25°C		92			90			88		dBc
	Full	78			80						dBc
f_{IN} = 140 MHz	25°C		88			88			86		dBc
f_{IN} = 185 MHz	25°C		83			87			85		dBc
	Full							80			dBc
f_{IN} = 220 MHz	25°C		83			85			85		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 30 MHz	25°C		−98			−95			−94		dBc
f_{IN} = 90 MHz	25°C		−97			−95			−93		dBc
	Full			−78			−80				dBc
f_{IN} = 140 MHz	25°C		−97			−93			−92		dBc
f_{IN} = 185 MHz	25°C		−96			−92			−92		dBc
	Full									−80	dBc
f_{IN} = 220 MHz	25°C		−94			−90			−88		dBc

Parameter[1]	Temperature	AD9643-170 Min	AD9643-170 Typ	AD9643-170 Max	AD9643-210 Min	AD9643-210 Typ	AD9643-210 Max	AD9643-250 Min	AD9643-250 Typ	AD9643-250 Max	Unit
TWO-TONE SFDR											
f_{IN} = 184.12 MHz (−7 dBFS), 187.12 MHz (−7 dBFS)	25°C		88			88			88		dBc
CROSSTALK[2]	Full		95			95			95		dB
FULL POWER BANDWIDTH[3]	25°C		1000			1000			1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Full power bandwidth is the bandwidth of operation in which proper ADC performance can be achieved.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−10		+22	µA
Low Level Input Current	Full	−22		−10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−80		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		70	µA
Low Level Input Current	Full	−5		+5	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temp	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
LVDS Data and OR Outputs					
Differential Output Voltage (VOD), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (VOS), ANSI Mode	Full	1.15	1.22	1.35	V
Differential Output Voltage (VOD), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (VOS), Reduced Swing Mode	Full	1.15	1.22	1.35	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Temp	AD9643-170 Min	AD9643-170 Typ	AD9643-170 Max	AD9643-210 Min	AD9643-210 Typ	AD9643-210 Max	AD9643-250 Min	AD9643-250 Typ	AD9643-250 Max	Unit
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			625			625			625	MHz
Conversion Rate[1]	Full	40		170	40		210	40		250	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	5.8			4.8			4			ns
CLK Pulse Width High (t_{CH})											
Divide-by-1 Mode, DCS Enabled	Full	2.61	2.9	3.19	2.16	2.4	2.64	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled	Full	2.76	2.9	3.05	2.28	2.4	2.52	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			0.8			ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
DATA OUTPUT PARAMETERS											
LVDS Mode											
Data Propagation Delay (t_{PD})	Full		6.0			6.0			6.0		ns
DCO Propagation Delay (t_{DCO})	Full		6.7			6.7			6.7		ns
DCO-to-Data Skew (t_{SKEW})	Full	0.4	0.7	1.0	0.4	0.7	1.0	0.4	0.7	1.0	ns
Pipeline Delay (Latency)	Full		10			10			10		Cycles
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
Wake-Up Time (from Standby)	Full		10			10			10		µs
Wake-Up Time (from Power-Down)	Full		250			250			250		µs
Out-of-Range Recovery Time	Full		3			3			3		Cycles

[1] Conversion rate is the clock rate after the divider.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to the rising edge of CLK setup time	1	0.3		ns
t_{HSYNC}	SYNC to the rising edge of CLK hold time	1	0.4		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

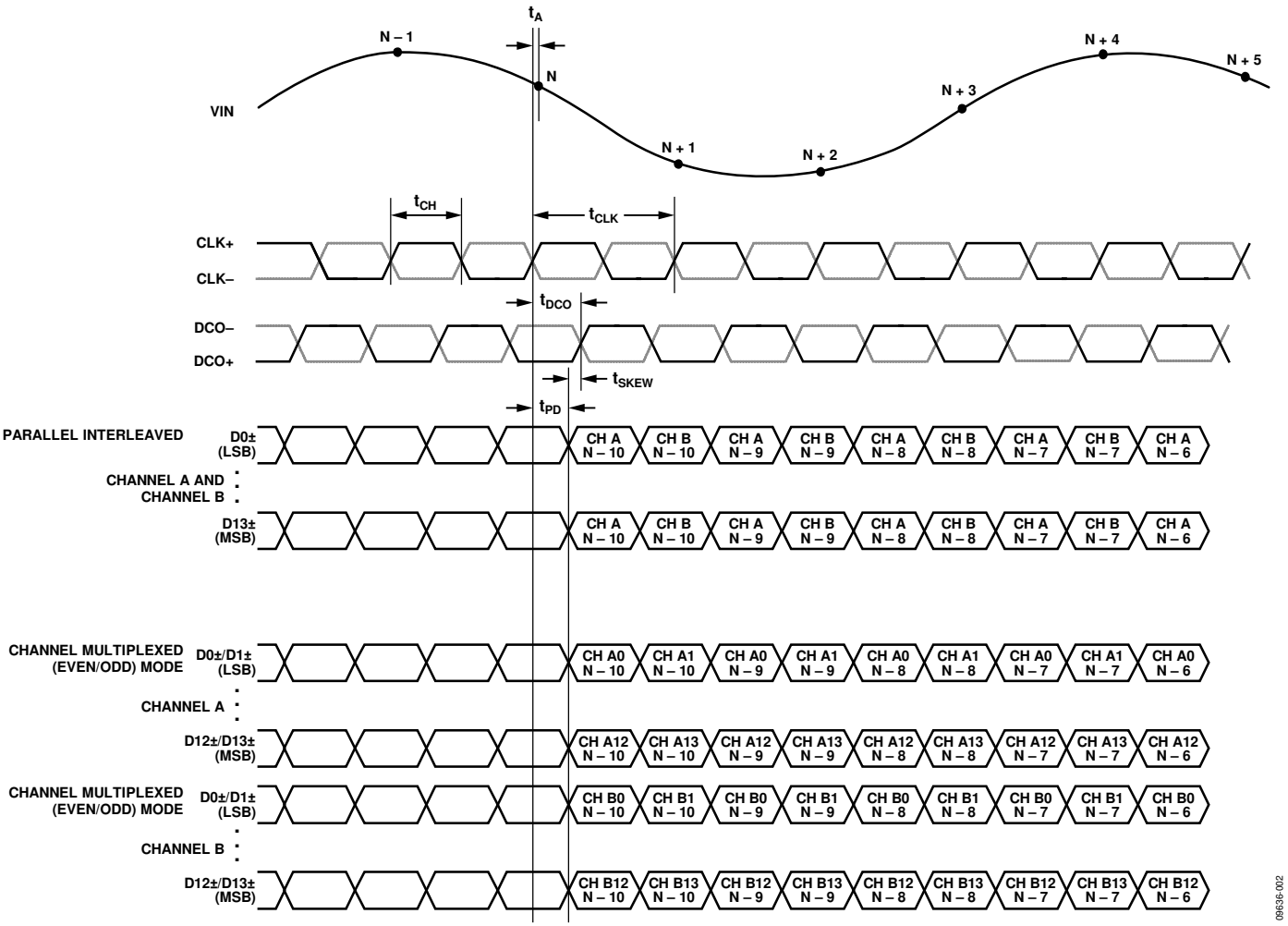

Figure 2. LVDS Modes for Data Output Timing

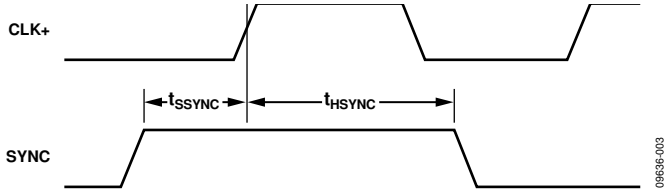

Figure 3. SYNC Timing Inputs

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.3 V
SCLK to AGND	−0.3 V to DRVDD + 0.3 V
SDIO to AGND	−0.3 V to DRVDD + 0.3 V
OEB to AGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
D0−/D0+ Through D13−/D13+ to AGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. This increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	26.8	1.14	10.4	°C/W
	1.0	21.6			°C/W
	2.0	20.2			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

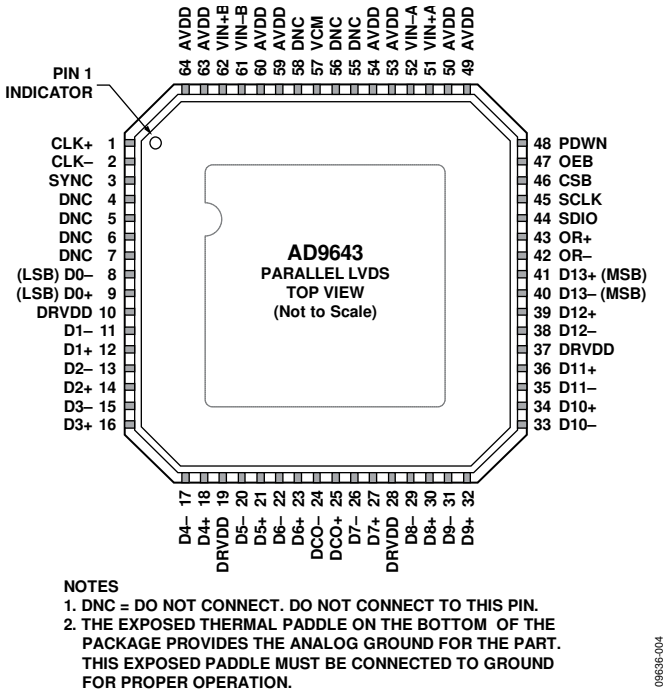

Figure 4. LFCSP Interleaved Parallel LVDS Pin Configuration (Top View)

Table 8. Pin Function Descriptions for Interleaved Parallel LVDS Mode

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7, 55, 56, 58	DNC		Do Not Connect. Do not connect to this pin.
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
9	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
8	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
12	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
11	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
14	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
13	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
16	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
15	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
18	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.

Pin No.	Mnemonic	Type	Description
17	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
21	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
20	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
23	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
22	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
30	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
29	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
32	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
31	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
34	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
33	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
36	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
35	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
39	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
38	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
41	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
40	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock.
44	SDIO	Input/Output	SPI Serial Data I/O.
46	CSB	Input	SPI Chip Select (Active Low).
Output Enable Bar and Power-Down			
47	OEB	Input/Output	Output Enable Bar Input (Active Low).
48	PDWN	Input/Output	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 14).

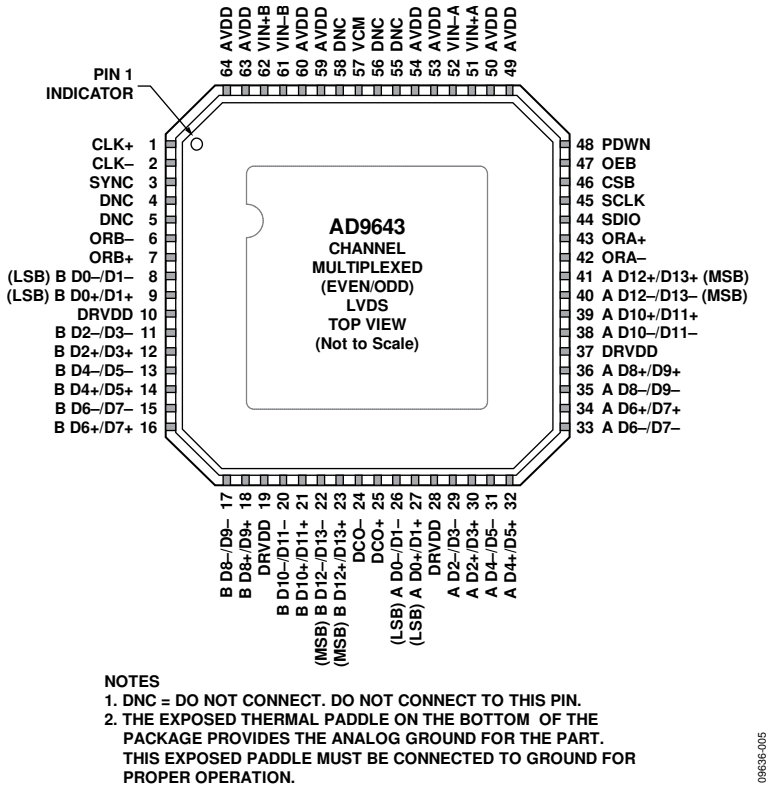

Figure 5. LFCSP Channel Multiplexed (Even/Odd) LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions for Channel Multiplexed (Even/Odd) LVDS Mode

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5	DNC		Do Not Connect. Do not connect to this pin.
0	AGND, Exposed Paddle	Ground	Analog Ground. The exposed thermal paddle on the bottom of the package provides the analog ground for the part. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	DNC		Do Not Connect. Do not connect to this pin.
56	DNC		Do Not Connect. Do not connect to this pin.
58	DNC		Do Not Connect. Do not connect to this pin.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. This pin should be decoupled to ground using a 0.1 µF capacitor.
1	CLK+	Input	ADC Clock Input—True.
2	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
7	ORB+	Output	Channel B LVDS Overrange Output—True. The overrange indication is valid on the rising edge of the DCO.
6	ORB−	Output	Channel B LVDS Overrange Output—Complement. The overrange indication is valid on the rising edge of the DCO.
8	B D0−/D1− (LSB)	Output	Channel B LVDS Output Data 0/Data 1—Complement.
9	B D0+/D1+ (LSB)	Output	Channel B LVDS Output Data 0/Data 1—True.
11	B D2−/D3−	Output	Channel B LVDS Output Data 2/Data 3—Complement.
12	B D2+/D3+	Output	Channel B LVDS Output Data 2/Data 3—True.
13	B D4−/D5−	Output	Channel B LVDS Output Data 4/Data 5—Complement.
14	B D4+/D5+	Output	Channel B LVDS Output Data 4/Data 5—True.
15	B D6−/D7−	Output	Channel B LVDS Output Data 6/Data 7—Complement.
16	B D6+/D7+	Output	Channel B LVDS Output Data 6/Data 7—True.
17	B D8−/D9−	Output	Channel B LVDS Output Data 8/Data 9—Complement.
18	B D8+/D9+	Output	Channel B LVDS Output Data 8/Data 9—True.
20	B D10−/D11−	Output	Channel B LVDS Output Data 10/Data 11—Complement.
21	B D10+/D11+	Output	Channel B LVDS Output Data 10/Data 11—True.
22	B D12−/D13− (MSB)	Output	Channel B LVDS Output Data 12/Data 13—Complement.
23	B D12+/D13+ (MSB)	Output	Channel B LVDS Output Data 12/Data 13—True.
26	A D0−/D1− (LSB)	Output	Channel A LVDS Output Data 0/Data 1—Complement.
27	A D0+/D1+ (LSB)	Output	Channel A LVDS Output Data 0/Data 1—True.
29	A D2−/D3−	Output	Channel A LVDS Output Data 2/Data 3—Complement.
30	A D2+/D3+	Output	Channel A LVDS Output Data 2/Data 3—True.
31	A D4−/D5−	Output	Channel A LVDS Output Data 4/Data 5—Complement.
32	A D4+/D5+	Output	Channel A LVDS Output Data 4/Data 5—True.
33	A D6−/D7−	Output	Channel A LVDS Output Data 6/Data 7—Complement.
34	A D6+/D7+	Output	Channel A LVDS Output Data 6/Data 7—True.
35	A D8−/D9−	Output	Channel A LVDS Output Data 8/Data 9—Complement.
36	A D8+/D9+	Output	Channel A LVDS Output Data 8/Data 9—True.
38	A D10−/D11−	Output	Channel A LVDS Output Data 10/Data 11—Complement.
39	A D10+/D11+	Output	Channel A LVDS Output Data 10/Data 11—True.
40	A D12−/D13− (MSB)	Output	Channel A LVDS Output Data 12/Data 13—Complement.
41	A D12+/D13+ (MSB)	Output	Channel A LVDS Output Data 12/Data 13—True.
43	ORA+	Output	Channel A LVDS Overrange Output—True. The overrange indication is valid on the rising edge of the DCO.
42	ORA−	Output	Channel A LVDS Overrange Output—Complement. The overrange indication is valid on the rising edge of the DCO.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK	Input	SPI Serial Clock.
44	SDIO	Input/Output	SPI Serial Data Input/Output.
46	CSB	Input	SPI Chip Select (Active Low).
Output Enable Bar and Power-Down			
47	OEB	Input	Output Enable Bar Input (Active Low).
48	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 14).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, sample rate = maximum sample rate per speed grade, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, unless otherwise noted.

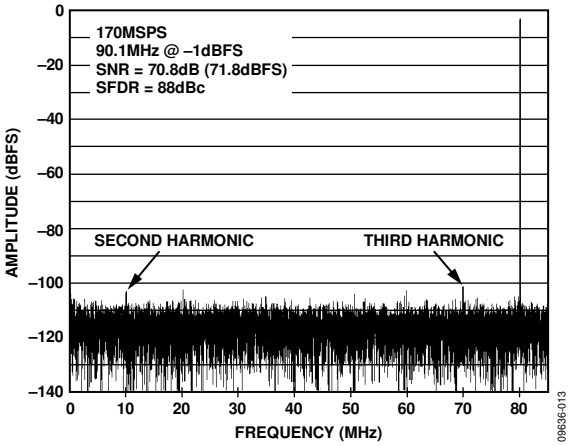

Figure 6. AD9643-170 Single-Tone FFT with f_{IN} = 90.1 MHz

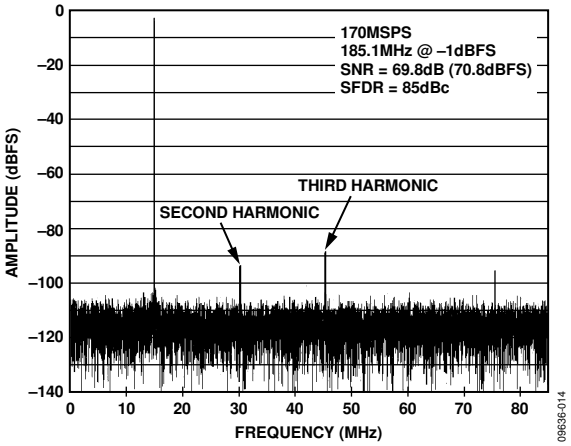

Figure 7. AD9643-170 Single-Tone FFT with f_{IN} = 185.1 MHz

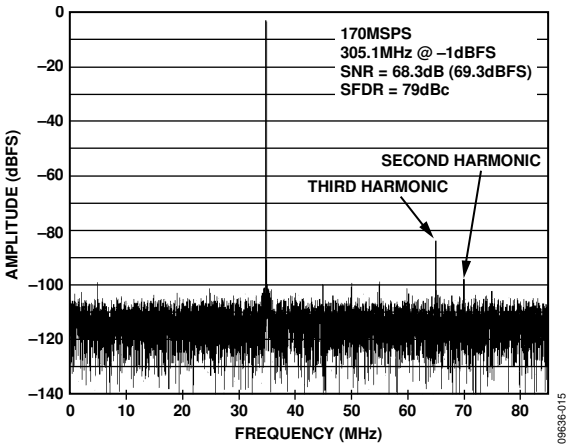

Figure 8. AD9643-170 Single-Tone FFT with f_{IN} = 305.1 MHz

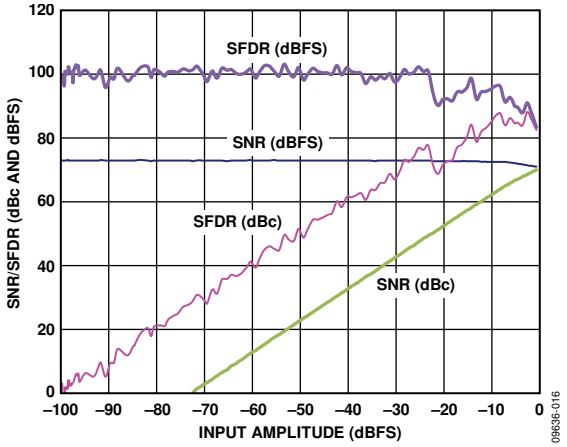

Figure 9. AD9643-170 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz

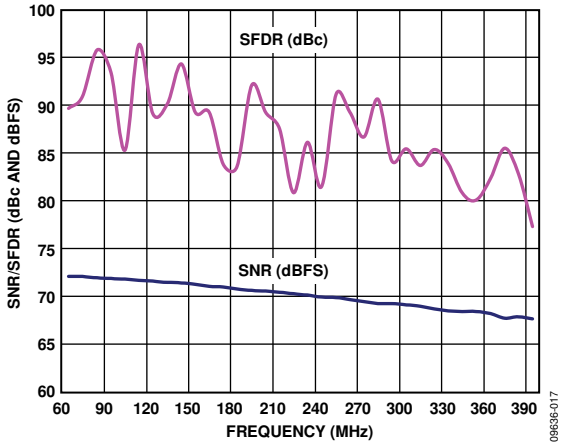

Figure 10. AD9643-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

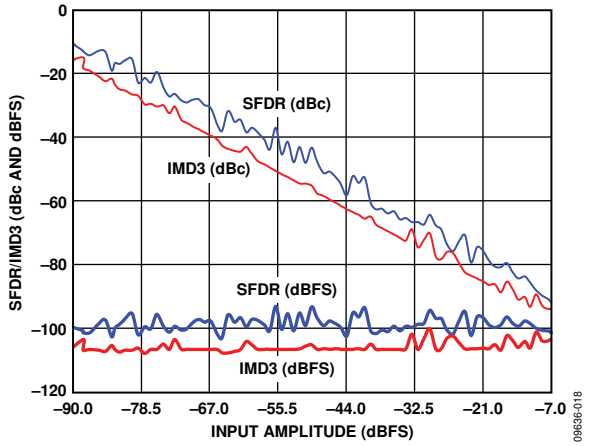

Figure 11. AD9643-170 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

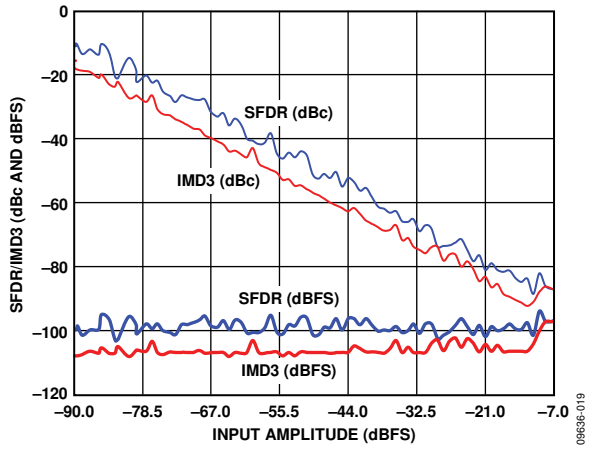

Figure 12. AD9643-170 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

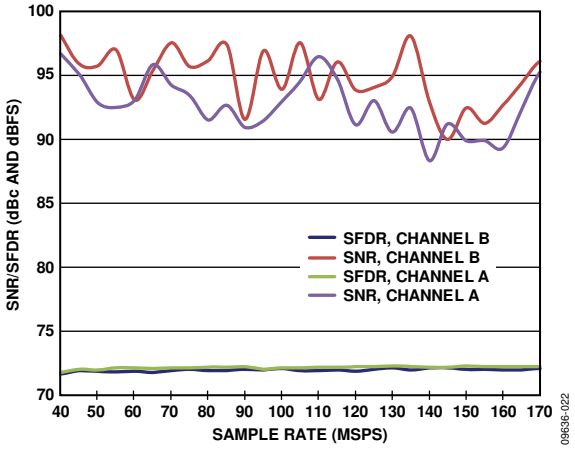

Figure 15. AD9643-170 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

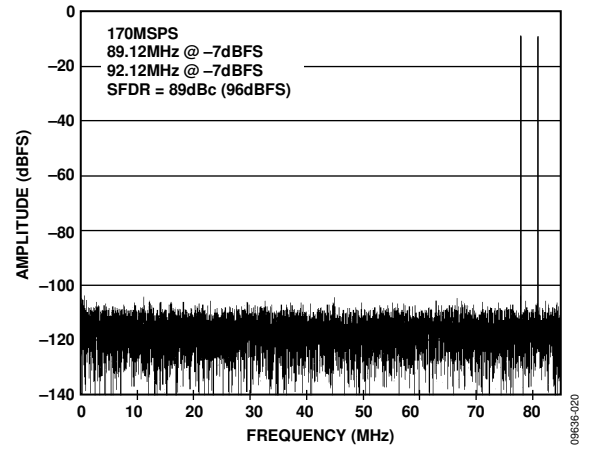

Figure 13. AD9643-170 Two-Tone FFT with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

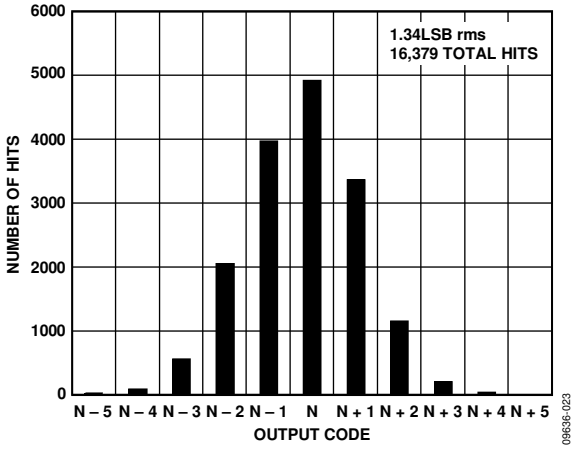

Figure 16. AD9643-170 Grounded Input Histogram

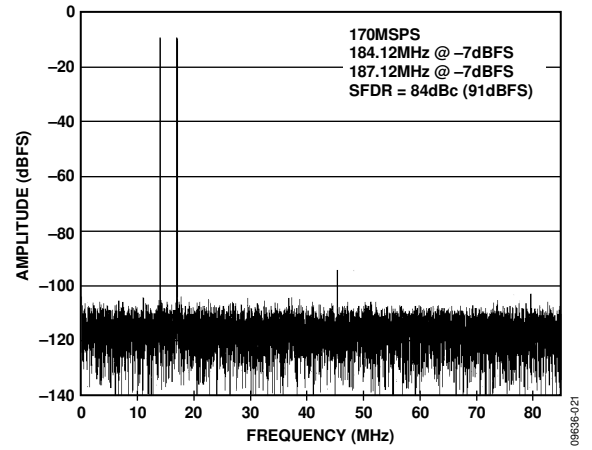

Figure 14. AD9643-170 Two-Tone FFT with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

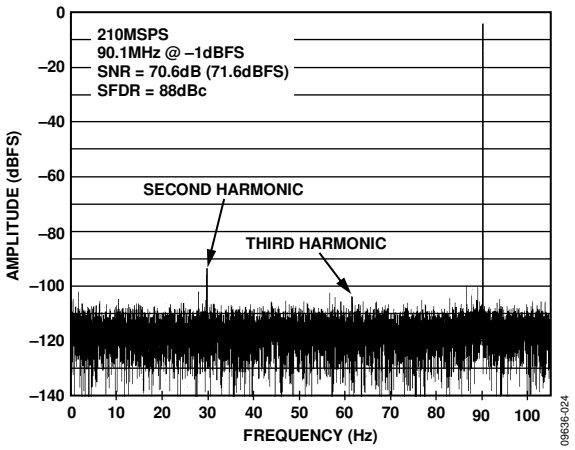

Figure 17. AD9643-210 Single-Tone FFT with f_{IN} = 90.1 MHz

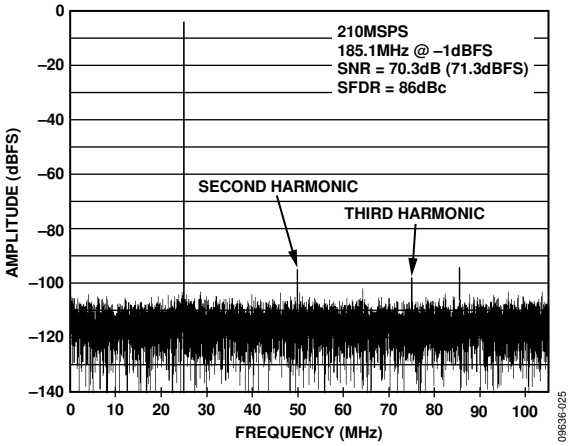

Figure 18. AD9643-210 Single-Tone FFT with f_{IN} = 185.1 MHz

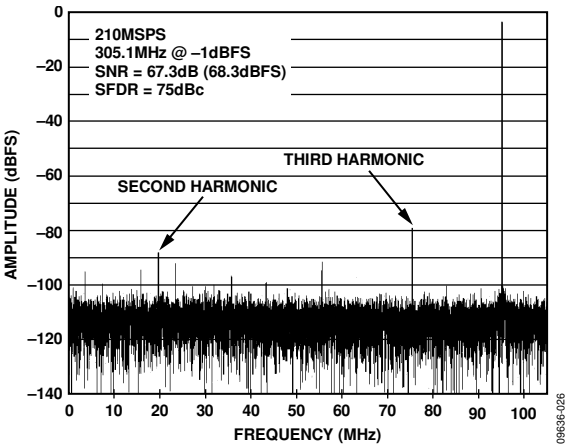

Figure 19. AD9643-210 Single-Tone FFT with f_{IN} = 305.1 MHz

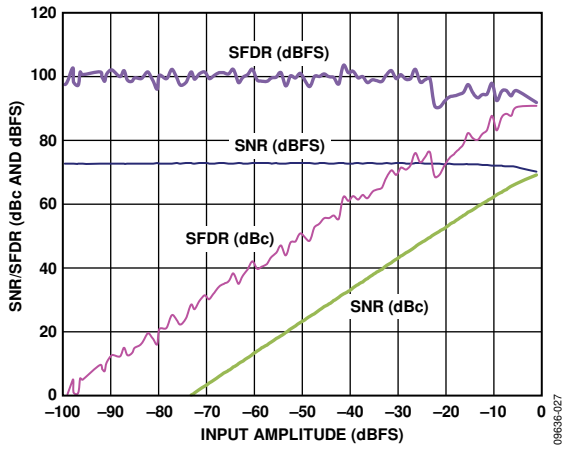

Figure 20. AD9643-210 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz

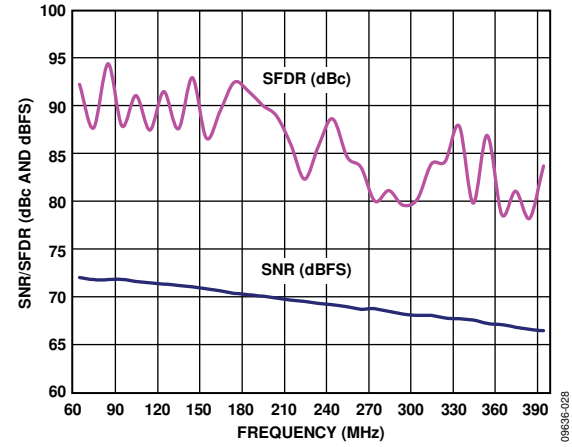

Figure 21. AD9643-210 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

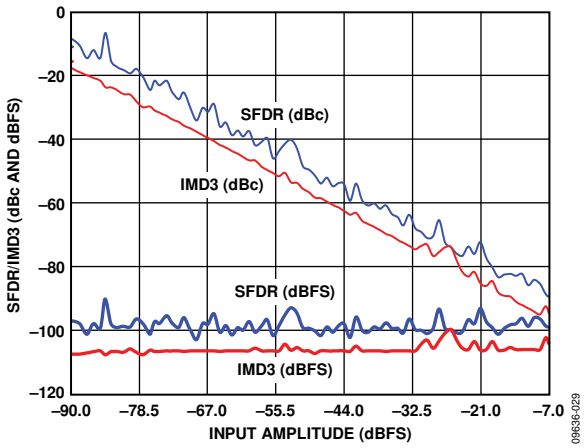

Figure 22. AD9643-210 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 210 MSPS

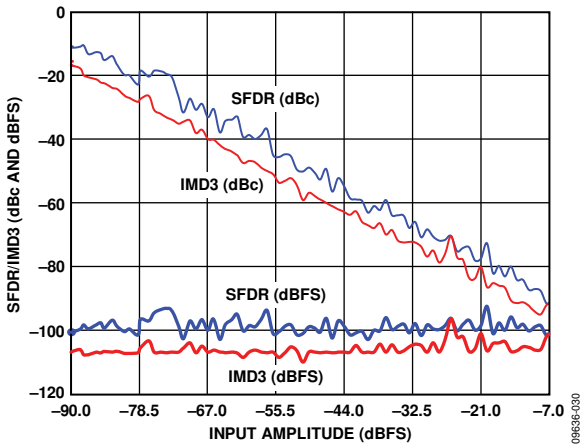

Figure 23. AD9643-210 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 210 MSPS

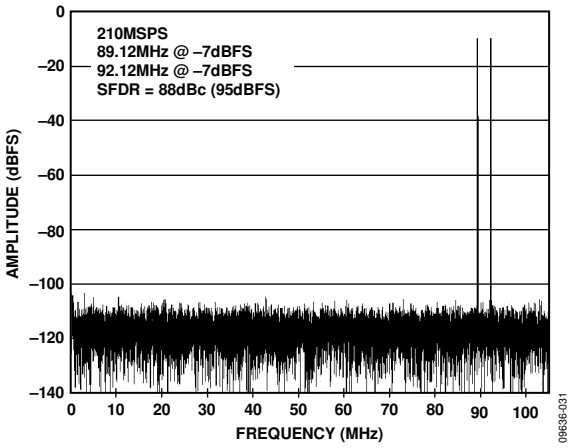

Figure 24. AD9643-210 Two-Tone FFT with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 210 MSPS

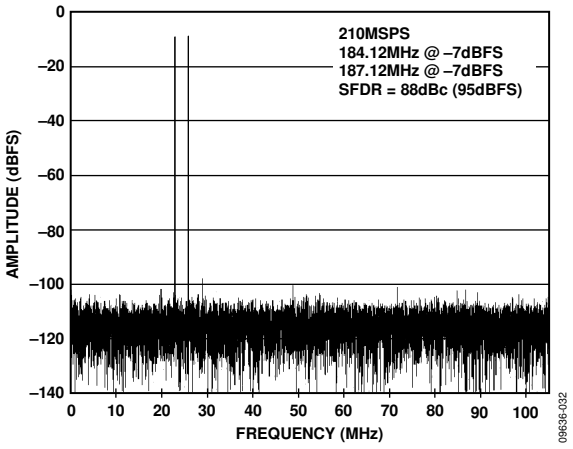

Figure 25. AD9643-210 Two-Tone FFT with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 210 MSPS

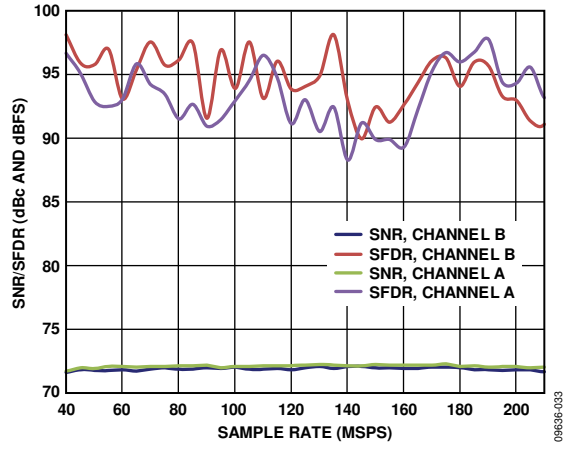

Figure 26. AD9643-210 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

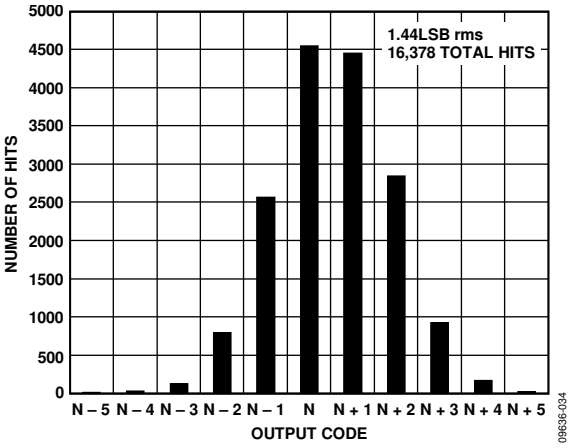

Figure 27. AD9643-210 Grounded Input Histogram

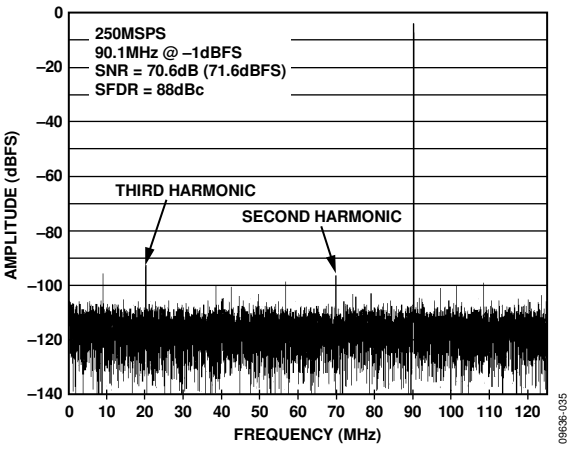

Figure 28. AD9643-250 Single-Tone FFT with f_{IN} = 90.1 MHz

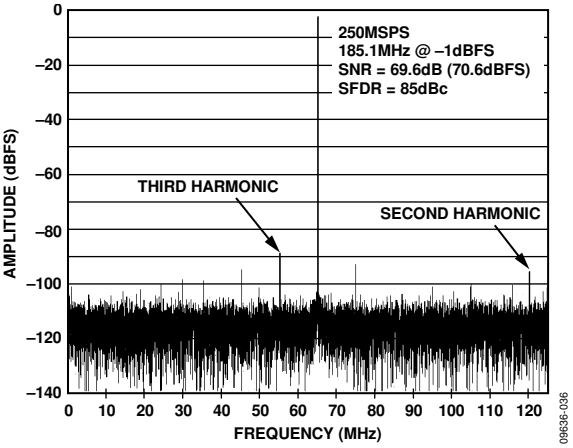

Figure 29. AD9643-250 Single-Tone FFT with f_{IN} = 185.1 MHz

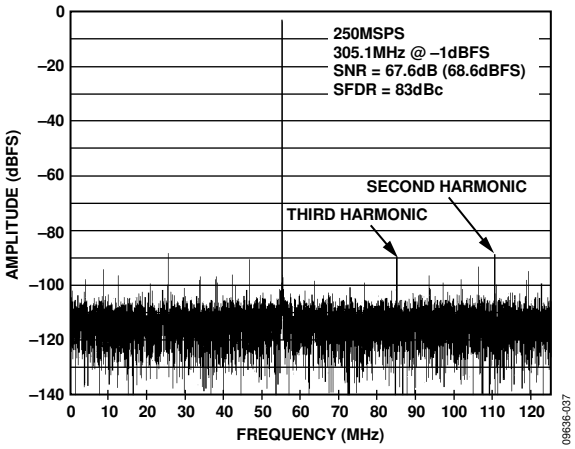

Figure 30. AD9643-250 Single-Tone FFT with f_{IN} = 305.1 MHz

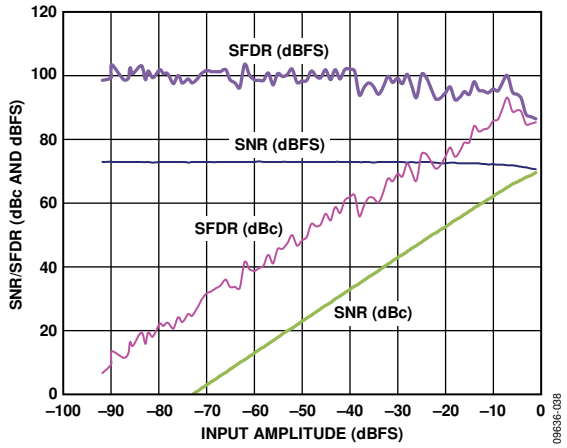

Figure 31. AD9643-250 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

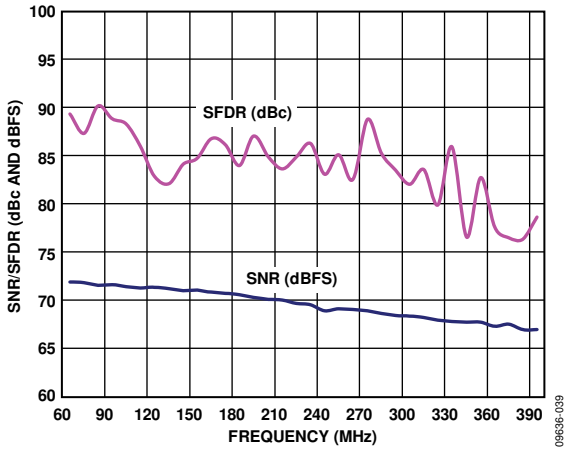

Figure 32. AD9643-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

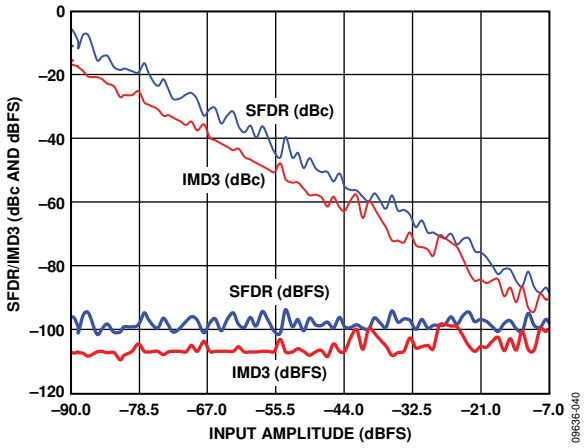

Figure 33. AD9643-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

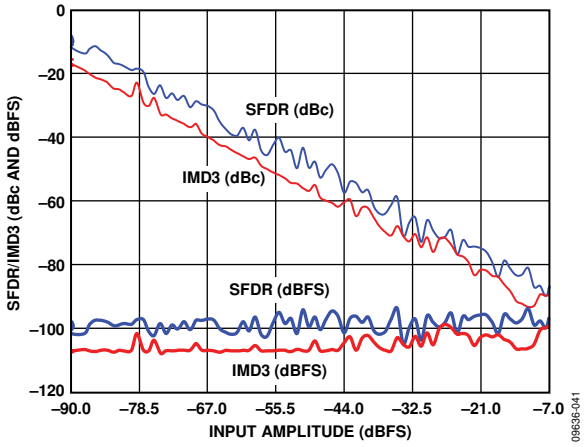

Figure 34. AD9643-250 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

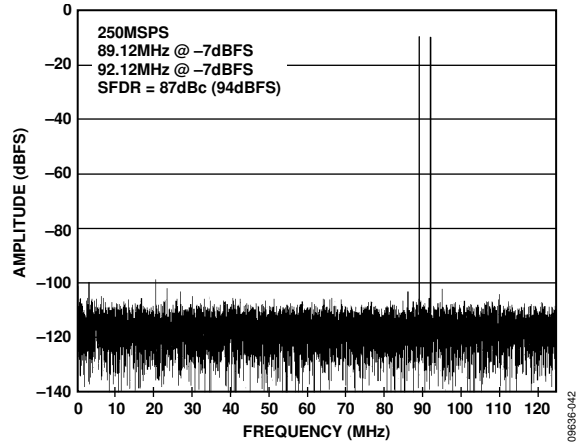

Figure 35. AD9643-250 Two-Tone FFT with f_{IN1} = 89.12, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

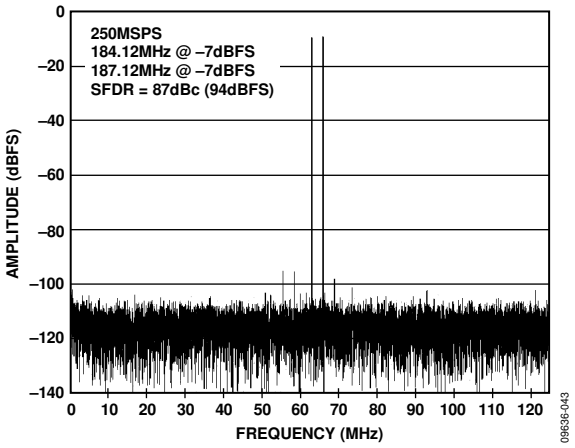

Figure 36. AD9643-250 Two-Tone FFT with f_{IN1} = 184.12, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

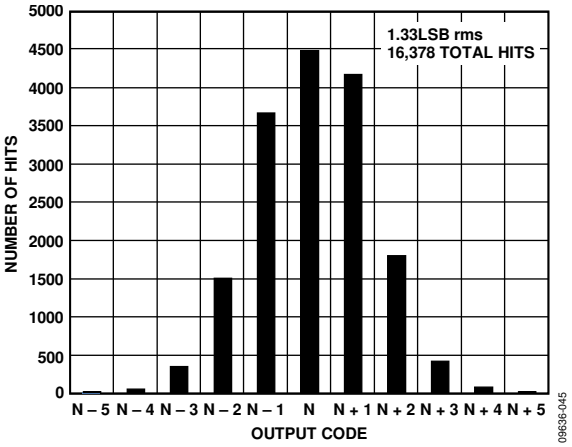

Figure 38. AD9643-250 Grounded Input Histogram

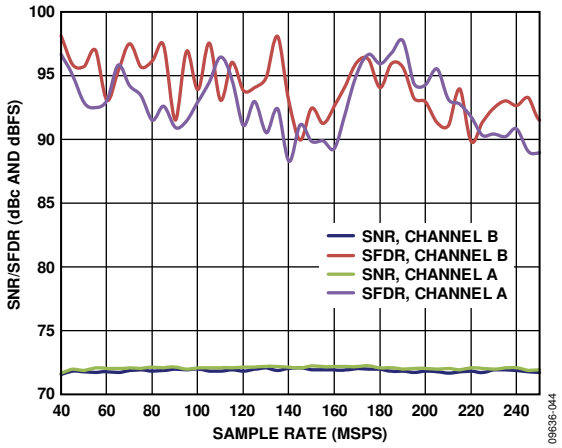

Figure 37. AD9643-250 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

EQUIVALENT CIRCUITS

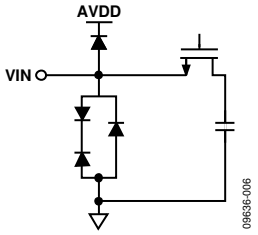

Figure 39. Equivalent Analog Input Circuit

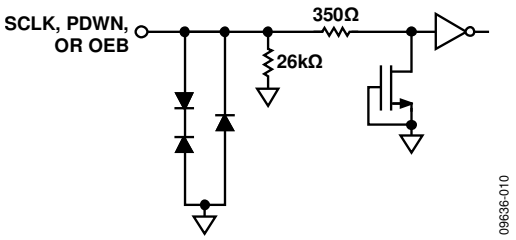

Figure 43. Equivalent SCLK, PDWN, or OEB Input Circuit

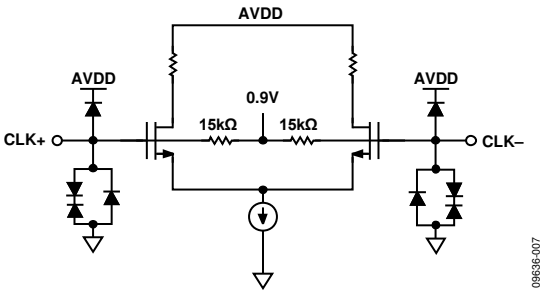

Figure 40. Equivalent Clock Input Circuit

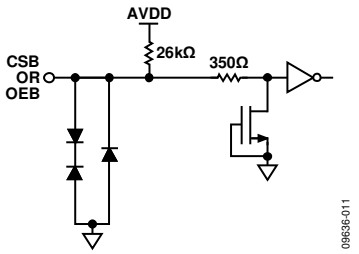

Figure 44. Equivalent CSB Input Circuit

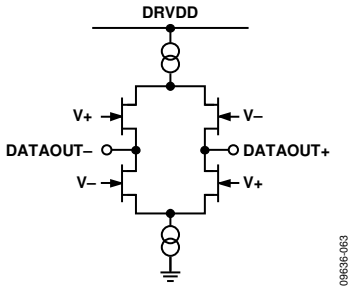

Figure 41. Equivalent LVDS Output Circuit

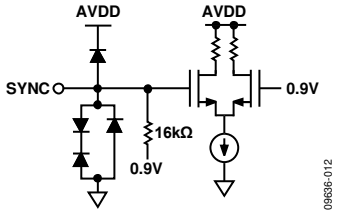

Figure 45. Equivalent SYNC Input Circuit

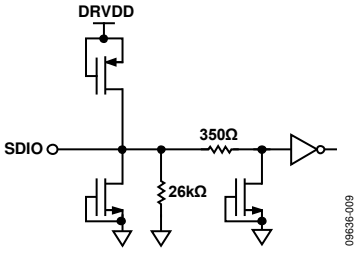

Figure 42. Equivalent SDIO Circuit

THEORY OF OPERATION

The AD9643 has two analog input channels and two digital output channels. The intermediate frequency (IF) signal passes through several stages before appearing at the output port(s).

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9643 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9643 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9643 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 46). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, the shunt capacitors should be reduced. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

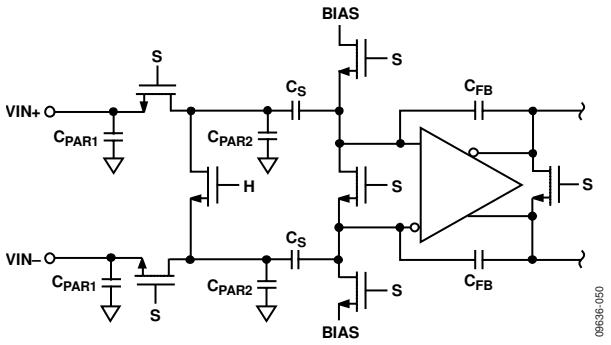

Figure 46. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, and the inputs should be differentially balanced.

Input Common Mode

The analog inputs of the AD9643 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section. This decoupling capacitor should be placed close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD9643 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2