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76V, 1A Step-Down Regulator

FEATURES

- **Wide Operating Input Voltage Range: 4V to 76V**
- **Internal 350mΩ Power MOSFET**
- **No Compensation Required**
- **Adjustable 100mA to 1A Maximum Output Current**
- Low Dropout Operation: 100% Duty Cycle
- Low Quiescent Current: 12µA
- Wide Output Range: 0.8V to V_{IN}
- 0.8V ±1% Feedback Voltage Reference
- Precise RUN Pin Threshold
- Internal and External Soft-Start
- Programmable 1.8V, 3.3V, 5V or Adjustable Output
- Few External Components Required
- Programmable Input Overvoltage Lockout
- Low Profile (0.75mm) 3mm × 5mm DFN and Thermally-Enhanced MSE16 Packages

APPLICATIONS

- Industrial Control Supplies
- Medical Devices
- Distributed Power Systems
- Portable Instruments
- Battery-Operated Devices
- Automotive
- Avionics

DESCRIPTION

The LTC®3637 is a high efficiency step-down DC/DC regulator with an internal high side power switch that draws only 12µA DC supply current while maintaining a regulated output voltage at no load.

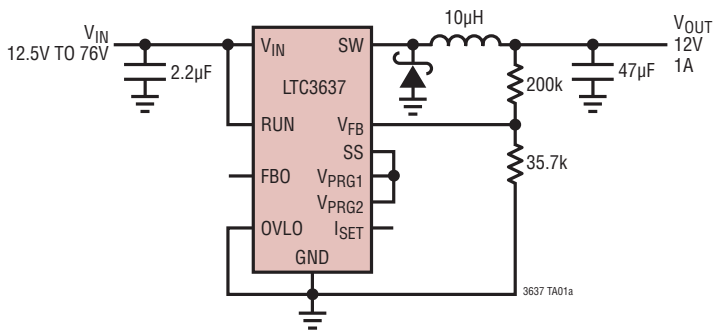
The LTC3637 can supply up to 1A load current and features a programmable peak current limit that provides a simple method for optimizing efficiency and for reducing output ripple and component size. The LTC3637's combination of Burst Mode® operation, integrated power switch, low quiescent current, and programmable peak current limit provides high efficiency over a broad range of load currents.

With its wide input range of 4V to 76V, and programmable overvoltage lockout, the LTC3637 is a robust regulator suited for regulating from a wide variety of power sources. Additionally, the LTC3637 includes a precise run threshold and soft-start feature to guarantee that the power system start-up is well-controlled in any environment.

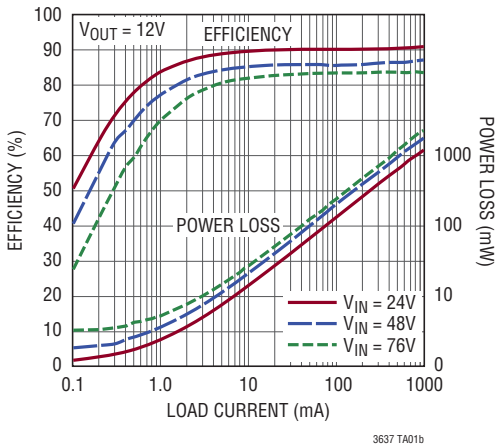
The LTC3637 is available in the thermally-enhanced 3mm × 5mm DFN and the MSE16 packages.

TYPICAL APPLICATION

12.5V to 76V Input to 12V Output, 1A Regulator



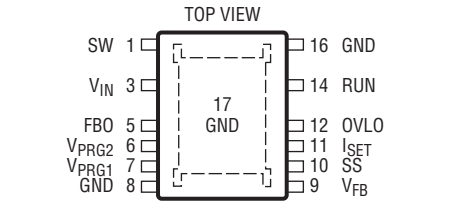
Efficiency and Power Loss vs Load Current



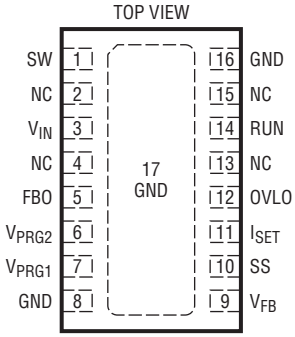
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Supply Voltage ..... –0.3V to 80V
RUN Voltage ..... –0.3V to 80V
SS, FBO, I_{SET} Voltages ..... –0.3V to 6V
V_{FB}, V_{PRG1}, V_{PRG2}, OVLO Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 4)
LTC3637E, LTC3637I ..... –40°C to 125°C
LTC3637H ..... –40°C to 150°C
LTC3637MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
VARIATION: MSE16 (12)
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
(NOTE 6)
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3637EMSE#PBF	LTC3637EMSE#TRPBF	3637	16-Lead Plastic MSOP	–40°C to 125°C
LTC3637IMSE#PBF	LTC3637IMSE#TRPBF	3637	16-Lead Plastic MSOP	–40°C to 125°C
LTC3637HMSE#PBF	LTC3637HMSE#TRPBF	3637	16-Lead Plastic MSOP	–40°C to 150°C
LTC3637MPMSE#PBF	LTC3637MPMSE#TRPBF	3637	16-Lead Plastic MSOP	–55°C to 150°C
LTC3637EDHC#PBF	LTC3637EDHC#TRPBF	3637	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3637IDHC#PBF	LTC3637IDHC#TRPBF	3637	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3637HDHC#PBF	LTC3637HDHC#TRPBF	3637	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3637MPDHC#PBF	LTC3637MPDHC#TRPBF	3637	16-Lead (5mm × 3mm) Plastic DFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (V_{IN})							
V_{IN}	Input Voltage Operating Range			4		76	V
V_{OUT}	Output Voltage Operating Range			0.8		V_{IN}	V
UVLO	V_{IN} Undervoltage Lockout	V_{IN} Rising V_{IN} Falling Hysteresis	● ●	3.45 3.30	3.65 3.5 150	3.85 3.70	V V mV
I_Q	DC Supply Current (Note 5) Active Mode Sleep Mode Shutdown Mode	 No Load RUN = 0V			 165 12 3	 350 20 10	 µA µA µA
	RUN and OVLO Pin Threshold Voltage	Rising Falling Hysteresis		1.17 1.06	1.21 1.10 110	1.25 1.14	V V mV
	RUN Pin Leakage Current	RUN = 1.3V		–10	0	10	nA
Output Supply (V_{FB})							
	Feedback Comparator Threshold Voltage (Adjustable Output)	V_{FB} Rising, V_{PRG1} = V_{PRG2} = 0V LTC3637E, LTC3637I LTC3637H, LTC3637MP	 ● ●	 0.792 0.788	 0.800 0.800	 0.808 0.812	 V V
	Feedback Comparator Hysteresis (Adjustable Output)	V_{FB} Falling, V_{PRG1} = V_{PRG2} = 0V	●	2.5	5	7	mV
	Feedback Pin Current	V_{FB} = 1V, V_{PRG1} = 0V, V_{PRG2} = 0V		–10	0	10	nA
	Feedback Comparator Threshold Voltages (Fixed Output)	V_{FB} Rising, V_{PRG1} = SS, V_{PRG2} = 0V V_{FB} Falling, V_{PRG1} = SS, V_{PRG2} = 0V	● ●	4.940 4.910	5.015 4.985	5.090 5.060	V V
		V_{FB} Rising, V_{PRG1} = 0V, V_{PRG2} = SS V_{FB} Falling, V_{PRG1} = 0V, V_{PRG2} = SS	● ●	3.250 3.230	3.310 3.290	3.370 3.350	V V
		V_{FB} Rising, V_{PRG1} = V_{PRG2} = SS V_{FB} Falling, V_{PRG1} = V_{PRG2} = SS	● ●	1.775 1.765	1.805 1.795	1.835 1.825	V V
	Feedback Voltage Line Regulation	V_{IN} = 4V to 76V			0.001		%/V
Operation							
	Peak Current Comparator Threshold	I_{SET} Floating 100k Resistor from I_{SET} to GND I_{SET} Shorted to GND	● ● ●	2 0.9 0.17	2.4 1.2 0.24	2.8 1.5 0.31	A A A
	Power Switch On-Resistance	I_{SW} = –200mA			0.35		Ω
	Switch Pin Leakage Current	V_{IN} = 65V, SW = 0V			0.1	1	µA
	Soft-Start Pin Pull-Up Current	SS Pin < 2.5V		3	5	6	µA
	Internal Soft-Start Time	SS Pin Floating			0.8		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3637 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3637E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3637I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3637H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3637MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range.

High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is 43°C/W for the DFN or 45°C/W for the MSOP.

ELECTRICAL CHARACTERISTICS

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

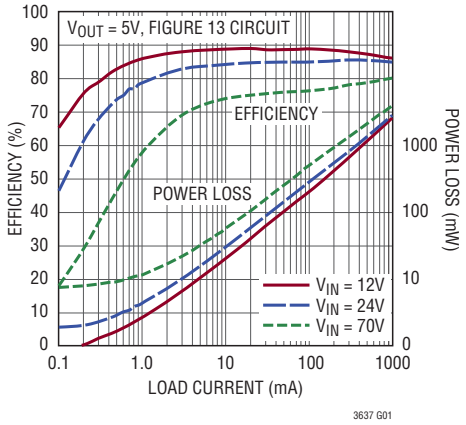
Note 4: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device. The overtemperature protection level is not production tested.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

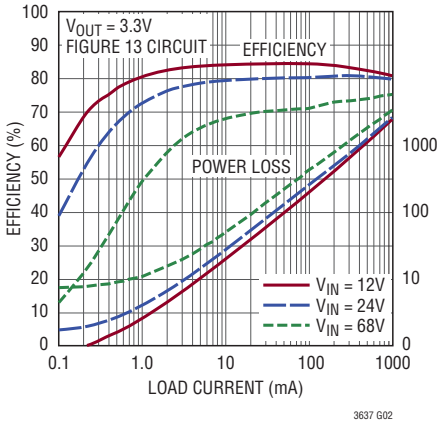
Note 6: For application concerned with pin creepage and clearance distances at high voltages, the MSOP package should be used. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS

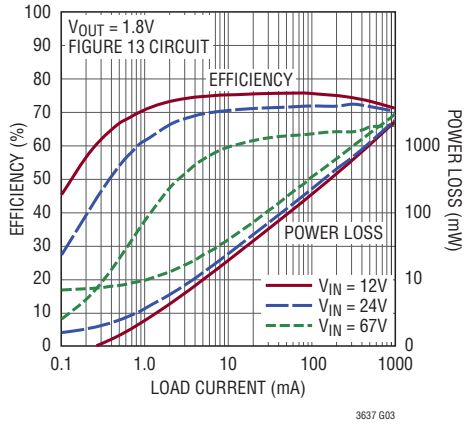
Efficiency and Power Loss vs Load Current, V_{OUT} = 5V



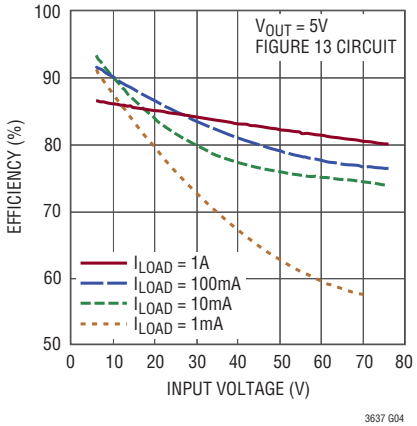
Efficiency and Power Loss vs Load Current, V_{OUT} = 3.3V



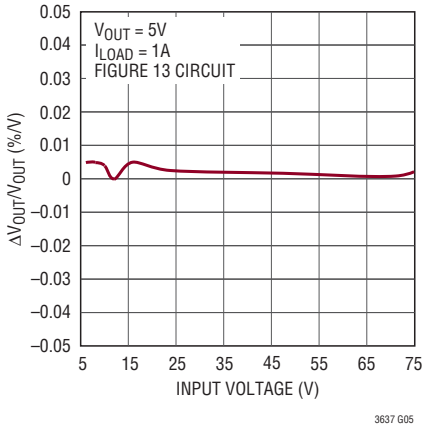
Efficiency and Power Loss vs Load Current, V_{OUT} = 1.8V



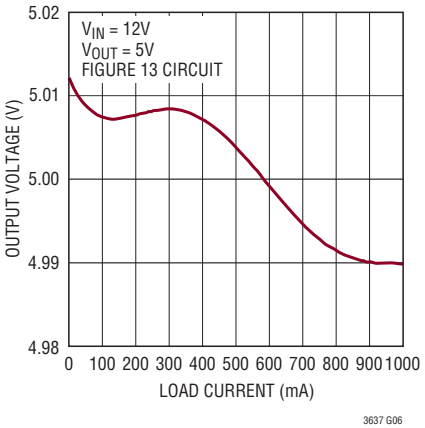
Efficiency vs Input Voltage



Line Regulation vs Input Voltage

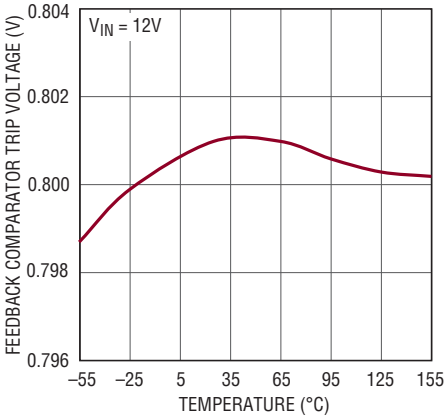


Load Regulation vs Load Current



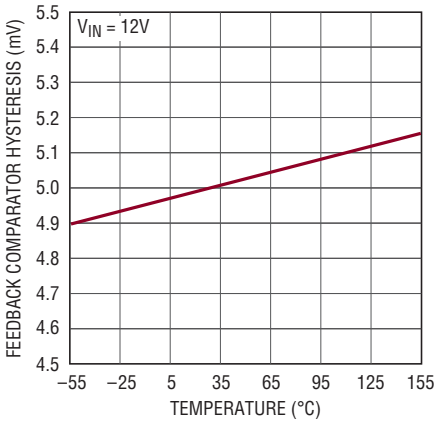
TYPICAL PERFORMANCE CHARACTERISTICS

Feedback Comparator Trip Voltage vs Temperature



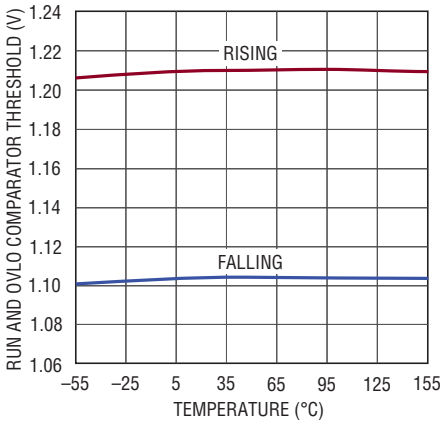
3637 G07

Feedback Comparator Hysteresis vs Temperature



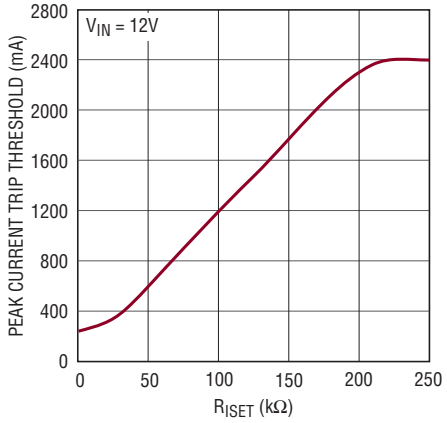
3637 G08

RUN and OVLO Comparator Threshold Voltages vs Temperature



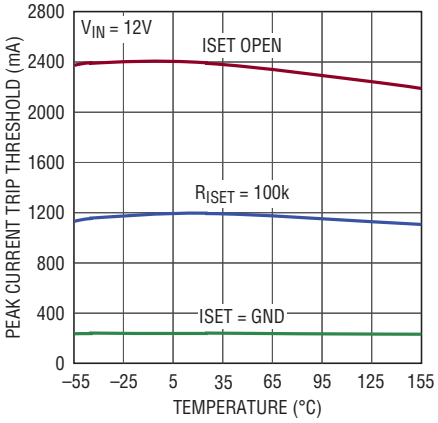
3637 G09

Peak Current Trip Threshold vs R_{ISET}



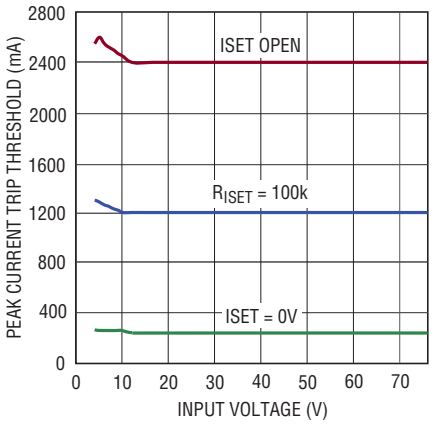
3637 G10

Peak Current Trip Threshold vs Temperature



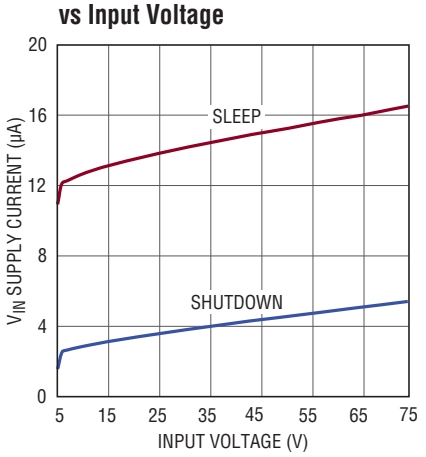
3637 G11

Peak Current Trip Threshold vs Input Voltage



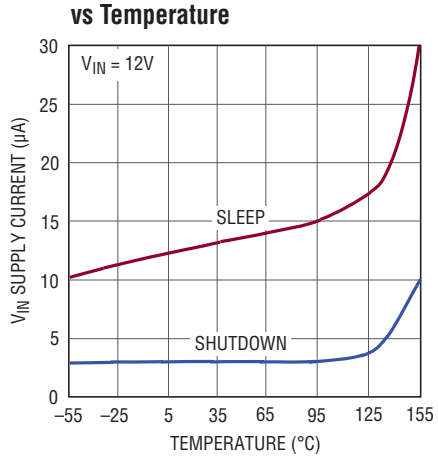
3637 G12

Quiescent V_{IN} Supply Current vs Input Voltage



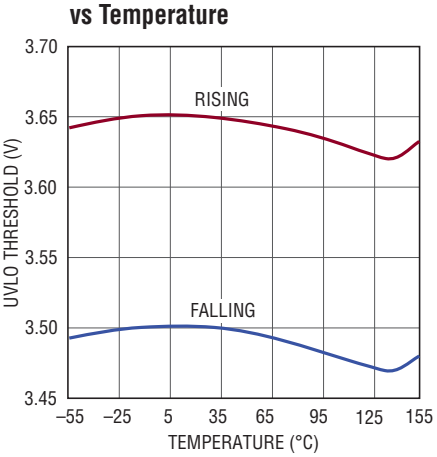
3637 G13

Quiescent V_{IN} Supply Current vs Temperature



3637 G14

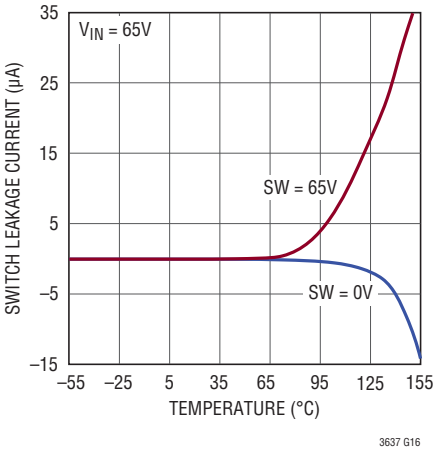
UVLO Threshold Voltages vs Temperature



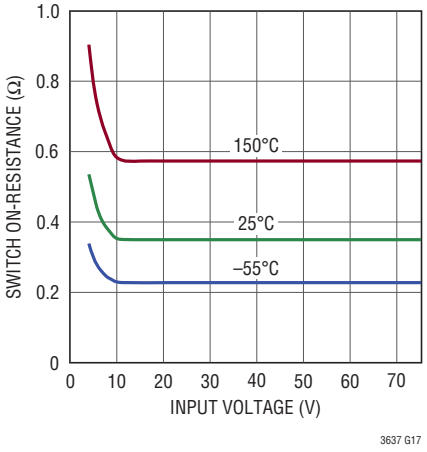
3637 G15

TYPICAL PERFORMANCE CHARACTERISTICS

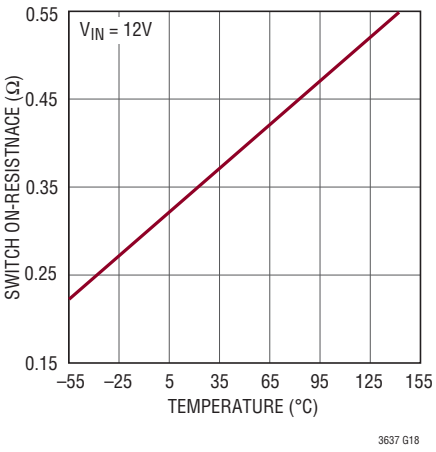
Switch Leakage Current vs Temperature



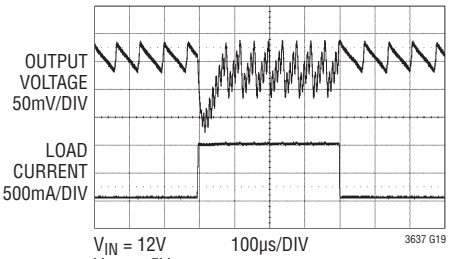
Switch On-Resistance vs Input Voltage



Switch On-Resistance vs Temperature

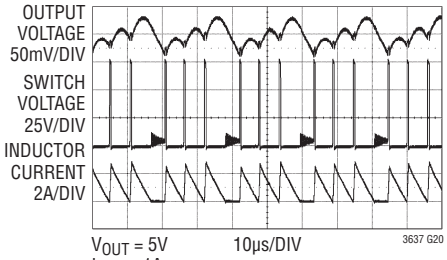


Load Step Transient Response



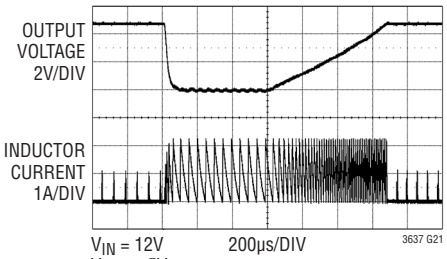
V_{IN} = 12V 100µs/DIV
V_{OUT} = 5V
5mA TO 1A LOAD STEP
FIGURE 13 CIRCUIT

Operating Waveforms, V_{IN} = 76V



V_{OUT} = 5V 10µs/DIV
I_{OUT} = 1A
FIGURE 13 CIRCUIT

Short Circuit and Recovery



V_{IN} = 12V 200µs/DIV
V_{OUT} = 5V
I_{OUT} = 50mA (NON SHORT CIRCUIT)
FIGURE 13 CIRCUIT

PIN FUNCTIONS

SW (Pin 1): Switch Node Connection to Inductor. This pin connects to the drains of the internal power MOSFET switches.

NC (Pins 2, 4, 13, 15 DHC Package Only): No Internal Connection. Leave these pins open.

V_{IN} (Pin 3): Main Input Supply Pin. A ceramic bypass capacitor should be tied between this pin and GND.

FBO (Pin 5): Feedback Comparator Output. The typical pull-up current is 20µA. The typical pull- down impedance is 70Ω.

V_{PRG2}, V_{PRG1} (Pins 6, 7): Output Voltage Selection. Short both pins to ground for an external resistive divider programmable output voltage. Short V_{PRG1} to SS and short V_{PRG2} to ground for a 5V output voltage. Short V_{PRG1} to ground and short V_{PRG2} to SS for a 3.3V output voltage. Short both pins to SS for a 1.8V output voltage.

GND (Pins 8, 16, Exposed Pad Pin 17): Ground. The exposed backside pad must be soldered to the PCB ground plane for optimal thermal performance.

V_{FB} (Pin 9): Output Voltage Feedback. When configured for an adjustable output voltage, connect to an external resistive divider to divide the output voltage down for comparison to the 0.8V reference. For the fixed output configuration, directly connect this pin to the output supply.

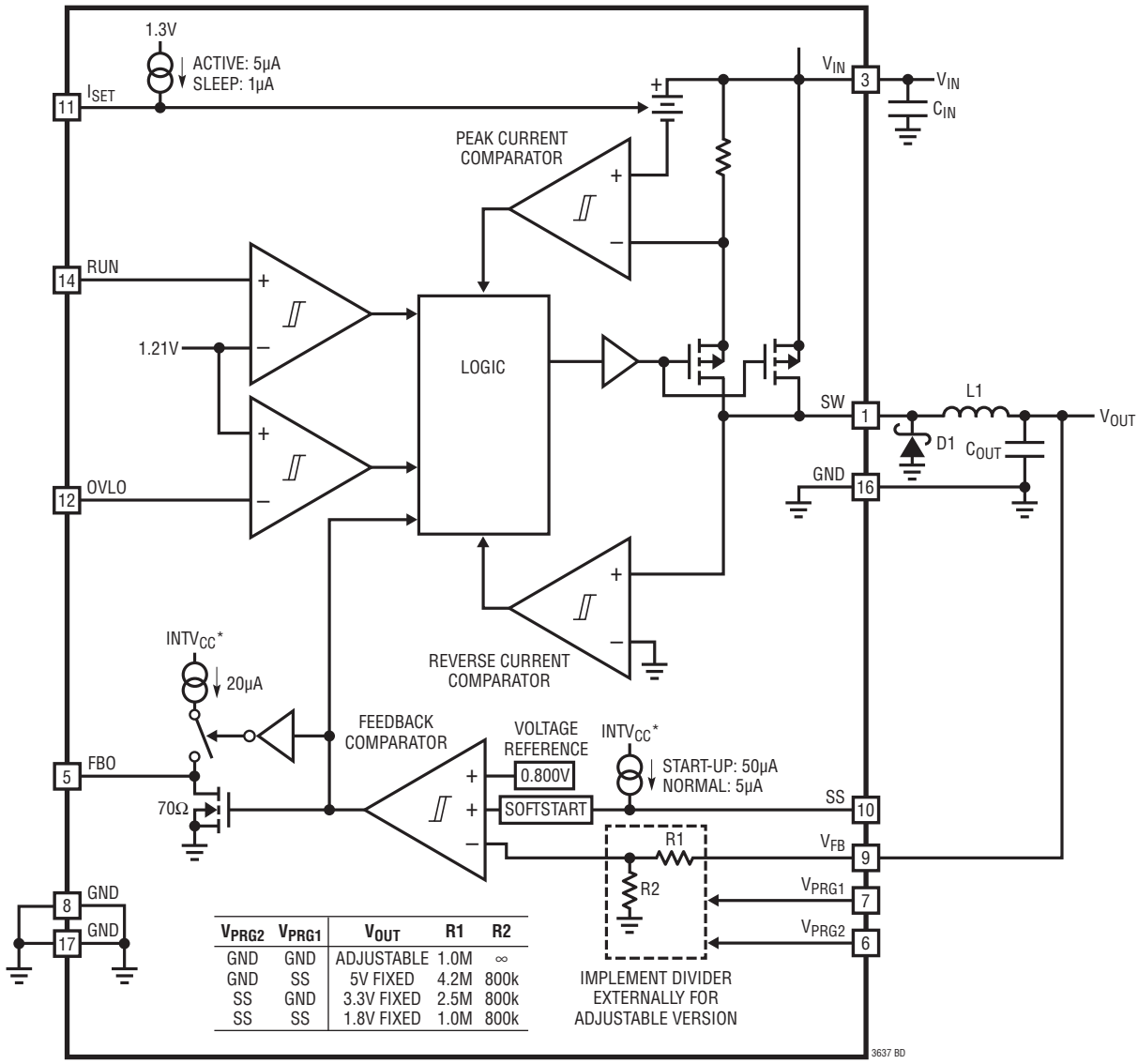
SS (Pin 10): Soft-Start Control Input. A capacitor to ground at this pin sets the output voltage ramp time. A 50µA current initially charges the soft-start capacitor until switching begins, at which time the current is reduced to its nominal value of 5µA. The output voltage ramp time from zero to its regulated value is 1ms for every 16.5nF of capacitance from SS to GND. If left floating, the ramp time defaults to an internal 0.8ms soft-start.

I_{SET} (Pin 11): Peak Current Set Input and Voltage Output Ripple Filter. A resistor from this pin to ground sets the peak current comparator threshold. Leave floating for the maximum peak current (2.4A typical) or short to ground for minimum peak current (0.24A typical). The maximum output current is one-half the peak current. The 5µA current that is sourced out of this pin when switching, is reduced to 1µA in sleep. Optionally, a capacitor can be placed from this pin to GND to trade off efficiency for light load output voltage ripple. See Applications Information.

OVLO (Pin 12): Overvoltage Lockout Input. Connect to the input supply through a resistor divider to set the overvoltage lockout level. A voltage on this pin above 1.21V disables the internal MOSFET switch. Normal operation resumes when the voltage on this pin decreases below 1.10V. A transient exceeding the OVLO threshold triggers a soft-start reset, resulting in a graceful recovery from an input supply transient. Connect this pin to ground to disable the overvoltage lockout.

RUN (Pin 14): Run Control Input. A voltage on this pin above 1.21V enables normal operation. Forcing this pin below 0.7V shuts down the LTC3637, reducing quiescent current to approximately 3µA. Optionally, connect to the input supply through a resistor divider to set the undervoltage lockout.

BLOCK DIAGRAM



V_{PRG2}	V_{PRG1}	V_{OUT}	R1	R2
GND	GND	ADJUSTABLE	1.0M	∞
GND	SS	5V FIXED	4.2M	800k
SS	GND	3.3V FIXED	2.5M	800k
SS	SS	1.8V FIXED	1.0M	800k

*WHEN V_{IN} > 5V, $INTV_{CC}$ = 5V
WHEN V_{IN} ≤ 5V, $INTV_{CC}$ FOLLOWS V_{IN}

OPERATION (Refer to Block Diagram)

The LTC3637 is a step-down DC/DC regulator with an internal high side power switch that uses Burst Mode control. The low quiescent current and high switching frequency results in high efficiency across a wide range of load currents. Burst Mode operation functions by using short "burst" cycles to switch the inductor current through the internal power MOSFET, followed by a sleep cycle where the power switch is off and the load current is supplied by the output capacitor. During the sleep cycle, the LTC3637 draws only 12µA of supply current. At light loads, the burst cycles are a small percentage of the total cycle time which minimizes the average supply current, greatly improving efficiency. Figure 1 shows an example of Burst Mode operation. The switching frequency and the number of switching cycles during Burst Mode operation are dependent on the inductor value, peak current, load current, input voltage and output voltage.

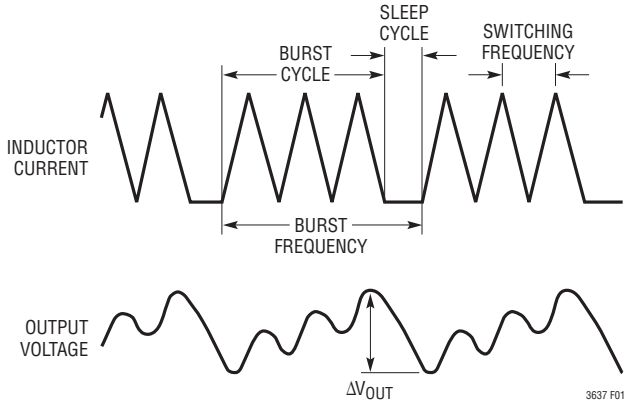


Figure 1. Burst Mode Operation

Main Control Loop

The LTC3637 uses the V_{PRG1} and V_{PRG2} control pins to connect internal feedback resistors to the V_{FB} pin. This enables fixed outputs of 1.8V, 3.3V or 5V without increasing component count, input supply current or exposure to noise on the sensitive input to the feedback comparator. External feedback resistors (adjustable mode) can still be used by connecting both V_{PRG1} and V_{PRG2} to ground.

In adjustable mode the feedback comparator monitors the voltage on the V_{FB} pin and compares it to an internal 800mV reference. If this voltage is greater than the reference, the comparator activates a sleep mode in which the power switch and current comparators are disabled, reducing the V_{IN} pin supply current to only 12µA. As the load current discharges the output capacitor, the voltage on the V_{FB} pin decreases. When this voltage falls 5mV below the 800mV reference, the feedback comparator trips and enables burst cycles.

At the beginning of the burst cycle, the internal high side power switch (P-channel MOSFET) is turned on and the inductor current begins to ramp up. The inductor current increases until either the current exceeds the peak current comparator threshold or the voltage on the V_{FB} pin exceeds 800mV, at which time the high side power switch is turned off and the external catch diode turns on. The inductor current ramps down until the reverse current comparator trips, signaling that the current is close to zero. If the voltage on the V_{FB} pin is still less than the 800mV reference, the high side power switch is turned on again and another cycle commences. The average current during a burst cycle will normally be greater than the average load current. For this architecture, the maximum average output current is equal to half of the peak current.

The hysteretic nature of this control architecture results in a switching frequency that is a function of the input voltage, output voltage, and inductor value. This behavior provides inherent short-circuit protection. If the output is shorted to ground, the inductor current will decay very slowly during a single switching cycle. Since the high side switch turns on only when the inductor current is near zero, the LTC3637 inherently switches at a lower frequency during start-up or short-circuit conditions.

Start-Up and Shutdown

If the voltage on the RUN pin is less than 0.7V, the LTC3637 enters a shutdown mode in which all internal circuitry is disabled, reducing the DC supply current to 3µA. When the voltage on the RUN pin exceeds 1.21V, normal operation of the main control loop is enabled. The RUN pin comparator has 110mV of internal hysteresis, and therefore must fall below 1.1V to stop switching and disable the main control loop.

An internal 0.8ms soft-start function limits the ramp rate of the output voltage on start-up to prevent excessive input supply droop. If a longer ramp time and consequently less supply droop is desired, a capacitor can be placed from

OPERATION (Refer to Block Diagram)

the SS pin to ground. The 5µA current that is sourced out of this pin will create a smooth voltage ramp on the capacitor. If this ramp rate is slower than the internal 0.8ms soft-start, then the output voltage will be limited by the ramp rate on the SS pin instead. The internal and external soft-start functions are reset on start-up and after an undervoltage or overvoltage event on the input supply.

The peak inductor current is not limited by the internal or external soft-start functions; however, placing a capacitor from the I_{SET} pin to ground does provide this capability.

Peak Inductor Current Programming

The peak current comparator nominally limits the peak inductor current to 2.4A. This peak inductor current can be adjusted by placing a resistor from the I_{SET} pin to ground. The 5µA current sourced out of this pin through the resistor generates a voltage that adjusts the peak current comparator threshold.

During sleep mode, the current sourced out of the I_{SET} pin is reduced to 1µA. The I_{SET} current is increased back to 5µA on the first switching cycle after exiting sleep mode. The I_{SET} current reduction in sleep mode, along with adding a filtering capacitor, C_{ISET}, from the I_{SET} pin to ground, provides a method of reducing light load output voltage ripple at the expense of lower efficiency and slightly degraded load step transient response.

Dropout Operation

When the input supply decreases toward the output supply, the duty cycle increases to maintain regulation. The P-channel MOSFET top switch in the LTC3637 allows the duty cycle to increase all the way to 100%. At 100% duty cycle, the P-channel MOSFET stays on continuously, providing output current equal to the peak current, which can be greater than 2A. The power dissipation of the LTC3637 can increase dramatically during dropout operation especially at input voltages less than 10V. The increased power dissipation is due to higher potential output current and increased P-channel MOSFET on-resistance. See the Thermal Considerations section of the Applications Information for a detailed example.

Input Voltage and Overtemperature Protection

When using the LTC3637, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, however, the LTC3637 incorporates an overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC3637 will enter thermal shutdown mode. Both power switches will be turned off and the SW node will become high impedance. After the part has cooled below 160°C, it will restart. The overtemperature level is not production tested.

The LTC3637 additionally implements protection features which inhibit switching when the input voltage is not within a programmed operating range. By using a resistive divider from the input supply to ground, the RUN and OVLO pins can serve as a precise input supply voltage monitor. Switching is disabled when either the RUN pin falls below 1.1V or the OVLO pin rises above 1.21V, which can be configured to limit switching to a specific range of input supply voltage. Pulling the RUN pin below 700mV forces a low quiescent current shutdown (3µA). Furthermore, if the input voltage falls below 3.5V typical (3.7V maximum), an internal undervoltage detector disables switching.

When switching is disabled, the LTC3637 can safely sustain input voltages up to the absolute maximum rating of 80V. Input supply undervoltage or overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

High Input Voltage Considerations

When operating with an input voltage to output voltage differential of more than 65V, a minimum output load current of 10mA is required to maintain a well-regulated output voltage under all operating conditions, including shutdown mode. If this 10mA minimum load is not available, then the minimum output voltage that can be maintained by the LTC3637 is limited to V_{IN} – 65V.

APPLICATIONS INFORMATION

The basic LTC3637 application circuit is shown on the front page of the data sheet. External component selection is determined by the maximum load current requirement and begins with the selection of the peak current programming resistor, R_{ISET}. The inductor value L can then be determined, followed by capacitors C_{IN} and C_{OUT}.

Peak Current Resistor Selection

The peak current comparator has a guaranteed peak current limit of 2A (2.4A typical), which guarantees a maximum average load current of 1A. For applications that demand less current, the peak current threshold can be reduced to as little as 200mA (240mA typical). This lower peak current allows the use of lower value, smaller components (input capacitor, output capacitor, and inductor), resulting in lower supply ripple and a smaller overall DC/DC regulator.

The threshold can be easily programmed using a resistor (R_{ISET}) between the I_{SET} pin and ground. The voltage generated on the I_{SET} pin by R_{ISET} and the internal 5µA current source sets the peak current. The voltage on the I_{SET} pin is internally limited within the range of 0.1V to 1.0V. The value of resistor for a particular peak current can be selected by using Figure 2 or the following equation:

$$R_{ISET} = 140k \bullet I_{PEAK} - 24k$$

where $200mA < I_{PEAK} < 2A$.

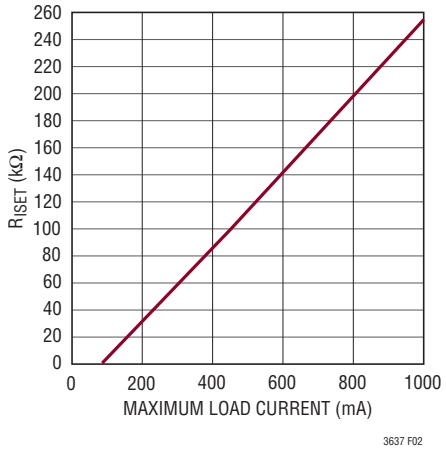


Figure 2. R_{ISET} Selection

The internal 5µA current source is reduced to 1µA in sleep mode to maximize efficiency and to facilitate a trade-off between efficiency and light load output voltage ripple, as described in the Optimizing Output Voltage Ripple section of the Applications Information. For maximum efficiency, minimize the capacitance on the I_{SET} pin and place the R_{ISET} resistor as close to the pin as possible.

The typical peak current is internally limited to be within the range of 240mA to 2.4A. Shorting the I_{SET} pin to ground programs the current limit to 240mA, and leaving it float sets the current limit to the maximum value of 2.4A. When selecting this resistor value, be aware that the maximum average output current for this architecture is limited to half of the peak current. Therefore, be sure to select a value that sets the peak current with enough margin to provide adequate load current under all conditions. Selecting the peak current to be 2.2 times greater than the maximum load current is a good starting point for most applications.

Inductor Selection

The inductor, input voltage, output voltage, and peak current determine the switching frequency during a burst cycle of the LTC3637. For a given input voltage, output voltage, and peak current, the inductor value sets the switching frequency during a burst cycle when the output is in regulation. Generally, switching between 50kHz and 250kHz yields high efficiency, and 200kHz is a good first choice for many applications. The inductor value can be determined by the following equation:

$$L = \left(\frac{V_{OUT}}{f \bullet I_{PEAK}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The variation in switching frequency during a burst cycle with input voltage and inductance is shown in Figure 3. For lower values of I_{PEAK}, multiply the frequency in Figure 3 by $2.4A/I_{PEAK}$.

An additional constraint on the inductor value is the LTC3637's 150ns minimum on-time of the high side switch. Therefore, in order to keep the current in the inductor well-controlled, the inductor value must be chosen so that

APPLICATIONS INFORMATION

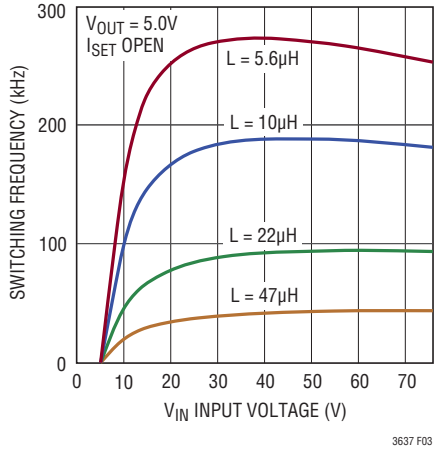


Figure 3. Switching Frequency for V_{OUT} = 5.0V

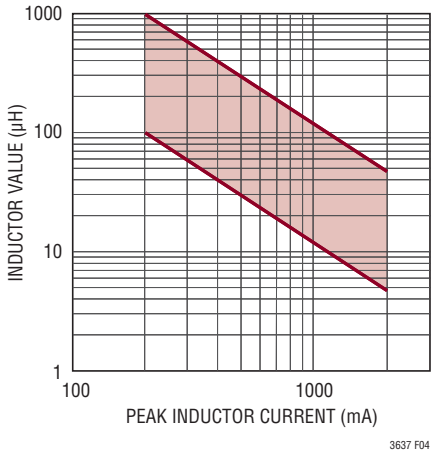


Figure 4. Recommended Inductor Values for Maximum Efficiency

it is larger than a minimum value which can be computed as follows:

$$L > \frac{V_{IN(MAX)} \bullet t_{ON(MIN)}}{I_{PEAK}} \bullet 1.2$$

where $V_{IN(MAX)}$ is the maximum input supply voltage when switching is enabled, $t_{ON(MIN)}$ is 150ns, I_{PEAK} is the peak current, and the factor of 1.2 accounts for typical inductor tolerance and variation over temperature. For applications that have large input supply transients, the OVLO pin can be used to disable switching above the maximum operating voltage, $V_{IN(MAX)}$, so that the minimum inductor value is not artificially limited by a transient condition. Inductor values that violate the above equation will cause the peak current to overshoot and permanent damage to the part may occur.

Although the above equation provides the minimum inductor value, higher efficiency is generally achieved with a larger inductor value, which produces a lower switching frequency. For a given inductor type, however, as inductance is increased, DC resistance (DCR) also increases. Higher DCR translates into higher copper losses and lower current rating, both of which place an upper limit on the inductance. The recommended range of inductor values for small surface mount inductors as a function of peak current is shown in Figure 4. The values in this range are a good compromise between the trade-offs discussed above. For applications where board area is not a limiting factor, inductors with larger cores can be used, which extends the recommended range of Figure 4 to larger values.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is independent of core size for a fixed inductor value but is very dependent of the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly

APPLICATIONS INFORMATION

depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Würth, Coilcraft, TDK, Toko, and Sumida.

C_{IN} and C_{OUT} Selection

The input capacitor, C_{IN}, is needed to filter the trapezoidal current at the source of the top high side MOSFET. C_{IN} should be sized to provide the energy required to charge the inductor without causing a large decrease in input voltage (ΔV_{IN}). The relationship between C_{IN} and ΔV_{IN} is given by:

$$C_{IN} > \frac{L \bullet I_{PEAK}^2}{2 \bullet V_{IN} \bullet \Delta V_{IN}}$$

It is recommended to use a larger value for C_{IN} than calculated by the above equation since capacitance decreases with applied voltage. In general, a 4.7µF X7R ceramic capacitor is a good choice for C_{IN} in most LTC3637 applications.

To minimize large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based only on 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to satisfy the load current when the LTC3637 is in sleep. The output ripple has a lower limit of $V_{OUT}/160$ due to the 5mV typical hysteresis of the feedback comparator. The time delay of the comparator adds an additional ripple voltage that is a function of the load current. During this delay time, the LTC3637 continues to switch and supply current to the output. The output ripple can be approximated by:

$$\Delta V_{OUT} \approx \left(\frac{I_{PEAK}}{2} - I_{LOAD} \right) \bullet \frac{4 \bullet 10^{-6}}{C_{OUT}} + \frac{V_{OUT}}{160}$$

The output ripple is a maximum at no load and approaches lower limit of $V_{OUT}/160$ at full load. Choose the output capacitor C_{OUT} to limit the output voltage ripple ΔV_{OUT} using the following equation:

$$C_{OUT} \geq \frac{I_{PEAK} \bullet 2 \bullet 10^{-6}}{\Delta V_{OUT} - \frac{V_{OUT}}{160}}$$

The value of the output capacitor must be large enough to accept the energy stored in the inductor without a large change in output voltage during a single switching cycle.

Setting this voltage step equal to 1% of the output voltage, the output capacitor must be:

$$C_{OUT} > 50 \bullet L \bullet \left(\frac{I_{PEAK}}{V_{OUT}} \right)^2$$

Typically, a capacitor that satisfies the voltage ripple requirement is adequate to filter the inductor ripple. To avoid overheating, the output capacitor must also be sized to handle the ripple current generated by the inductor. The worst-case ripple current in the output capacitor is given by $I_{RMS} = I_{PEAK}/2$. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important only to use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have high voltage coefficient and audible piezoelectric effects. The high quality factor (Q)

APPLICATIONS INFORMATION

of ceramic capacitors in series with trace inductance can also lead to significant input voltage ringing.

Input Voltage Steps

If the input voltage falls below the regulated output voltage, the body diode of the internal high side MOSFET will conduct current from the output supply to the input supply. If the input voltage falls rapidly, the voltage across the inductor will be significant and may saturate the inductor. A large current will then flow through the high side MOSFET body diode, resulting in excessive power dissipation that may damage the part.

If rapid voltage steps are expected on the input supply, put a small silicon or Schottky diode in series with the V_{IN} pin to prevent reverse current and inductor saturation, shown below as D2 in Figure 5. The diode should be sized for a reverse voltage of greater than the input voltage, and to withstand repetitive currents higher than the maximum peak current of the LTC3637.

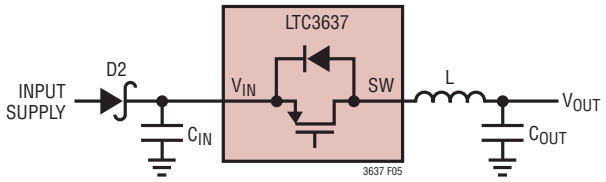


Figure 5. Preventing Current Flow to the Input

Ceramic Capacitors and Audible Noise

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

For application with inductive source impedance, such as a long wire, an electrolytic capacitor or a ceramic capacitor with a series resistor may be required in parallel with C_{IN} to dampen the ringing of the input supply. Figure 6 shows this circuit and the typical values required to dampen the ringing.

Ceramic capacitors are also piezoelectric sensitive. The LTC3637's burst frequency depends on the load current, and in some applications at light load the LTC3637 can excite the ceramic capacitor at audio frequencies, generating audible noise. If the noise is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

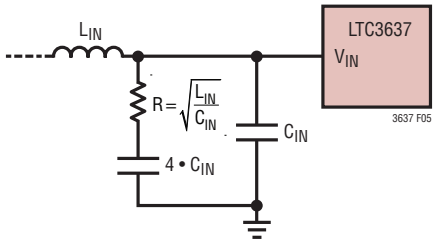


Figure 6. Series RC to Reduce V_{IN} Ringing

Output Voltage Programming

The LTC3637 has three fixed output voltage modes that can be selected with the V_{PRG1} and V_{PRG2} pins and an adjustable mode. The fixed output modes use an internal feedback divider which enables higher efficiency, higher noise immunity, and lower output voltage ripple for 5V, 3.3V and 1.8V applications. To select the fixed 5V output voltage, connect V_{PRG1} to SS and V_{PRG2} to GND. For 3.3V, connect V_{PRG1} to GND and V_{PRG2} to SS. For 1.8V, connect both V_{PRG1} and V_{PRG2} to SS. For any of the fixed output voltage options, directly connect the V_{FB} pin to V_{OUT}.

For the adjustable output mode (V_{PRG1} = 0V, V_{PRG2} = 0V), the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 7. The output voltage can range from 0.8V to V_{IN}. Be careful to keep the divider resistors very close to the V_{FB} pin to minimize the trace length and noise pick-up on the sensitive V_{FB} signal.

APPLICATIONS INFORMATION

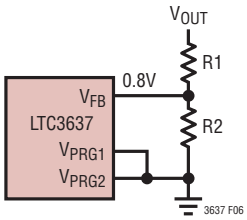


Figure 7. Setting the Output Voltage with External Resistors

To minimize the no-load supply current, resistor values in the megohm range may be used; however, large resistor values should be used with caution. The feedback divider is the only load current when in shutdown. If PCB leakage current to the output node or switch node exceeds the load current, the output voltage will be pulled up. In normal operation, this is generally a minor concern since the load current is much greater than the leakage.

To avoid excessively large values of R1 in high output voltage applications ($V_{OUT} \geq 10V$), a combination of external and internal resistors can be used to set the output voltage. This has an additional benefit of increasing the noise immunity on the V_{FB} pin. Figure 8 shows the LTC3637 with the V_{FB} pin configured for a 5V fixed output with an external divider to generate a higher output voltage. The internal 5M resistance appears in parallel with R2, and the value of R2 must be adjusted accordingly. R2 should be chosen to be less than 200k to keep the output voltage variation less than 1% due to the tolerance of the LTC3637's internal resistor.

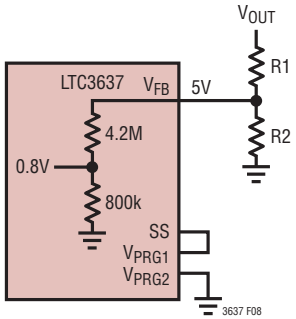


Figure 8. Setting the Output Voltage with External and Internal Resistors

RUN Pin and External Input Overvoltage/Undervoltage Lockout

The RUN pin has two different threshold voltage levels. Pulling the RUN pin below 0.7V puts the LTC3637 into a low quiescent current shutdown mode (I_Q ~ 3µA). When the RUN pin is greater than 1.21V, the controller is enabled. Figure 9 shows examples of configurations for driving the RUN pin from logic.

The RUN and OVLO pins can alternatively be configured as precise undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistive divider from V_{IN} to ground. A simple resistive divider can be used as shown in Figure 10 to meet specific V_{IN} voltage requirements.

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC3637, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}. The

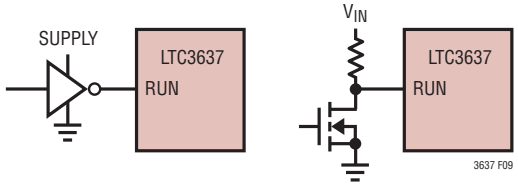


Figure 9. RUN Pin Interface to Logic

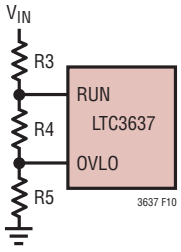


Figure 10. Adjustable UV and OV Lockout

APPLICATIONS INFORMATION

individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ OVLO Threshold}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ UVLO Threshold}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not need a precise external OVLO, the OVLO pin can be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the above equations with R5 = 0Ω.

Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal V_{IN} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the above equations with R3 = 0Ω.

Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3+R4+R5} \right) < 6V$$

Catch Diode Selection

The catch diode D1 conducts current only during switch-off time. Use a Schottky diode to limit forward voltage drop to increase efficiency. The Schottky diode must have a peak reverse voltage that is equal to the regulator maximum input voltage or OVLO set voltage and must be sized for average forward current in normal operation. Average forward current can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT} \bullet V_{IN}}{(V_{IN} - V_{OUT})}$$

An additional consideration is reverse leakage current. When the catch diode is reversed biased, any leakage current will appear as load current. When operating under light load conditions, the low supply current consumed by the LTC3637 will be optimized by using a catch diode with minimum reverse leakage current. Low leakage Schottky diodes often have larger forward voltage drops at a given current, so a trade-off can exist between low load and high load efficiency. Often Schottky diodes with larger reverse bias ratings will have less leakage at a given output voltage than a diode with a smaller reverse bias rating. Therefore, superior leakage performance can be achieved at the expense of diode size.

Soft-Start

Soft-start is implemented by ramping the effective reference voltage from 0V to 0.8V. To increase the duration of soft-start, place a capacitor from the SS pin to ground. An internal 5μA pull-up current will charge this capacitor. The value of the soft-start capacitor can be calculated by the following equation:

$$C_{SS} = \text{Soft-Start Time} \bullet \frac{5\mu A}{0.35V}$$

The minimum soft-start time is limited to the internal soft-start timer of 0.8ms. When the LTC3637 detects a fault condition (input supply undervoltage or overtemperature) or when the RUN pin falls below 1.1V, or when the OVLO pin rises above 1.21V, the SS pin is quickly pulled to ground and the internal soft-start timer is reset. This ensures an orderly restart when using an external soft-start capacitor.

Note that the soft-start capacitor may not be the limiting factor in the output voltage ramp. The maximum output current, which is equal to half the peak current, must charge the output capacitor from 0V to its regulated value. For small peak currents or large output capacitors, this ramp time can be significant. Therefore, the output voltage ramp time from 0V to the regulated V_{OUT} value is limited to a minimum of:

$$\text{Ramp Time} \geq \frac{2 \bullet C_{OUT}}{I_{PEAK}} V_{OUT}$$

Optimizing Output Voltage Ripple

Once the peak current resistor, R_{ISET}, and inductor are selected to meet the load current and frequency requirements, an optional capacitor, C_{ISET}, can be added in parallel with

APPLICATIONS INFORMATION

R_{ISET}. This will boost efficiency at mid-loads and reduce the output voltage ripple dependency on load current at the expense of slightly degraded load step transient response.

The peak inductor current is controlled by the voltage on the I_{SET} pin. Current out of the I_{SET} pin is 5µA while the LTC3637 is switching and is reduced to 1µA during sleep mode. The I_{SET} current will return to 5µA on the first cycle after sleep mode. Placing a parallel RC from the I_{SET} pin to ground filters the I_{SET} voltage as the LTC3637 enters and exits sleep mode which in turn will affect the output voltage ripple, efficiency and load step transient performance.

In general, when R_{ISET} is greater than 120k a C_{ISET} capacitor in the 47pF to 100pF range will improve most performance parameters. When R_{ISET} is less than 100k, the capacitance on the I_{SET} pin should be minimized.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} operating current and I^2R losses. The V_{IN} operating current dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents.

1. The V_{IN} operating current comprises two components: The DC supply current as given in the electrical characteristics and the internal MOSFET gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, ΔQ, moves from V_{IN} to ground. The resulting $\Delta Q/dt$ is the current out of V_{IN} that is typically larger than the DC bias current.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. When switching, the average output current flowing through the inductor is "chopped" between the high side PMOS switch and the external catch diode. Thus, the series resistance looking back into the switch pin is a function of the top and bottom switch $R_{DS(ON)}$ values and the duty cycle ($DC = V_{OUT}/V_{IN}$) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})DC + (R_{DS(ON)BOT}) \bullet (1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current:

   $$I^2R \text{ Loss} = I_O^2(R_{SW} + R_L)$$

   Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total power loss.

Thermal Considerations

In most applications, the LTC3637 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3637 is running at high ambient temperature with low supply voltage and high duty cycles, such as dropout, the heat dissipated may exceed the maximum junction temperature of the part.

To prevent the LTC3637 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise from ambient to junction is given by:

$$T_R = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is given by:

$$T_J = T_A + T_R$$

APPLICATIONS INFORMATION

Generally, the worst-case power dissipation is in dropout at low input voltage. In dropout, the LTC3637 can provide a DC current as high as the full 2.4A peak current to the output. At low input voltage, this current flows through a higher resistance MOSFET, which dissipates more power.

As an example, consider the LTC3637 in dropout at an input voltage of 5V, a load current of 1A and an ambient temperature of 85°C. From the Typical Performance graphs of Switch On-Resistance, the $R_{DS(ON)}$ of the top switch at V_{IN} = 5V and 100°C is approximately 0.6Ω. Therefore, the power dissipated by the part is:

$$P_D = (I_{LOAD})^2 \bullet R_{DS(ON)} = (1A)^2 \bullet 0.6\Omega = 0.6W$$

For the MSOP package the θ_{JA} is 45°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 85°C + 0.6W \bullet \frac{45°C}{W} = 112°C$$

which is below the maximum junction temperature of 150°C.

Note that the while the LTC3637 is in dropout, it can provide output current that is equal to the peak current of the part. This can increase the chip power dissipation dramatically and may cause the internal overtemperature protection circuitry to trigger at 180°C and shut down the LTC3637.

Design Example

As a design example, consider using the LTC3637 in an application with the following specifications: typical V_{IN} = 24V, maximum applied V_{IN} = 80V, V_{OUT} = 3.3V, I_{OUT} = 1A, f = 200kHz. Furthermore, assume for this example that switching should start when V_{IN} is greater than 6V and stop switching when V_{IN} is greater than 48V.

First, calculate the inductor value that gives the required switching frequency:

$$L = \left(\frac{3.3V}{200kHz \bullet 2.4A}\right) \bullet \left(1 - \frac{3.3V}{24V}\right) \cong 4.7\mu H$$

Next, verify that this value meets the L_{MIN} requirement. For this input voltage and peak current, the minimum inductor value is:

$$L_{MIN} = \frac{48V \bullet 150ns}{2.4A} \bullet 1.2 \cong 4\mu H$$

Therefore, the minimum inductor requirement is satisfied and the 4.7µH inductor value may be used.

Next, C_{IN} and C_{OUT} are selected. For this design, C_{IN} should be sized for a current rating of at least:

$$I_{RMS} = 1A \bullet \frac{3.3V}{24V} \bullet \sqrt{\frac{24V}{3.3V} - 1} \cong 350mA_{RMS}$$

The value of C_{IN} is selected to keep the input from drooping less than 240mV (1%):

$$C_{IN} > \frac{4.7\mu H \bullet 2.4A^2}{2 \bullet 24V \bullet 240mV} \cong 2.2\mu F$$

C_{OUT} will be selected based on a value large enough to satisfy the output voltage ripple requirement. For a 50mV output ripple, the value of the output capacitor can be calculated from:

$$C_{OUT} > \frac{4.7\mu H \bullet 2.4A^2}{2 \bullet 3.3V \bullet 50mV} \cong 100\mu F$$

C_{OUT} also needs an ESR that will satisfy the output voltage ripple requirement. The required ESR can be calculated from:

$$ESR < \frac{50mV}{2.4A} \cong 20m\Omega$$

A 100µF ceramic capacitor has significantly less ESR than 20mΩ.

Since an output voltage of 3.3V is one of the standard output configurations, the LTC3637 can be configured by connecting V_{PRG1} to ground and V_{PRG2} to the SS pin.

The undervoltage and overvoltage lockout requirements on V_{IN} can be satisfied with a resistive divider from V_{IN} to the RUN and OVLO pins (refer to Figure 9). Pick R_{TOTAL} = 1M = R3 + R4 + R5 to minimize the loading on V_{IN} and calculate R3, R4 and R5 as follows (standard values):

$$R5 = 1M \bullet \frac{1.21V}{48V} = 24.9k$$

$$R4 = 1M \bullet \frac{1.21V}{6V} - 24.9k = 174k$$

$$R3 = 1M - 24.9k - 174k = 806k$$

APPLICATIONS INFORMATION

Note that the V_{IN} falling thresholds for both UVLO and OVLO will be 10% less than the rising thresholds or 5.4V and 43V respectively.

The absolute maximum rating on the OVLO pin (6V) is not violated based on the following:

$$OVLO(MAX) = 80V \bullet \frac{24.9k}{(806k + 174k + 24.9k)} = 2V$$

The I_{SET} pin should be left open in this example to select maximum peak current (2.4A typical). Figure 11 shows a complete schematic for this design example.

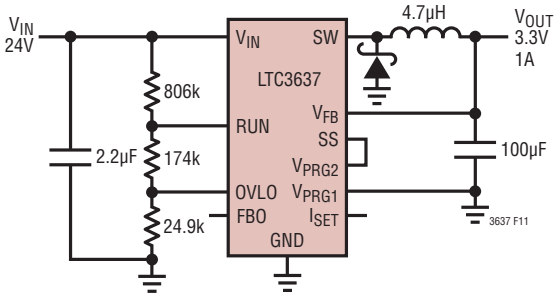
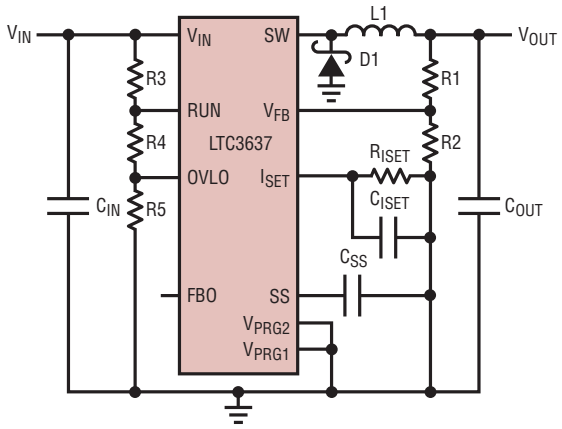


Figure 11. 24V to 3.3V, 1A Regulator at 200kHz

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3637. Check the following in your layout:

1. Large switched currents flow in the power switches and input capacitor. The loop formed by these components should be as small as possible. A ground plane is recommended to minimize ground impedance.
2. Connect the (+) terminal of the input capacitor, C_{IN}, as close as possible to the V_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small signal nodes. The rapid transitions on the switching node can couple to high impedance nodes, in particular V_{FB}, and create increased output ripple.
4. Flood all unused area on all layers with copper except for the area under the inductor. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND, or any other DC rail in your system).



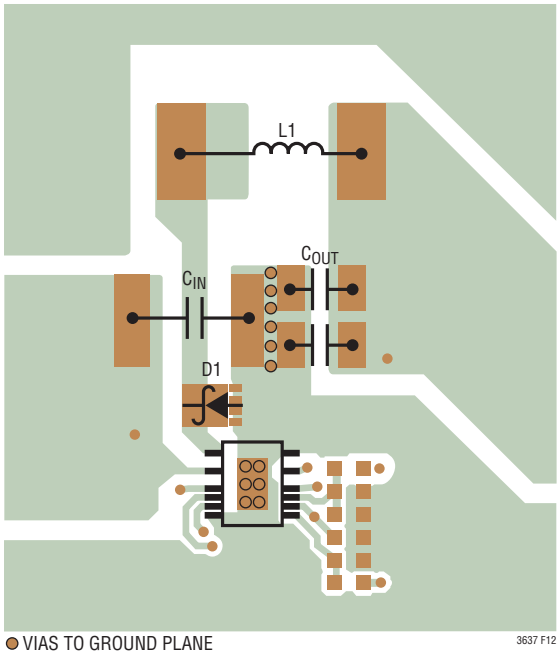
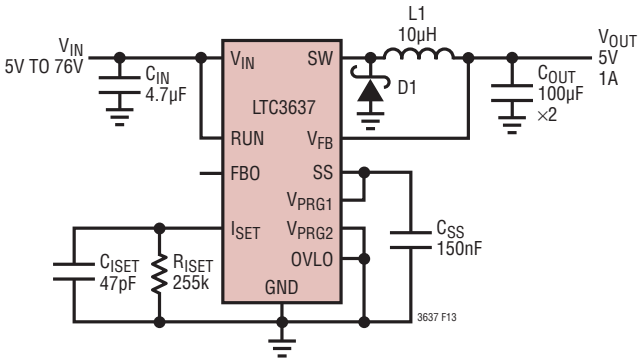


Figure 12. Example PCB Layout

Pin Clearance/Creepage Considerations

The LTC3637 is available in two packages (MSE16 and DHC) both with identical functionality. However, the 0.2mm (minimum space) between pins and paddle on the DHC package may not provide sufficient PC board trace clearance between high and low voltage pins in some higher voltage applications. In applications where clearance is required, the MSE16 package should be used. The MSE16 package has removed pins between all the adjacent high voltage and low voltage pins, providing 0.657mm clearance which will be sufficient for most applications. For more information, refer to the printed circuit board design standards described in IPC-2221 (www.ipc.org).

TYPICAL APPLICATIONS



C_{IN}: TDK C5750X7R2A-475M
C_{OUT}: 2 ×MURATA GRM32ER61A107ME20L
D1: DIODES INC. SBR3U100LP
L1: SUMIDA CDRH105R-100

Soft-Start Waveform

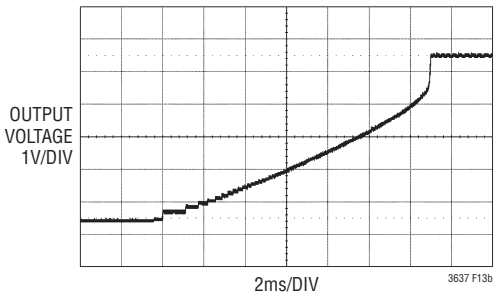
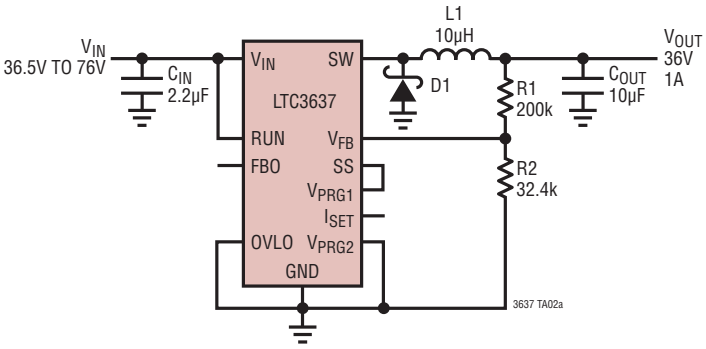
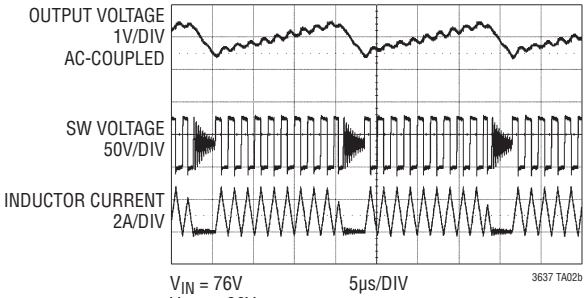


Figure 13. 5V-76V Input to 5V Output, 1A Regulator with Soft-Start

36.5V to 76V Input to 36V Output, 1A Regulator

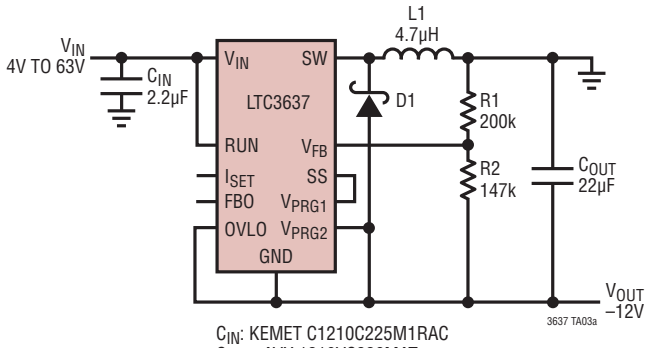


C_{IN}: TDK CGA6N3X7R2A225M
C_{OUT}: TAIYO YUDEN UMK325BJ106MM
D1: DIODES INC. ES2BA-13-F
L1: TDK SLF10145T-100M



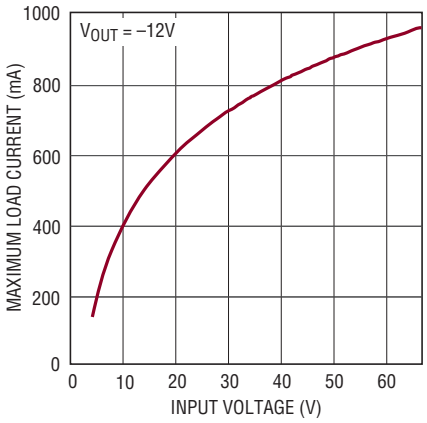
TYPICAL APPLICATIONS

4V to 64V Input to –12V Output Positive-to-Negative Regulator



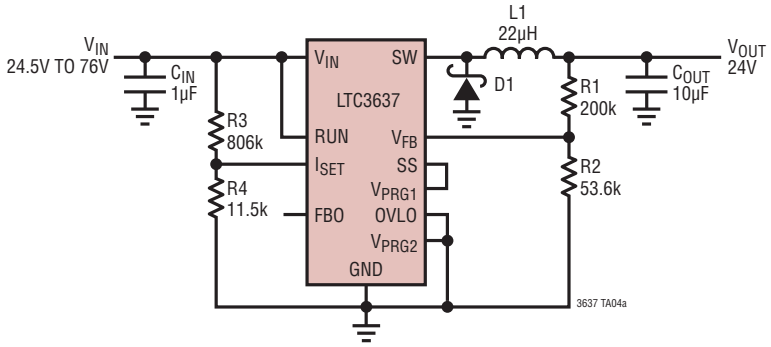
C_{IN}: KEMET C1210C225M1RAC
C_{OUT}: AVX 1210YC226MAT
D1: AVX SD3220S100S5R0
L1: COOPER BUSSMANN DR7-4R7-R

Maximum Load Current vs Input Voltage



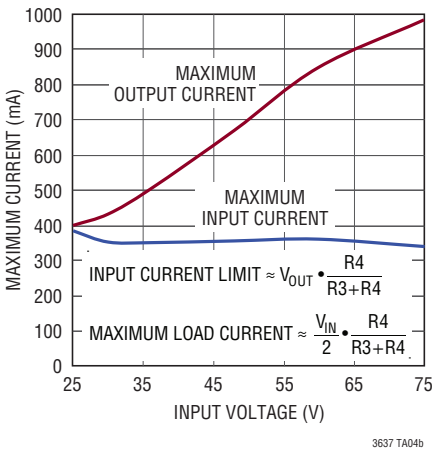
$$\text{MAXIMUM LOAD CURRENT} \approx \frac{V_{IN}}{V_{IN}+|V_{OUT}|} \bullet \frac{I_{PEAK}}{2}$$

24.5V to 76V Input to 24V Output with 350mA Input Current Limit



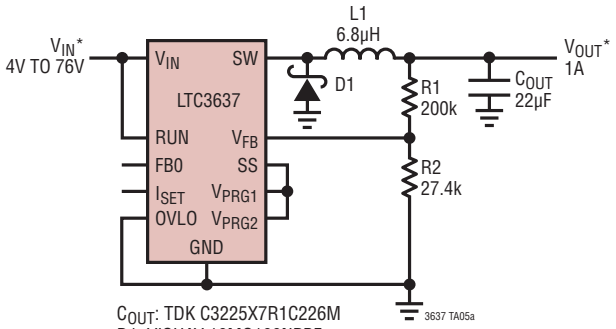
C_{IN}: TAIYO YUDEN HMK325B7105MN
C_{OUT}: TDK C3225X7R1H106M
D1: DIODES INC. SBR3U100LP
L1: WÜRTH 7447714220

Maximum Input and Load Current vs Input Voltage



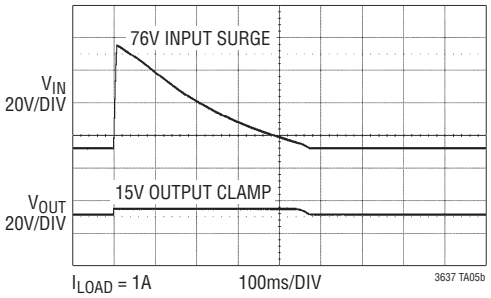
TYPICAL APPLICATIONS

4V to 76V Input to 15V Output* Clamp, 1A High Efficiency Surge Stopper

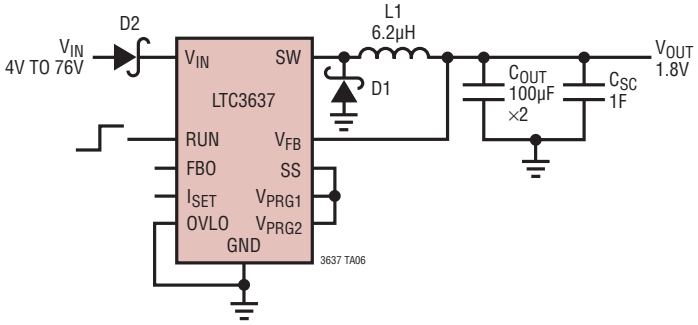


C_{OUT}: TDK C3225X7R1C226M
D1: VISHAY 10MQ100NPBF
L1: VISAHY IHLP-2525CZ-01

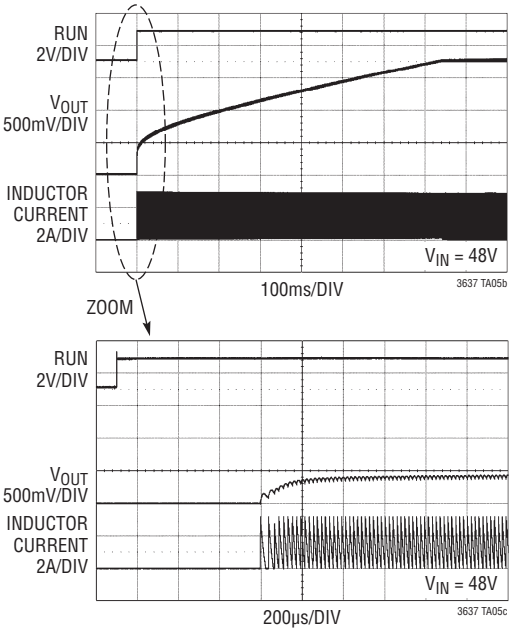
*WHEN V_{IN} > 15V, LTC3637 SWITCHES AND V_{OUT} IS REGULATED TO 15V;
WHEN V_{IN} ≤ 15V, LTC3637 OPERATES IN DROPOUT AND V_{OUT} FOLLOWS V_{IN}



4V to 76V Input to 1.8V SuperCap Charger



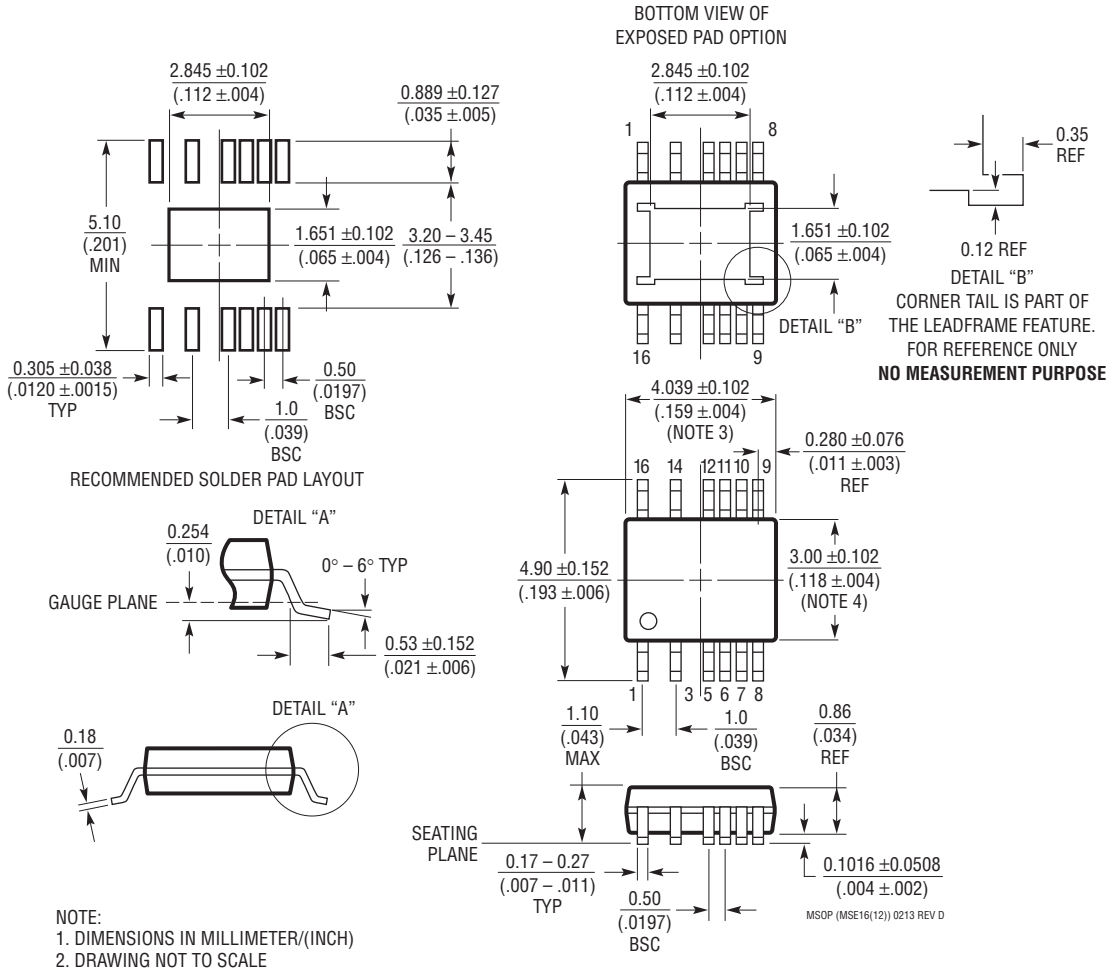
C_{OUT}: TDK C3225X5R0J107M
C_{SC}: COOPER BUSSMANN M0810-2R5105-R
D1: VISHAY VSSA310S-E3
D2: VISHAY 10MDQ100NPBF
L1: WÜRTH 744 066 0062



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
Variation: MSE16 (12)
16-Lead Plastic MSOP with 4 Pins Removed
Exposed Die Pad
(Reference LTC DWG # 05-08-1871 Rev D)

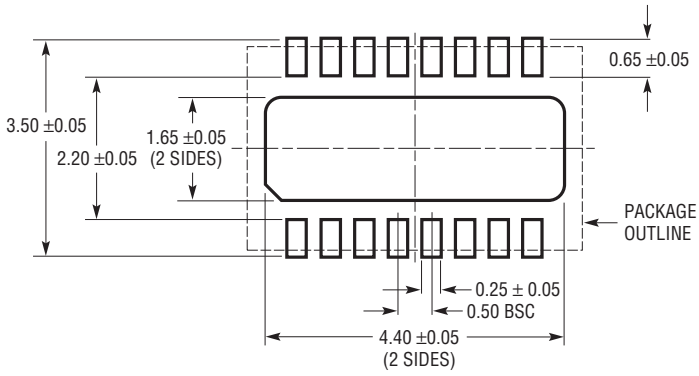


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

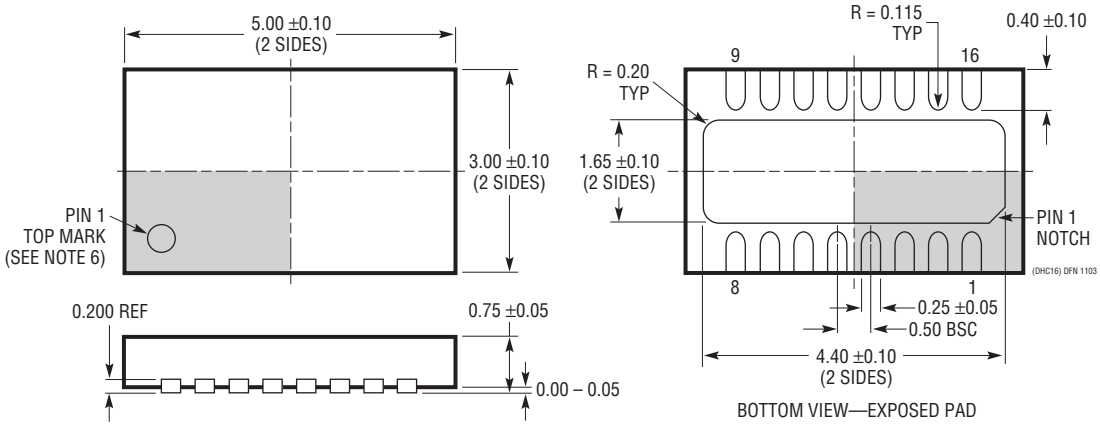
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/14	Clarify FBO and UVLO pin description	7
		Fix typos on Block Diagram. Clarify SS operation.	8
		Clarify FBO operation	10
		Clarify Design Example	18