RL78/G11

RENESAS MCU

R01DS0282EJ0200
Rev.2.00
Feb 15, 2018

True Low Power Platform (as low as 58.3 μA/MHz, and 0.64 μA for LVD), 1.6 V to 5.5 V operation, 16 Kbyte Flash, 33 DMIPS at 24 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- V_{DD} = 1.6 V to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 μs: @ 24 MHz operation with high-speed on-chip oscillator) to ultra-low speed (66.6 μs: @ 15 kHz operation with low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 Mbytes
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 1.5 Kbytes

Code flash memory

- Code flash memory: 16 Kbytes
- Block size: 1 Kbytes
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 2 Kbytes
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Middle-speed on-chip oscillator

- Selectable from 4 MHz, 2 MHz, and 1 MHz.

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications)
- T_A = -40 to +105°C (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event link controller (ELC)

- Event signals of 18 types can be linked to the specified peripheral function.

Serial interfaces

- CSI: 4 channels
- UART: 2 channel
- I^2C/simplified I^2C: 4 channels
- Multimaster I^2C: 2 channels

Timers

- 16-bit timer (TAU): 4 channels
- TKB: 1 channel
- 12-bit interval timer: 1 channel
- <R> 8-bit interval timer: 2 channels
- Watchdog timer: 1 channel

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 10 to 11 channels
- Internal reference voltage (1.45 V) and temperature sensor

D/A converter

- 8/10-bit resolution D/A converter (V_{DD} = 1.6 to 5.5 V)
- <R> Analog input: 2 channels (channel 1: output to the ANO1 pin, channel 0: output to the comparator)
- Output voltage: 0 V to V_{DD}
- Real-time output function

Comparator

- 2 channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode

PGA

- 1 channels

I/O ports

- I/O port: 17 to 21 (N-ch open drain I/O [V_{DD} withstand voltage[Note 1]/EV_{DD} withstand voltage[Note 2]]: 10 to 14)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3.0 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit
- On-chip data operation circuit

Note 1. 16, 20, 24-pin products

Note 2. 25-pin products

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G11				
			10 pins	16 pins	20 pins	24 pins	25 pins
16 KB	2 KB	1.5 KB	R5F1051A	R5F1054A	R5F1056A	R5F1057A	R5F1058A

Remark The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11

Part No. R 5 F 1 0 5 8 A G x x x L A # U 0

- Packaging specification
  - #30: Tube (LSSOP), Tray (LSSOP, SSOP)
  - #U0: Tray (HWQFN, WFLGA)
  - #50: Embossed Tape (LSSOP, SSOP)
  - #W0: Embossed Tape (HWQFN, WFLGA)
- Package type:
  - SP: LSSOP, SSOP, 0.65 mm pitch
  - NA: HWQFN, 0.50 mm pitch
  - LA: WFLGA, 0.50 mm pitch
- ROM number (Omitted for blank products)
- Fields of application:
  - A: Consumer applications, T_A = -40 to +85°C
  - G: Industrial applications, T_A = -40 to +105°C
- ROM capacity:
  - A: 16 KB
- Pin count:
  - 1: 10-pin
  - 4: 16-pin
  - 6: 20-pin
  - 7: 24-pin
  - 8: 25-pin
- RL78/G11
- Memory type:
  - F : Flash memory
- Renesas MCU
- Renesas semiconductor product

Pin count	Package	Ordering Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)	R5F1051AGSP#30, R5F1051AASP#30 R5F1051AGSP#50, R5F1051AASP#50
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)	R5F1054AGSP#30, R5F1054AASP#30 R5F1054AGSP#50, R5F1054AASP#50
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	R5F1056AGSP#30,R5F1056AASP#30 R5F1056AGSP#50,R5F1056AASP#50
24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.50 mm pitch)	R5F1057AGNA#U0,R5F1057AANA#U0 R5F1057AGNA#W0,R5F1057AANA#W0
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)	R5F1058AGLA#U0,R5F1058AALA#U0 R5F1058AGLA#W0,R5F1058AALA#W0

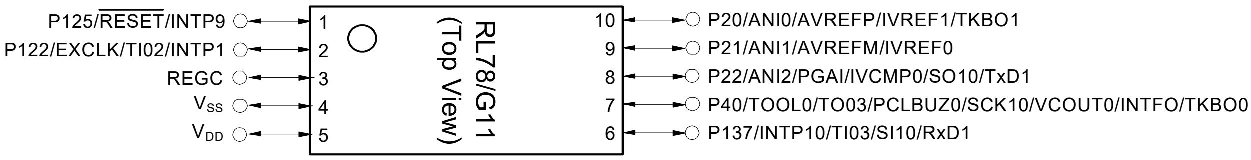
Caution 1. For the fields of application, refer to Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11.

Caution 2. The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

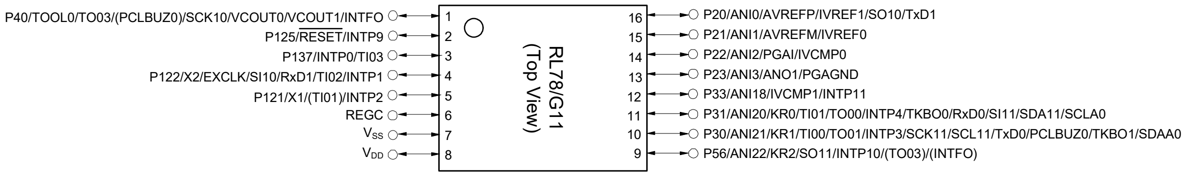
1.3.1 10-pin products

• 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)



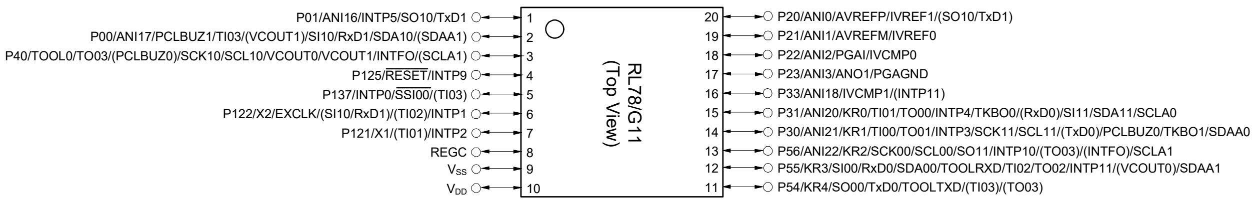
1.3.2 16-pin products

• 16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)



1.3.3 20-pin products

• 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)



Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

1.3.4 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

Caution **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

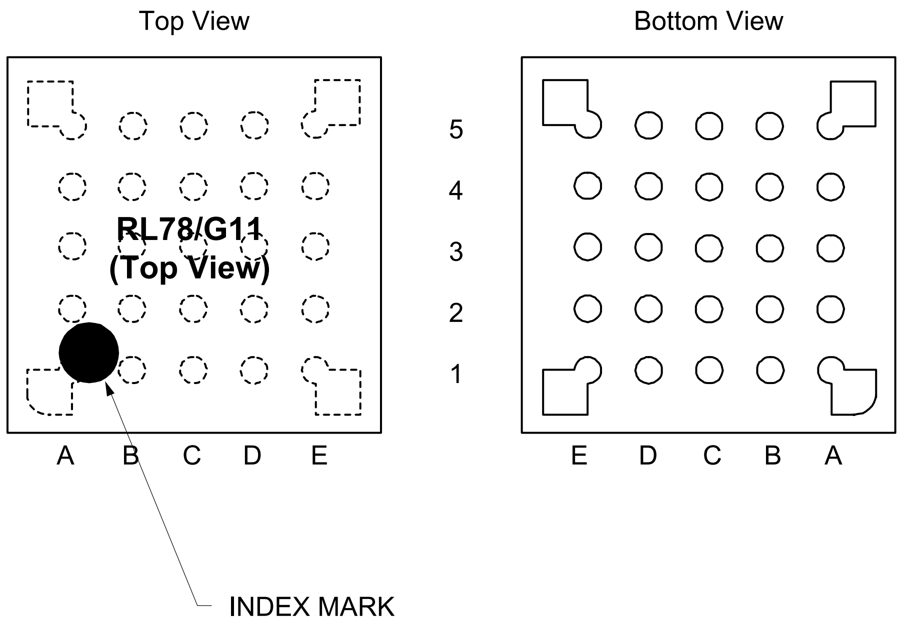
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. It is recommended to connect an exposed die pad to Vss.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

1.3.5 25-pin products

• 25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)



	A	B	C	D	E	
5	P40/TOOL0/TO03/(PCLBUZ0)/SCK10/SCL10/VCOUT0/VCOUT1/INTFO/(SCLA1)	P125/$\overline{\text{RESET}}$/INTP9	P01/ANI16/INTP5/SO10/TxD1	P20/ANI0/AVREFP/IVREF1/(SO10/TxD1)	P21/ANI1/AVREFM/IVREF0	5
4	P122/X2/EXCLK/(SI10/RxD1)/(TI02)/INTP1	P137/INTP0/$\overline{\text{SSI00}}$/(TI03)	P00/ANI17/PCLBUZ1/TI03/(VCOUT1)/SI10/RxD1/SDA10/(SDAA1)	P22/ANI2/PGAI/IVCMP0	P23/ANI3/ANO1/PGAGND	4
3	P121/X1/(TI01)/INTP2/(SI01)	V_{DD}	EV_{DD}	P33/ANI18/IVCMP1/(INTP11)/(SCLA1)	P32/ANI19/SO11/(INTP10)/(VCOUT1)/(SDAA1)	3
2	REGC	V_{SS}	P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0)/PCLBUZ0/TKBO1/(SDAA0)	P31/ANI20/KR0/TI01/TO00/INTP4/TKBO0/(RxD0)/SI11/SDA11/(SCLA0)	P56/ANI22/KR2/SCK00/SCL00/(SO11)/INTP10/(TO03)/(INTFO)/SCLA1	2
1	P51/KR7/INTP8/(TI02)/(TO02)/SCK01/SCL01/(TxD0)	P52/KR6/INTP7/SI01/SDA01/(RxD0)/(SDAA0)	P53/KR5/INTP6/SO01/SDAA0	P54/KR4/SO00/TxD0/TOOLTXD/(TI03)/(TO03)/SCLA0	P55/KR3/SI00/RxD0/SDA00/TOOLRXD/TI02/TO02/INTP11/(VCOUT0)/SDAA1	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

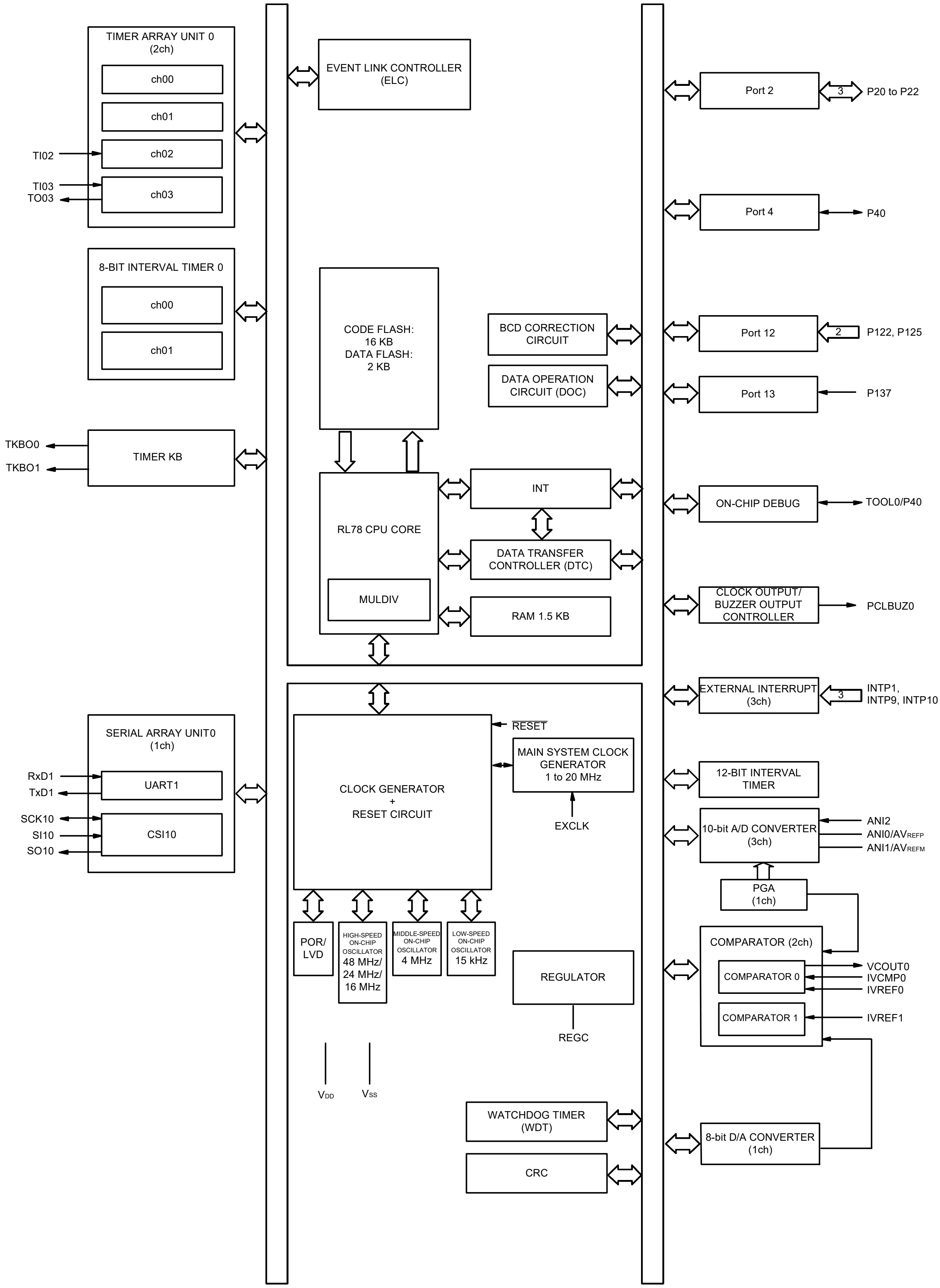
1.4 Pin Identification

ANI0 to ANI3, ANI16 to ANI22	: Analog input
ANO1	: Analog output
AV_{REFM}	: A/D converter reference potential (- side) input
AV_{REFP}	: A/D converter reference potential (+ side) input
EV_{DD}	: Power supply
EXCLK	: External clock input (main system clock)
INTP0 to INTP11	: External interrupt input
INTFO	: Interrupt Flag output
IVCMP0, IVCMP1	: Comparator input
IVREF0, IVREF1	: Comparator reference input
KR0 to KR7	: Key return
PGAI, PGAGND	: PGA Input
P00 to P01	: Port 0
P20 to P23	: Port 2
P30 to P33	: Port 3
P40	: Port 4
P51 to P56	: Port 5
P121, P122, P125	: Port 12
P137	: Port 13

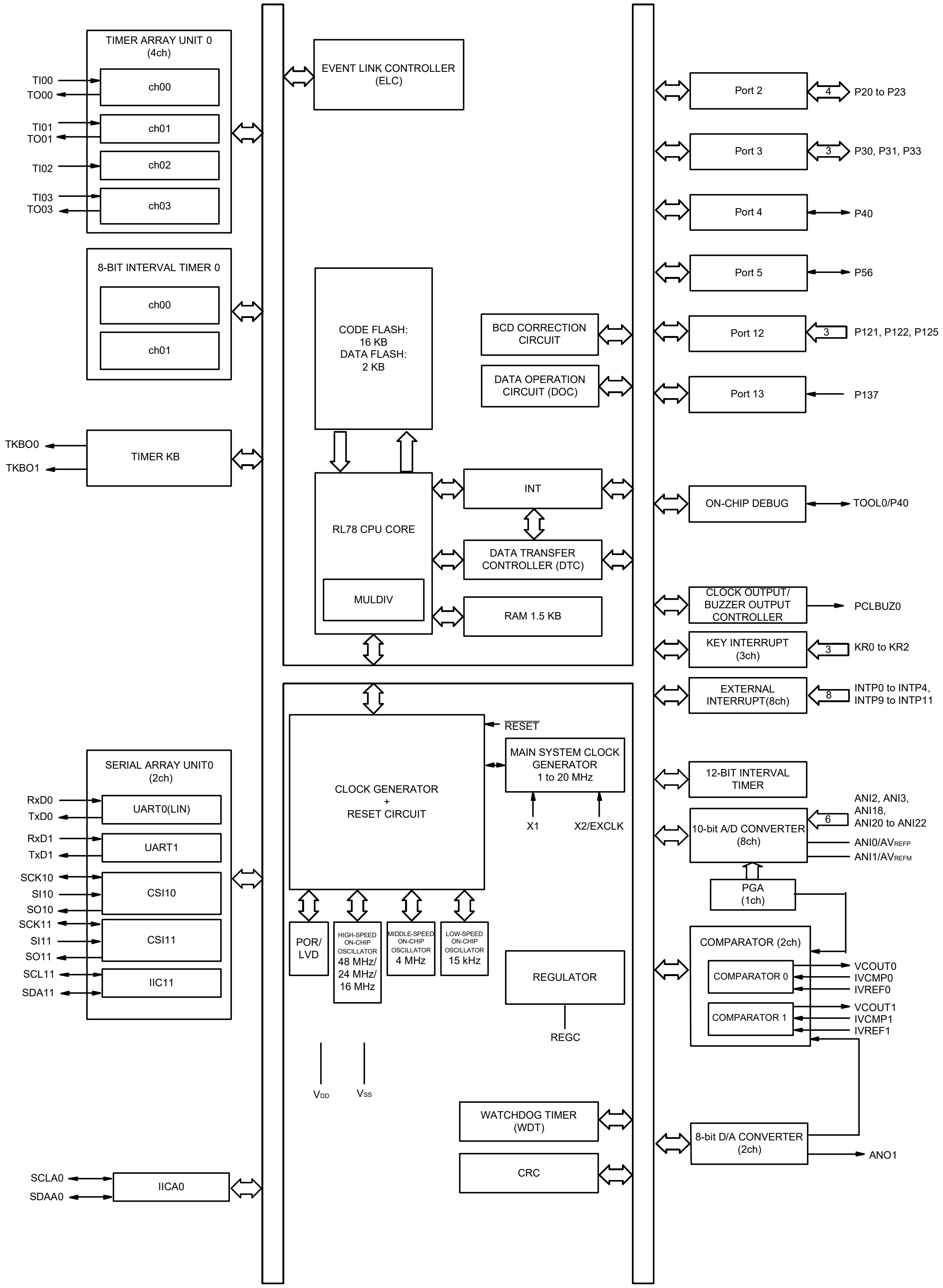
PCLBUZ0, PCLBUZ1	: Programmable clock output/buzzer output
REGC	: Regulator capacitance
$\overline{\text{RESET}}$	: Reset
RxD0, RxD1	: Receive data
SCK00, SCK01 SCK10, SCK11	: Serial clock input/output
SCLA0, SCLA1	: Serial clock input/output
SCL00, SCL01 SCL10, SCL11	: Serial clock output
SDAA0, SDAA1	: Serial data input/output
SDA00, SDA01 SDA10, SDA11	: Serial data input/output
SI00, SI01 SI10, SI11	: Serial data input
SO00, SO01 SO10, SO11	: Serial data output
$\overline{\text{SSI00}}$	: Serial interface chip select input
TI00 to TI03	: Timer input
TKBO0, TKBO1	: TMKB output
TO00 to TO03	: Timer output
TOOL0	: Data input/output for tool
TOOLRXD, TOOLTXD	: Data input/output for external device
TxD0, TxD1	: Transmit data
VCOUT0, VCOUT1	: Comparator output
V_{DD}	: Power supply
V_{SS}	: Ground
X1, X2	: Crystal oscillator (main system clock)

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



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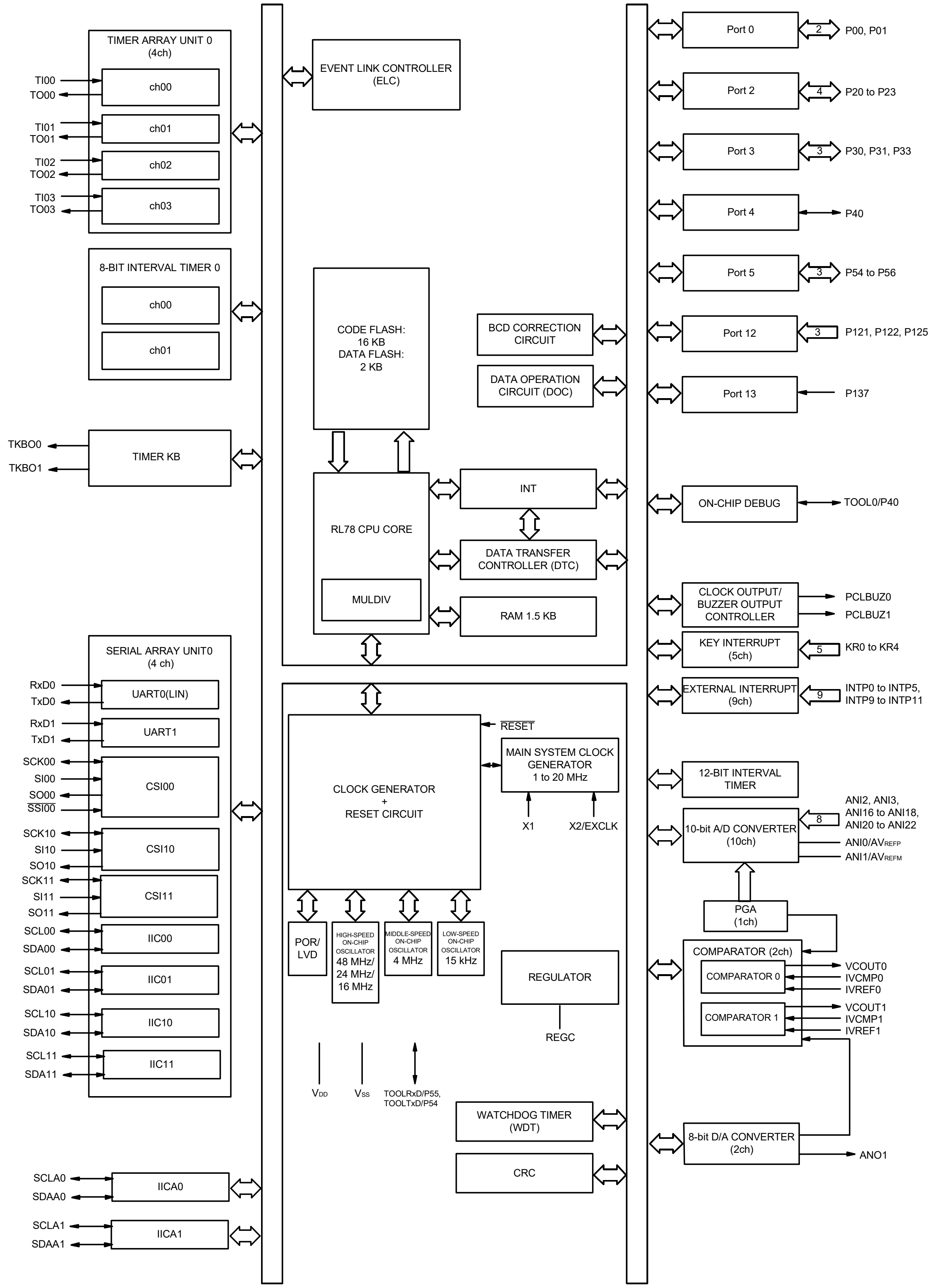
1.5.3 20-pin products



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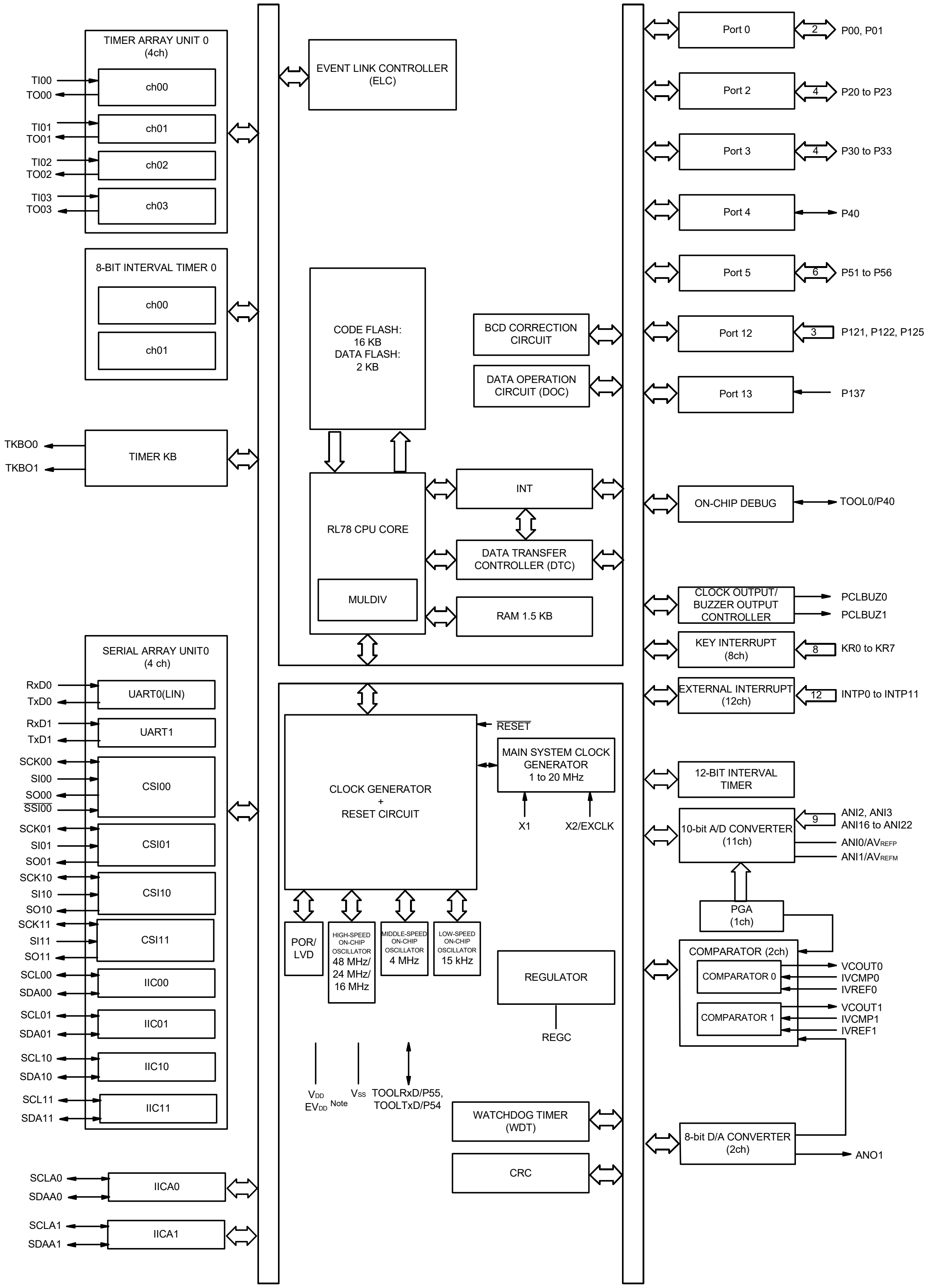
1.5.4 24-pin, 25-pin products



Note 25-pin products

1.6 Outline of Functions

This outline describes the functions at the time when Peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3) are set to 00H.

(1/2)

<table>
<tr><th colspan="2" rowspan="2">Item</th><th>10-pin</th><th>16-pin</th><th>20-pin</th><th>24-pin</th><th>25-pin</th></tr>
<tr><th>R5F1051A</th><th>R5F1054A</th><th>R5F1056A</th><th>R5F1057A</th><th>R5F1058A</th></tr>
<tr><td colspan="2">Code flash memory (KB)</td><td colspan="5">16 Kbytes</td></tr>
<tr><td colspan="2">Data flash memory (KB)</td><td colspan="5">2 Kbytes</td></tr>
<tr><td colspan="2">RAM</td><td colspan="5">1.5 Kbytes</td></tr>
<tr><td colspan="2">Address space</td><td colspan="5">1 Mbytes</td></tr>
<tr><td rowspan="3">Main system clock</td><td>High-speed system clock (f_{MX})</td><td colspan="5">X1 (crystal/ceramic) oscillation[Note], external main system clock input (EXCLK)
1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 16 MHz: V_{DD} = 2.4 to 2.7 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.4 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V</td></tr>
<tr><td>High-speed on-chip oscillator clock (f_{IH}) Max: 24 MHz</td><td colspan="5" rowspan="2">HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V),
HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V),
LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V),
LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V),
LP (Low-power main) mode: 1 MHz (V_{DD} = 1.8 to 5.5 V)</td></tr>
<tr><td>Middle-speed on-chip oscillator clock (f_{IM}) Max: 4 MHz</td></tr>
<tr><td><R> Subsystem clock</td><td>Low-speed on-chip oscillator clock (f_{IL})</td><td colspan="5">15 kHz (typ.): V_{DD} = 1.6 to 5.5 V</td></tr>
<tr><td colspan="2">General-purpose register</td><td colspan="5">8 bits × 32 registers (8 bits × 8 registers × 4 banks)</td></tr>
<tr><td colspan="2" rowspan="2">Minimum instruction execution time</td><td colspan="5">0.04167 µs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)</td></tr>
<tr><td colspan="5">0.05 µs (High-speed system clock: f_{MX} = 20 MHz operation)</td></tr>
<tr><td colspan="2">Instruction set</td><td colspan="5">• Data transfer (8/16 bits)
• Adder and subtractor/logical operation (8/16 bits)
• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)
• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)
• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</td></tr>
<tr><td rowspan="3">I/O port</td><td>Total</td><td>7</td><td>13</td><td>17</td><td colspan="2">21</td></tr>
<tr><td>CMOS I/O</td><td>4</td><td>9</td><td>13</td><td colspan="2">17</td></tr>
<tr><td>CMOS input</td><td>3</td><td colspan="4">4</td></tr>
<tr><td rowspan="6">Timer</td><td>16-bit timer</td><td colspan="5">4 channels</td></tr>
<tr><td>Watchdog timer</td><td colspan="5">1 channel</td></tr>
<tr><td>Timer KB</td><td colspan="5">1 channel</td></tr>
<tr><td>12-bit interval timer</td><td colspan="5">1 channel</td></tr>
<tr><td>8/16-bit interval timer</td><td colspan="5">2 channels (8 bit)/1 channel (16 bit)</td></tr>
<tr><td>Timer output</td><td>3</td><td>5</td><td colspan="3">6</td></tr>
</table>

Note 16, 20, 24, 25-pin products

Caution The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

(2/2)

Item		10-pin	16-pin	20-pin	24-pin	25-pin
		R5F1051A	R5F1054A	R5F1056A	R5F1057A	R5F1058A
Clock output/buzzer output		1		2		
<R>		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 117 Hz, 234 Hz, 469 Hz, 938 Hz, 1.875 kHz, 3.75 kHz, 7.5 kHz, 15 kHz (subsystem clock: f_{IL} = 15 kHz operation)				
10-bit resolution A/D converter	External	3 channels	8 channels	10 channels	11 channels	
	Internal	1 channel				
8-bit D/A converter		1 channel	2 channels			
Comparator (Window Comparator)		1 channel	2 channels			
PGA		1 channel				
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data				
<R> Serial interface		[10-pin products] • CSI: 1 channel/UART: 1 channel [16-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^{2}C: 1 channel [20-pin products] • CSI: 3 channel/UART: 2 channel/simplified I^{2}C: 3 channel [24-pin, 25-pin products] • CSI: 4 channels/UART: 2 channel/simplified I^{2}C: 4 channels				
	I^{2}C bus	None	1 channel	2 channels		
Data transfer controller (DTC)		13 sources	22 sources	23 sources	24 sources	
Event link controller (ELC)		Event input: 11 Event trigger output: 3	Event input: 16 Event trigger output: 4	Event input: 17 Event trigger output: 4	Event input: 18 Event trigger output: 4	
Vectored interrupt sources	Internal	20	24	25		
	External	3	9	10	13	
Key interrupt		None	3	5	8	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ± 0.04V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C) • Power-down-reset: 1.50 ± 0.04 V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C)				
Voltage detector	Power on	1.67 V to 4.06 V (14 stages)				
	Power down	1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided (Disable to tracing)				
Power supply voltage		V_{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T_A = -40 to +85°C (Consumer applications) T_A = -40 to +105°C (Industrial applications)				

2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications (T_A = −40 to +85°C)
R5F105xxAxx
G: When the products "G: Industrial applications (T_A = −40 to +105°C)" is used in the range of T_A = -40 to +85°C
R5F105xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G11 User's Manual.

Caution 3. The EV_{DD} pin is not present on products with 24 or less pins. Accordingly, replace EV_{DD} with V_{DD} and the voltage condition 1.6 ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V with 1.6 ≤ V_{DD} ≤ 5.5 V.

2.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, EV_{DD}	$V_{DD} \leq EV_{DD}$	-0.5 to + 6.5	V
	AV_{REFP}		0.3 to V_{DD} + 0.3 Note 2	V
	AV_{REFM}		-0.3 to V_{DD} + 0.3 Note 2 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to + 2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P20 to P23, P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P23	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI22	-0.3 to EV_{DD} + 0.3 and -0.3 to $AV_{REF}(+)$ + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI3	-0.3 to V_{DD} + 0.3 and -0.3 to $AV_{REF}(+)$ + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P00, P01, P40	-70	mA
			P30 to P33, P51 to P56	-100	mA
	I_{OH2}	Per pin	P20 to P23	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P00, P01, P40	70	mA
			P30 to P33, P51 to P56	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		4	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} ≤ 5.5 V		1		16	
		1.8 V ≤ V_{DD} ≤ 5.5 V		1		8	
		1.6 V ≤ V_{DD} ≤ 5.5 V		1		4	
High-speed on-chip oscillator clock frequency accuracy		T_A = -20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1		1	%
			1.6 V ≤ V_{DD} < 1.8 V	-5		5	
		T_A = -40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		5.5	
Middle-speed on-chip oscillator oscillation frequency Note 2	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy				-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMT}				0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMV}	T_A = 25°C	2.1 V ≤ V_{DD} ≤ 5.5 V		0.02		%/V
			2.0 V ≤ V_{DD} < 2.1 V		-12		
			1.6 V ≤ V_{DD} < 2.0 V		10		
Low-speed on-chip oscillator clock frequency Note 2	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				-10.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-42.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			-2.5	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			-5.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-122.0	mA
	I_{OH2}	Per pin for P20 to P23				-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			-0.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OH} = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				20.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			4.5	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD} < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				150.0	mA
	I_{OL2}	Per pin for P20 to P23				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ V_{DD} ≤ 5.5 V			1.6	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R>

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0.8 EV_{DD}		EV_{DD}	V
	V_{IH2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P23 (digital input)		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0		0.2 EV_{DD}	V
	V_{IL2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IH3}	P20 to P23 (digital input)		0		0.3 V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{RESET}$		0		0.2 V_{DD}	V

Caution **The maximum value of V_{IH} of pins P00, P01, P20, P30 to P33, P40 and P51 to P56 is V_{DD} or EV_{DD}, even in the N-ch open-drain mode.**
(P20: V_{DD}
P00, P01, P30 to P33, P40, P51 to P56: EV_{DD})

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	EV_{DD} - 1.5			V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	EV_{DD} - 0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	EV_{DD} - 0.6			V
			1.8 V ≤ EV_{DD} ≤ 5.5 V I_{OH} = -1.5 mA	EV_{DD} - 0.5			V
			1.6 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -1.0 mA	EV_{DD} - 0.5			V
	V_{OH2}	P20 to P23	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P23	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 400 μA			0.4	V

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P30 to P33, P40, and P51 to P56	V_I = EV_{DD}				1	μA
	I_{LIH2}	P20 to P23, P125, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121, P122, X1, X2, EXCLK	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P30 to P33, P40, and P51 to P56	V_I = V_{SS}				-1	μA
	I_{LIL2}	P20 to P23, P125, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121, P122, X1, X2, EXCLK	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00, P01, P30 to P33, P40, P51 to P56, P125	V_I = V_{SS}, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/4)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.7		mA
						V_{DD} = 3.0 V			1.7		
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.4		
						V_{DD} = 3.0 V			1.4		
			Normal operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.5	6.9	mA
						V_{DD} = 3.0 V			3.5	6.9	
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.2	6.3	
						V_{DD} = 3.0 V			3.2	6.3	
					f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V			2.4	4.6	
						V_{DD} = 3.0 V			2.4	4.6	
<R>			Normal operation	LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 3	V_{DD} = 3.0 V			1.1	2.0	mA
						V_{DD} = 2.0 V			1.1	2.0	
			Normal operation	LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 3	V_{DD} = 3.0 V			0.72	1.3	mA
						V_{DD} = 2.0 V			0.72	1.3	
<R>					f_{IM} = 4 MHz Note 6	V_{DD} = 3.0 V			0.58	1.1	
						V_{DD} = 2.0 V			0.58	1.1	
			Normal operation	LV (low-voltage main) mode	f_{IH} = 4 MHz Note 3	V_{DD} = 3.0 V			1.2	1.8	mA
						V_{DD} = 2.0 V			1.2	1.8	
			Normal operation	LP (low-power main) mode (MCSEL = 1)	f_{IH} = 1 MHz Note 3	V_{DD} = 3.0 V			290	480	μA
						V_{DD} = 2.0 V			290	480	
					f_{IM} = 1 MHz Note 6	V_{DD} = 3.0 V			124	230	
						V_{DD} = 2.0 V			124	230	
			Normal operation	HS (high-speed main) mode	f_{MX} = 20 MHz Note 2	V_{DD} = 5.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	
						V_{DD} = 3.0 V	Square wave input		2.7	5.3	
							Resonator connection		2.8	5.5	
					f_{MX} = 10 MHz Note 2	V_{DD} = 5.0 V	Square wave input		1.8	3.1	
							Resonator connection		1.9	3.2	
						V_{DD} = 3.0 V	Square wave input		1.8	3.1	
							Resonator connection		1.9	3.2	
			Normal operation	LS (low-speed main) mode (MCSEL = 0)	f_{MX} = 8 MHz Note 2	V_{DD} = 3.0 V	Square wave input		0.9	1.9	mA
							Resonator connection		1.0	2.0	
			Normal operation		f_{MX} = 8 MHz Note 2	V_{DD} = 2.0 V	Square wave input		0.9	1.9	
							Resonator connection		1.0	2.0	
			Normal operation	LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 2	V_{DD} = 3.0 V	Square wave input		0.6	1.1	mA
							Resonator connection		0.6	1.2	
			Normal operation		f_{MX} = 4 MHz Note 2	V_{DD} = 2.0 V	Square wave input		0.6	1.1	
							Resonator connection		0.6	1.2	
			Normal operation	LP (low-power main) mode (MCSEL = 1)	f_{MX} = 1 MHz Note 2	V_{DD} = 3.0 V	Square wave input		100	190	μA
							Resonator connection		145	250	
			Normal operation		f_{MX} = 1 MHz Note 2	V_{DD} = 2.0 V	Square wave input		100	190	
							Resonator connection		145	250	

(**Notes** and **Remarks** are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/4)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation	Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 5	Normal operation			1.8	5.9	μA
					f_{IL} = 15 kHz, T_A = +25°C Note 5	Normal operation			1.9	5.9	
					f_{IL} = 15 kHz, T_A = +85°C Note 5	Normal operation			2.3	8.7	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock is stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(3/4)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 4, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V			0.59	2.43	mA
					V_{DD} = 3.0 V			0.59	2.43	
				f_{HOCO} = 24 MHz Note 4, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V			0.41	1.83	
					V_{DD} = 3.0 V			0.41	1.83	
				f_{HOCO} = 16 MHz Note 4, f_{IH} = 16 MHz Note 4,	V_{DD} = 5.0 V			0.39	1.38	
					V_{DD} = 3.0 V			0.39	1.38	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V			250	710	μA
					V_{DD} = 2.0 V			250	710	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V			204	400	μA
					V_{DD} = 2.0 V			204	400	
				f_{IM} = 4 MHz Note 6	V_{DD} = 3.0 V			43	250	
					V_{DD} = 2.0 V			43	250	
			LV (low-voltage main) mode	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V			450	700	mA
					V_{DD} = 2.0 V			450	700	
			LP (low-power main) mode (MCSEL = 1)	f_{IH} = 1 MHz Note 4	V_{DD} = 3.0 V			192	400	μA
					V_{DD} = 2.0 V			192	400	
				f_{IM} = 1 MHz Note 6	V_{DD} = 3.0 V			28	100	
					V_{DD} = 2.0 V			28	100	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 3	V_{DD} = 5.0 V	Square wave input		0.20	1.55	mA
						Resonator connection		0.40	1.74	
					V_{DD} = 3.0 V	Square wave input		0.20	1.55	
						Resonator connection		0.40	1.74	
				f_{MX} = 10 MHz Note 3	V_{DD} = 5.0 V	Square wave input		0.15	0.86	
						Resonator connection		0.30	0.93	
					V_{DD} = 3.0 V	Square wave input		0.15	0.86	
						Resonator connection		0.30	0.93	
			LS (low-speed main) mode (MCSEL = 0)	f_{MX} = 8 MHz Note 3	V_{DD} = 3.0 V	Square wave input		68	550	μA
						Resonator connection		125	590	
				f_{MX} = 8 MHz Note 3	V_{DD} = 2.0 V	Square wave input		68	550	
						Resonator connection		125	590	
			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 3	V_{DD} = 3.0 V	Square wave input		23	128	μA
						Resonator connection		65	200	
				f_{MX} = 1 MHz Note 3	V_{DD} = 2.0 V	Square wave input		23	128	
						Resonator connection		65	200	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 3	V_{DD} = 3.0 V	Square wave input		10	64	μA
						Resonator connection		59	150	
				f_{MX} = 1 MHz Note 3	V_{DD} = 2.0 V	Square wave input		10	64	
						Resonator connection		59	150	
			Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 5				0.48	1.22	μA
				f_{IL} = 15 kHz, T_A = +25°C Note 5				0.55	1.22	
				f_{IL} = 15 kHz, T_A = +85°C Note 5				0.80	3.30	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD3} Note 2	STOP mode Note 3	T_A = -40°C		0.19	0.51	μA
			T_A = +25°C		0.25	0.51	
			T_A = +50°C		0.28	1.10	
			T_A = +70°C		0.38	1.90	
			T_A = +85°C		0.60	3.30	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. The values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

Peripheral Functions (Common to all products)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 3, 4	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)			0.02		μA
8-bit interval timer operating current Notes 1, 9	I_{TMT}	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)	8-bit counter mode × 2-channel operation		0.04		μA
			16-bit counter mode operation		0.03		μA
Watchdog timer operating current	I_{WDT} Notes 1, 3, 5	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	During maximum-speed conversion	Normal mode, AV_{VREFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{VREFP} = V_{DD} = 3.0 V		0.5	0.7	mA
Internal reference voltage (1.45 V) current Notes 1, 10	I_{ADREF}				85.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				85.0		μA
D/A converter operating current	I_{DAC} Note 1	Per channel				1.5	mA
PGA operating current	I_{PGA} Notes 1, 2				480	700	μA
Comparator operating current	I_{CMP} Note 8	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Comparator high-speed mode Window mode		12.5		μA
			Comparator low-speed mode Window mode		3.0		
			Comparator high-speed mode Standard mode		6.5		
			Comparator low-speed mode Standard mode		1.9		
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Comparator high-speed mode Window mode		8.0		
			Comparator low-speed mode Window mode		2.2		
			Comparator high-speed mode Standard mode		4.0		
			Comparator low-speed mode Standard mode		1.3		
LVD operating current	I_{LVD} Notes 1, 7				0.10		μA
Self-programming operating current	IFSP Notes 1, 12				2.0	12.20	mA
BGO current	IBGO Notes 1, 11				2.0	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation f_{IH} = 24 MHz, AVREFP = V_{DD} = 3.0 V	Mode transition Note 13		0.50	0.60	mA
			The A/D conversion operations are performed		1.20	1.44	mA
		CSI/UART operation f_{IH} = 24 MHz			0.70	0.84	mA
	ISNOZM Note 1	ADC operation f_{IM} = 4 MHz, AVREFP = V_{DD} = 3.0 V	Mode transition Note 13		0.05	0.08	mA
			The A/D conversion operations are performed		0.67	0.78	mA
		CSI operation, f_{IM} = 4 MHz			0.06	0.08	mA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. Operable range is 2.7 to 5.5 V.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and high-speed system clock are stopped.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

Note 8. Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{CMP} when the comparator circuit is in operation.

Note 9. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 10. Current consumed by generating the internal reference voltage (1.45 V).

Note 11. Current flowing during programming of the data flash.

Note 12. Current flowing during self-programming.

Note 13. For transition time to the SNOOZE mode, see **24.3.3 SNOOZE mode** in the RL78/G11 User's Manual.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V $\leq$ EV_{DD} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V $\leq$ V_{DD} $\leq$ 5.5 V	0.04167		1	μs
				2.4 V $\leq$ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V $\leq$ V_{DD} $\leq$ 5.5 V PMMC. MCSEL = 0	0.125		1	μs
				1.8 V $\leq$ V_{DD} $\leq$ 5.5 V PMMC. MCSEL = 1	0.25		1	
			LP (low-power main) mode	1.8 V $\leq$ V_{DD} $\leq$ 5.5 V		1		μs
			LV (low-voltage main) mode	1.6 V $\leq$ V_{DD} $\leq$ 5.5 V	0.25		1	μs
		Subsystem clock (f_{SUB}) operation	f_{IL}	1.8 V $\leq$ V_{DD} $\leq$ 5.5 V		66.7		μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V $\leq$ V_{DD} $\leq$ 5.5 V	0.04167		1	μs
				2.4 V $\leq$ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V $\leq$ V_{DD} $\leq$ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V $\leq$ V_{DD} $\leq$ 5.5 V	0.25		1	μs
External system clock frequency	f_{EX}	2.7 V $\leq$ V_{DD} $\leq$ 5.5 V			1		20	MHz
		2.4 V $\leq$ V_{DD} < 2.7 V			1		16	MHz
		1.8 V $\leq$ V_{DD} < 2.4 V			1		8	MHz
		1.6 V $\leq$ V_{DD} < 1.8 V			1		4	MHz
External system clock input high-/low-level width	t_{EXH}, t_{EXL}	2.7 V $\leq$ V_{DD} $\leq$ 5.5 V			24			ns
		2.4 V $\leq$ V_{DD} < 2.7 V			30			ns
		1.8 V $\leq$ V_{DD} < 2.4 V			60			ns
		1.6 V $\leq$ V_{DD} < 1.8 V			120			ns
TI00 to TI03 input high-/low-level width	t_{TIH}, t_{TIL} Note				$1/f_{MCK}$ + 10			ns

Note Following conditions must be satisfied on low level interface of EV_{DD} < V_{DD}.
1.8 V $\leq$ EV_{DD} $\leq$ 2.7 V: MIN. 125 ns
1.6 V $\leq$ EV_{DD} < 1.8 V: MIN. 250 ns

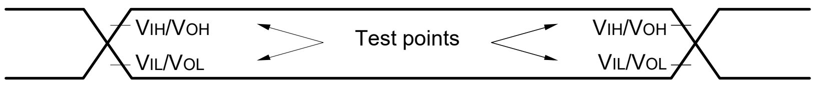
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

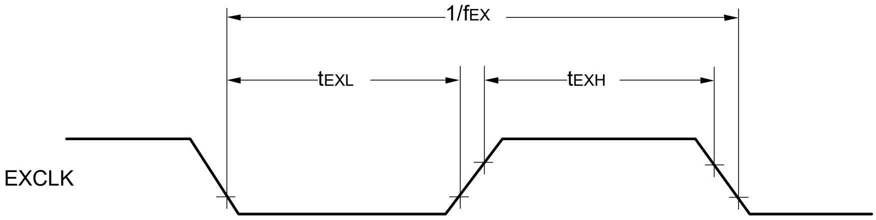
	Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
<R>	TO00 to TO03, TKBO0, and TKBO1 output frequency Note	f_{TO}	TO00 to TO03, TKBO0, and TKBO1 (in the case of output from port pins other than P20)	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V			12	MHz
					2.7 V ≤ EV_{DD} < 4.0 V			8	
					1.8 V ≤ EV_{DD} < 2.7 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
				LS (low-speed main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
				LP (low-power main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V			0.5	
				LV (low-voltage main) mode	1.6 V ≤ EV_{DD} ≤ 5.5 V			2	
			TKBO1 (in the case of output from P20)	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	MHz
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
				LS (low-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
					1.8 V ≤ V_{DD} < 2.4 V			0.75	
				LP (low-power main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V			0.5	
				LV (low-voltage main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
					1.8 V ≤ V_{DD} < 2.4 V			0.75	
					1.6 V ≤ V_{DD} < 1.8 V			0.5	
	PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
					2.7 V ≤ EV_{DD} < 4.0 V			8	
					1.8 V ≤ EV_{DD} < 2.7 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
			LS (low-speed main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
			LP (low-power main) mode		1.6 V ≤ EV_{DD} ≤ 5.5 V			1	
			LV (low-voltage main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
<R>	Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2, INTP9		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
			INTP3 to INTP8, INTP10, INTP11		1.6 V ≤ EV_{DD} ≤ 5.5 V	1			
	Key interrupt input low-level width	t_{KR}	KR0 to KR7		1.8 V ≤ EV_{DD} ≤ 5.5 V	250			ns
					1.6 V ≤ EV_{DD} < 1.8 V	1			μs
	$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Note When duty is 50%.

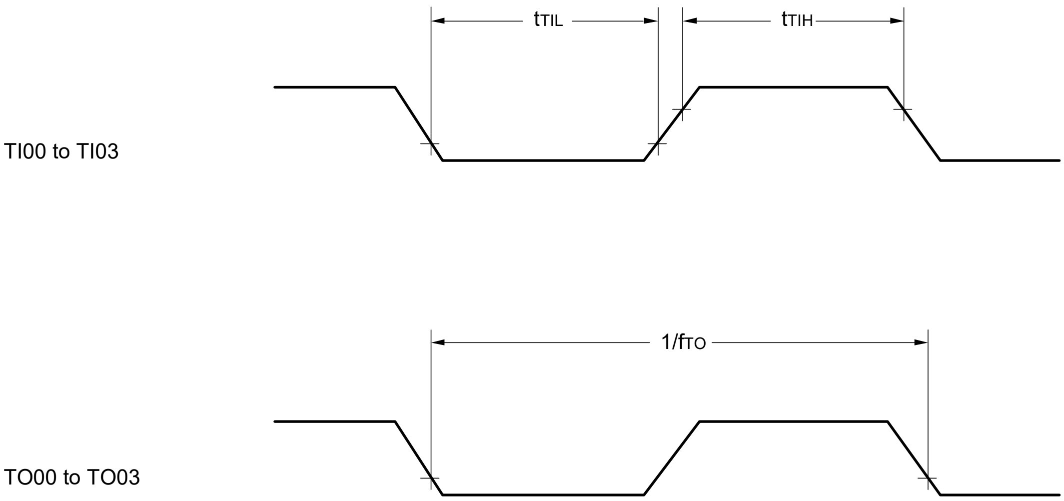
AC Timing Test Points



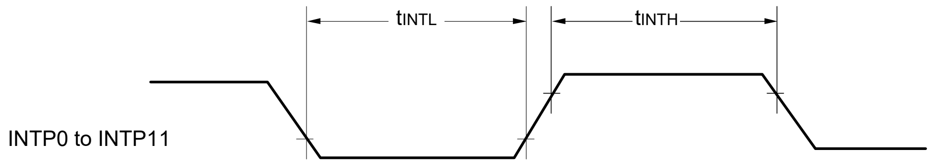
External System Clock Timing



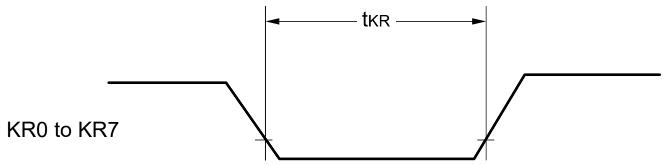
TI/TO Timing



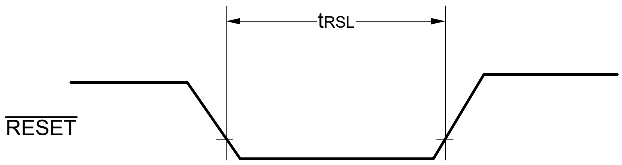
Interrupt Request Input Timing



Key Interrupt Input Timing

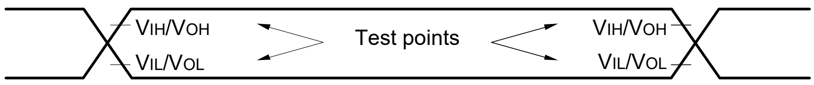


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as TxDq pins

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1, 2		2.7 V ≤ EV_{DD} ≤ 5.5V			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps
		1.8 V ≤ EV_{DD} ≤ 5.5 V			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps
		1.7 V ≤ EV_{DD} ≤ 5.5 V			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—			$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3	—			1.3		0.1		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. Following conditions must be satisfied on low level interface of EV_{DD} < V_{DD}.
2.4 V ≤ EV_{DD} ≤ 2.7 V: MAX.2.6 Mbps
1.8 V ≤ EV_{DD} ≤ 2.4 V: MAX.1.3 Mbps
1.6 V ≤ EV_{DD} ≤ 1.8 V: MAX.0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ EV_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ EV_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ EV_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ EV_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ EV_{DD} ≤ 5.5 V)

Caution **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

When P20 is used as TxD1 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	LS (low-speed main) Mode MIN.	LS (low-speed main) Mode MAX.	LP (Low-power main) mode MIN.	LP (Low-power main) mode MAX.	LV (low-voltage main) Mode MIN.	LV (low-voltage main) Mode MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.5		1.3		0.1		0.6	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.2		1.2		0.1		0.6	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.0		1.0		0.1		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		Using prohibited		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		Using prohibited		0.6		0.1		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V		Using prohibited		Using prohibited		Using prohibited		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		Using prohibited		Using prohibited		Using prohibited		0.5	Mbps
		1.6 V ≤ V_{DD} ≤ 5.5 V		Using prohibited		Using prohibited		Using prohibited		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		Using prohibited		Using prohibited		Using prohibited		0.5	Mbps

Note 1. f_{MCK} is a frequency selected by setting the CKS bit in the SPS and SMR registers.

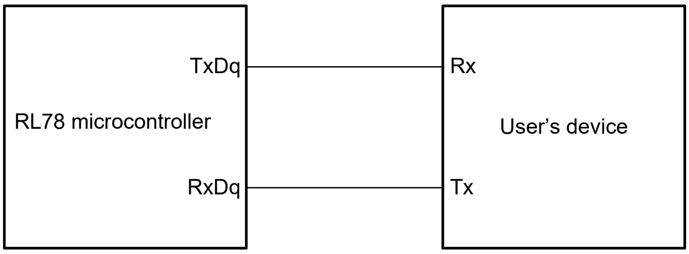
Note 2. The transfer rate of 4800 bps is only supported in the SNOOZE mode.
Note that the SNOOZE mode is not supported when fHOCO is 48 MHz.

Note 3. f_{CLK} in each operating mode is as follows.:

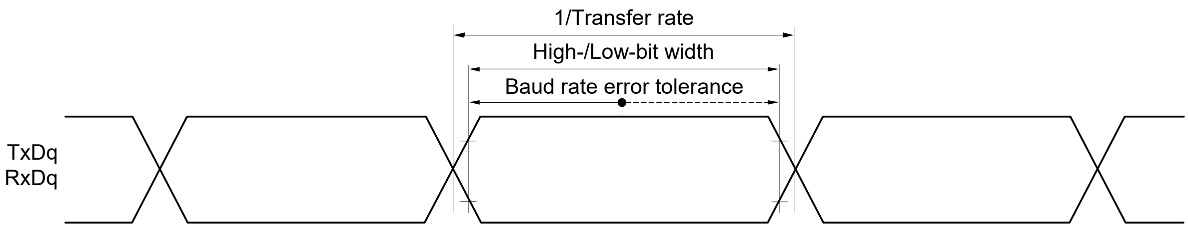
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK}	83.3		250		2000		500		ns
SCKp high-/low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 - 7		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	t_{KCY1}/2 - 10								ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V	23		110		110		110		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V	33								ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		10		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4		10		20		20		20	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

When P01, P32, P53, P54 and P56 are used as SOmn pins
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	LS (low-speed main) Mode MIN.	LS (low-speed main) Mode MAX.	LP (Low-power main) mode MIN.	LP (Low-power main) mode MAX.	LV (low-voltage main) Mode MIN.	LV (low-voltage main) Mode MAX.	Unit
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ EV_{DD} ≤ 5.5 V	167		500		4000		1000		ns
			2.4 V ≤ EV_{DD} ≤ 5.5 V	250								
			1.8 V ≤ EV_{DD} ≤ 5.5 V	500								
			1.7 V ≤ EV_{DD} ≤ 5.5 V	1000		1000						
			1.6 V ≤ EV_{DD} ≤ 5.5 V	Using prohibited								
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2- 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2- 18								
		2.4 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2- 38								
		1.8 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2- 50								
		1.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2- 100		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		
		1.6 V ≤ EV_{DD} ≤ 5.5 V		Using prohibited								
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		44		110		110		110		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V										
		2.4 V ≤ EV_{DD} ≤ 5.5 V		75								
		1.8 V ≤ EV_{DD} ≤ 5.5 V		110								
		1.7 V ≤ EV_{DD} ≤ 5.5 V		220		220		220		220		
		1.6 V ≤ EV_{DD} ≤ 5.5 V		Using prohibited								
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	1.7 V ≤ EV_{DD} ≤ 5.5 V		19		19		19		19		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V		Using prohibited								
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	1.7 V ≤ EV_{DD} ≤ 5.5 V		33.4		33.4		33.4		33.4	ns
			1.6 V ≤ EV_{DD} ≤ 5.5 V		Using prohibited							

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS MAX.	LS (low-speed main) Mode MIN.	LS MAX.	LP (Low-power main) mode MIN.	LP MAX.	LV (low-voltage main) Mode MIN.	LV MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	600		600		4000		1000		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	850		850						
			2.4 V ≤ V_{DD} ≤ 5.5 V	1000		1000						
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		1500				1500		
			1.7 V ≤ V_{DD} ≤ 5.5 V	—		—		—		2000		
			1.6 V ≤ V_{DD} ≤ 5.5 V	—		—		—				
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 12$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 18$								
		2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 38$								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		$t_{KCY1}/2 - 100$		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V										
		2.4 V ≤ V_{DD} ≤ 5.5 V		75								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		220		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.4 V ≤ V_{DD} ≤ 5.5 V		150		250		250		300	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—							
			1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

When P01, P32, P53, P54 and P56 are used as SOmn pins
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 3	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	8/f_{MCK}		—		—		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		2.7 V ≤ EV_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}		—		—		—	—	
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		2.4 V ≤ EV_{DD} ≤ 5.5 V		6/f_{MCK} and 500								
		1.8 V ≤ EV_{DD} ≤ 5.5 V		6/f_{MCK} and 750								
		1.7 V ≤ EV_{DD} ≤ 5.5V		6/f_{MCK} and 1500		6/f_{MCK} and 1500						
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—								
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		
		1.8 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		
		1.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—								
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		
		1.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 40		1/f_{MCK} + 40		1/f_{MCK} + 40		1/f_{MCK} + 40		
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—								
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	1.8 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 250		1/f_{MCK} + 250		1/f_{MCK} + 250		1/f_{MCK} + 250		
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—								

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output Note 1	t_{KSO2}	C = 30 pF Note 2	2.7 V ≤ EV_{DD} ≤ 5.5 V		$2/f_{MCK}$ + 44		$2/f_{MCK}$ + 110		$2/f_{MCK}$ + 110		$2/f_{MCK}$ + 110	ns
			2.4 V ≤ EV_{DD} ≤ 5.5 V		$2/f_{MCK}$ + 75							
			1.8 V ≤ EV_{DD} ≤ 5.5 V		$2/f_{MCK}$ + 110							
			1.7 V ≤ EV_{DD} ≤ 5.5 V		$2/f_{MCK}$ + 220		$2/f_{MCK}$ + 220		$2/f_{MCK}$ + 220		$2/f_{MCK}$ + 220	
			1.6 V ≤ EV_{DD} ≤ 5.5 V									
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ EV_{DD} ≤ 5.5 V	120		120		120		120		ns
			1.8 V ≤ EV_{DD} < 2.7 V	200		200		200		200		
			1.7 V ≤ EV_{DD} < 1.8 V	400		400		400		400		
			1.6 V ≤ EV_{DD} < 1.7 V	—								
		DAPmn = 1	2.7 V ≤ EV_{DD} ≤ 5.5 V	$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		ns
			1.8 V ≤ EV_{DD} < 2.7 V	$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		
			1.7 V ≤ EV_{DD} < 1.8 V	$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		
			1.6 V ≤ EV_{DD} < 1.7 V	—								
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ EV_{DD} ≤ 5.5 V	$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		$1/f_{MCK}$ + 120		ns
			1.8 V ≤ EV_{DD} < 2.7 V	$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		$1/f_{MCK}$ + 200		
			1.7 V ≤ EV_{DD} < 1.8 V	$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		$1/f_{MCK}$ + 400		
			1.6 V ≤ EV_{DD} < 1.7 V	—								
		DAPmn = 1	2.7 V ≤ EV_{DD} ≤ 5.5 V	120		120		120		120		ns
			1.8 V ≤ EV_{DD} < 2.7 V	200		200		200		200		
			1.7 V ≤ EV_{DD} < 1.8 V	400		400		400		400		
			1.6 V ≤ EV_{DD} < 1.7 V	—								

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. C is the load capacitance of the SOp output lines.

Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	14/f_{MCK}		—		—		—		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	14/f_{MCK} and 850		—		—		—		
			f_{MCK} ≤ 16 MHz	12/f_{MCK} and 850		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		2.4 V ≤ V_{DD} ≤ 5.5 V		12/f_{MCK} and 1000		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		1.7 V ≤ V_{DD} ≤ 5.5V		—		—		—		12/f_{MCK}		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		t_{KCY2}/2 - 66		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		1/f_{MCK} + 40		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.5 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		1/f_{MCK} + 250		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 160		2/f_{MCK} + 260		2/f_{MCK} + 260		2/f_{MCK} + 260	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 190							
			1.8 V ≤ V_{DD} ≤ 5.5 V		—							
			1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		2/f_{MCK} + 320	
			1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

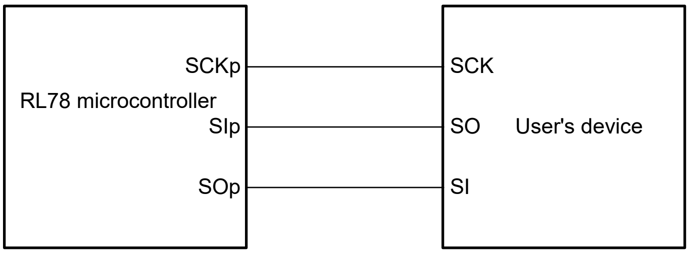
Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

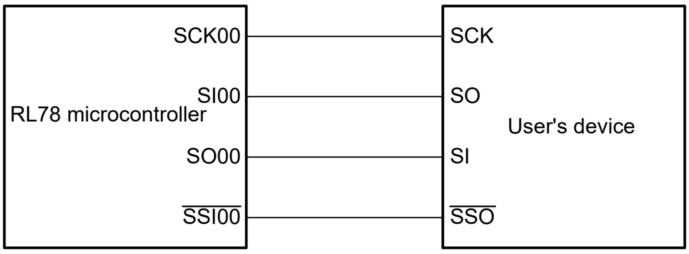
Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

CSI mode connection diagram (during communication at same potential)

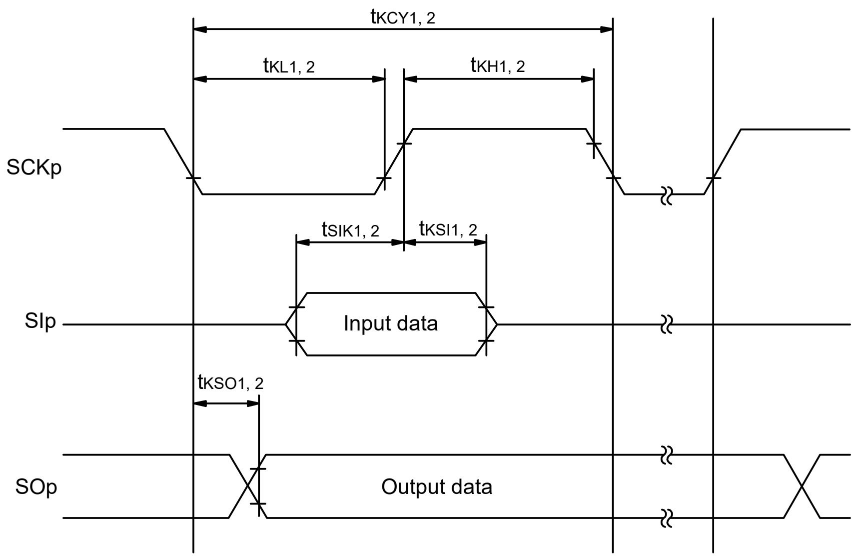


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

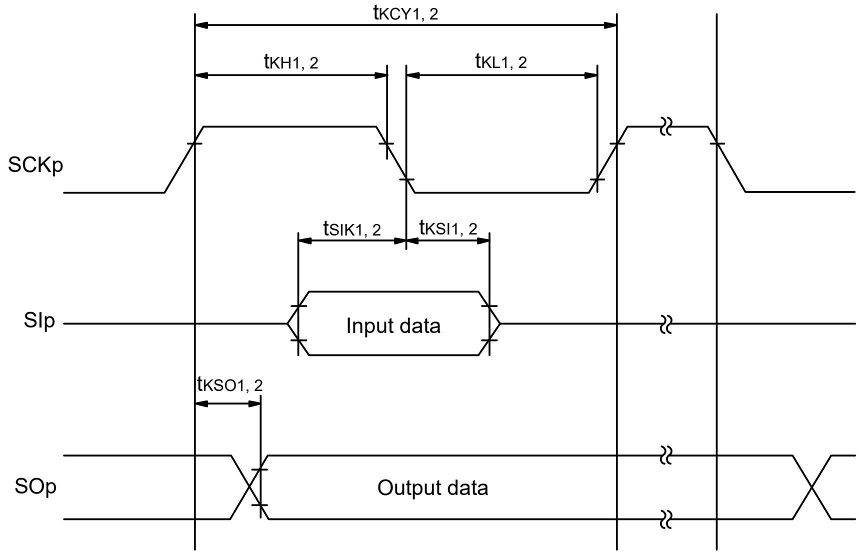


Remark p: CSI number (p = 00, 01, 10 and 11)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(5) During communication at same potential (simplified I^{2}C mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

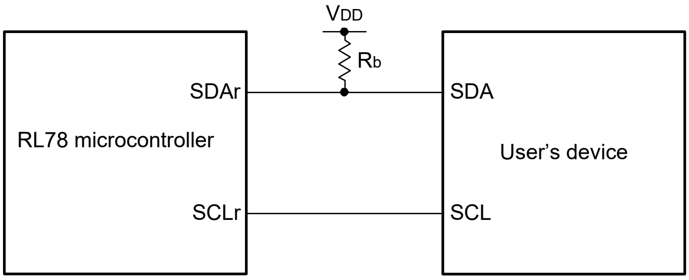
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1							
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1		250 Note 1	
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—							
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 85 Note 2		$1/f_{MCK}$ + 145 Note 2		$1/f_{MCK}$ + 145 Note 2		$1/f_{MCK}$ + 145 Note 2		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 Note 2								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 230 Note 2		$1/f_{MCK}$ + 230 Note 2		$1/f_{MCK}$ + 230 Note 2		$1/f_{MCK}$ + 230 Note 2		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 290 Note 2		$1/f_{MCK}$ + 290 Note 2		$1/f_{MCK}$ + 290 Note 2		$1/f_{MCK}$ + 290 Note 2		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		355		355		355		355	
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		405		405		405		405	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ									
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—							

Note 1. The value must be equal to or less than $f_{MCK}/4$.

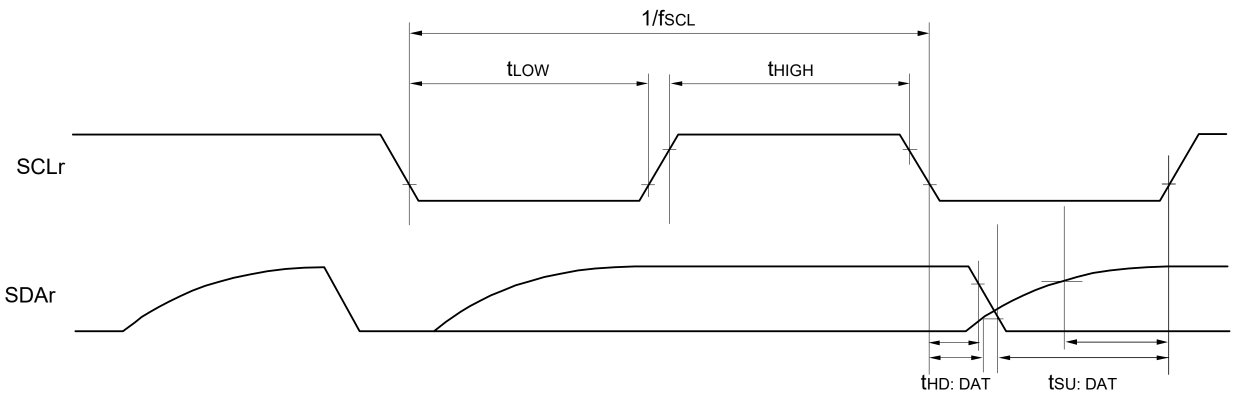
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution **Select the normal input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 3), mn = 00 to 03)

(6) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (UART mode) (dedicated baud rate generator output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/6$ Notes 1, 2, 4		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3		0.1		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with EV_{DD} ≥ Vb.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Note 4. The following conditions are required for low voltage interface when EV_{DD} < V_{DD}
2.4 V ≤ EV_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ EV_{DD} < 2.4 V: MAX. 1.3 Mbps

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			Note 1		Note 1		Note 1		Note 1	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			Note 3		Note 3		Note 3		Note 3	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			Notes 5, 6		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with EV_{DD} ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

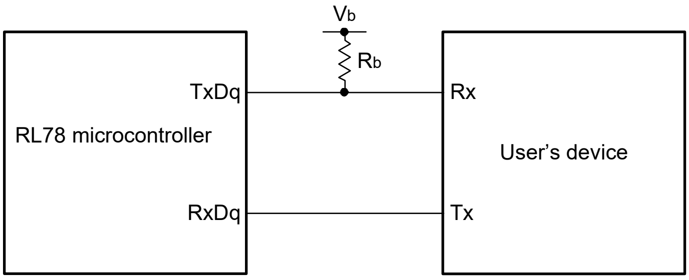
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

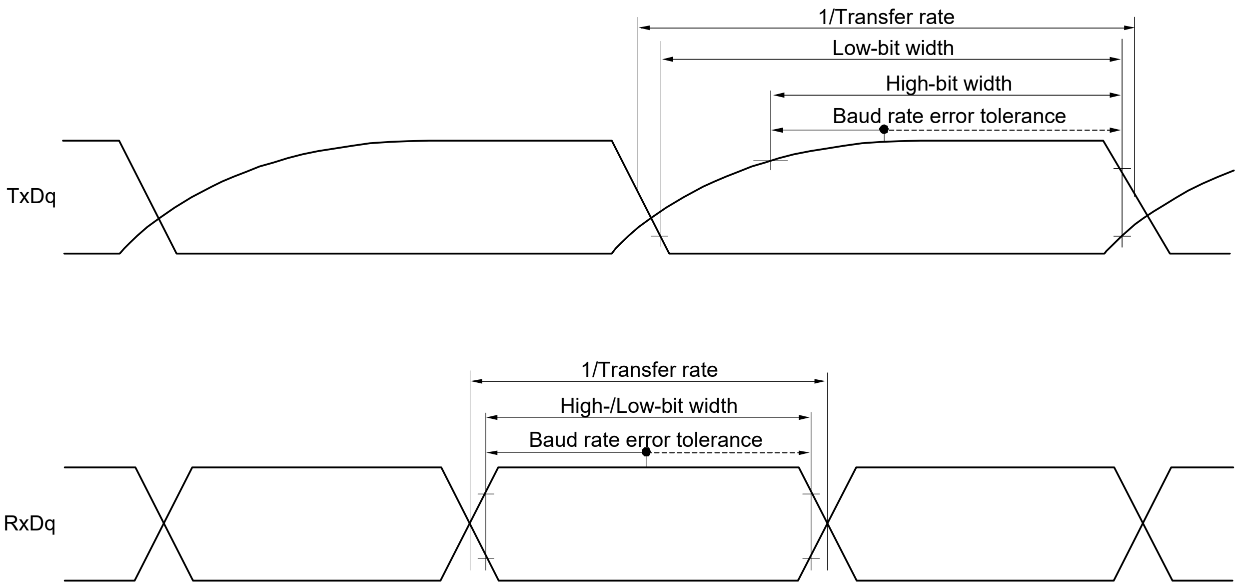
Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V $\le$ EV_{DD} = V_{DD} $\le$ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \ge 2/f_{CLK}$	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$	200		1150		1150		1150		ns
		$t_{KCY1} \ge 2/f_{CLK}$	$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$	300								ns
SCKp high-level width	t_{KH1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCKp low-level width	t_{KL1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$		$t_{KCY1}/2 - 10$								
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		58		479		479		479		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$		121								
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		10		10		10		10		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$										
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$			60		60		60		60	ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$			130		130		130		130	
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		23		110		110		110		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$		33								
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 20\ pF$, $R_b = 1.4\ k\Omega$		10		10		10		10		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 20\ pF$, $R_b = 2.7\ k\Omega$										

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		10	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ									

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 5)
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $4/f_{CLK}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		1150		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500								ns
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ	1150								ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 12		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 18								
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 50								ns

Note Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

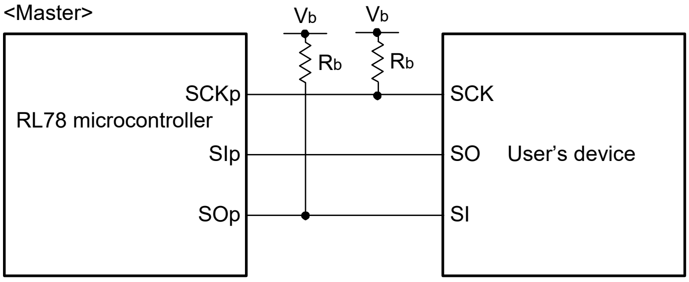
Parameter	Symbol	Conditions	HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	LS (low-speed main) Mode MIN.	LS (low-speed main) Mode MAX.	LP (Low-power main) mode MIN.	LP (Low-power main) mode MAX.	LV (low-voltage main) Mode MIN.	LV (low-voltage main) Mode MAX.	Unit
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		479		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ	177								
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ	479								
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100		100	ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195		195	ns
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		110		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110								
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25		25	ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
Note 3. Use it with $EV_{DD} \ge V_b$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

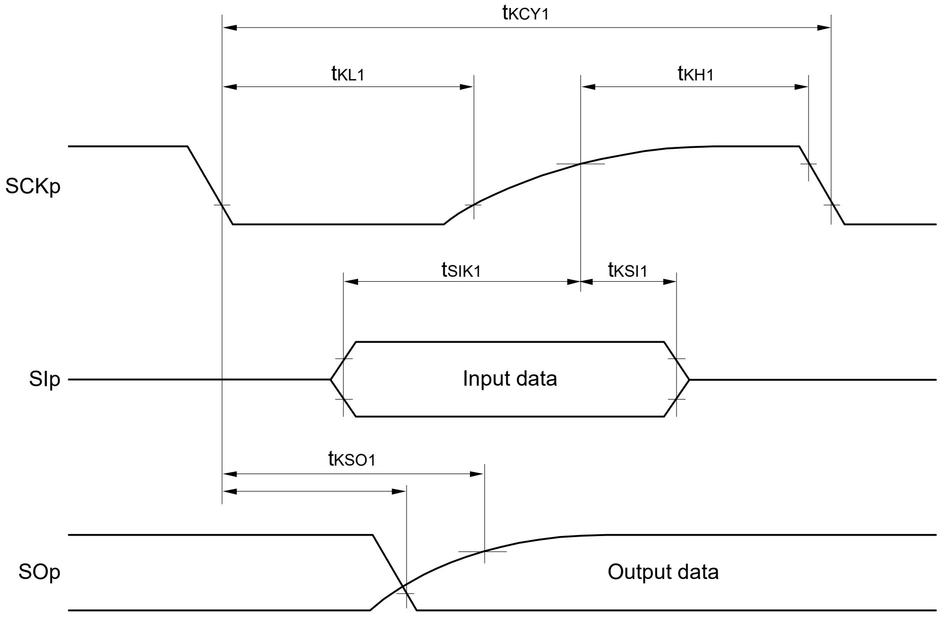


Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

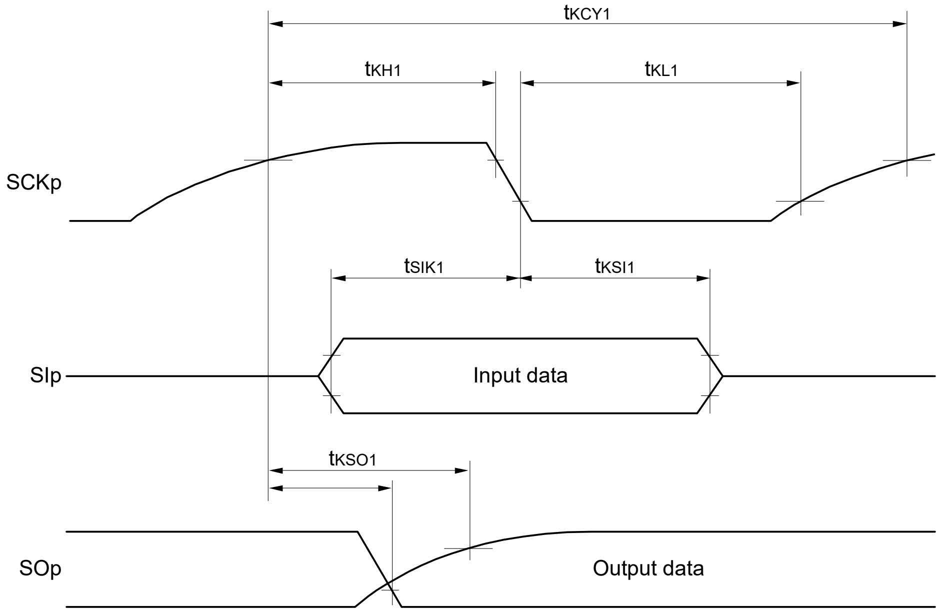
Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(9) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to 85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	LS (low-speed main) Mode MIN.	LS (low-speed main) Mode MAX.	LP (Low-power main) mode MIN.	LP (Low-power main) mode MAX.	LV (low-voltage main) Mode MIN.	LV (low-voltage main) Mode MAX.	Unit
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 2.7 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Notes, Caution** and **Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

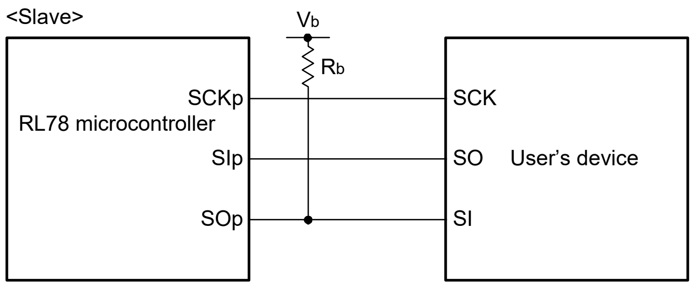
Note 2. Use it with $EV_{DD} \geq V_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

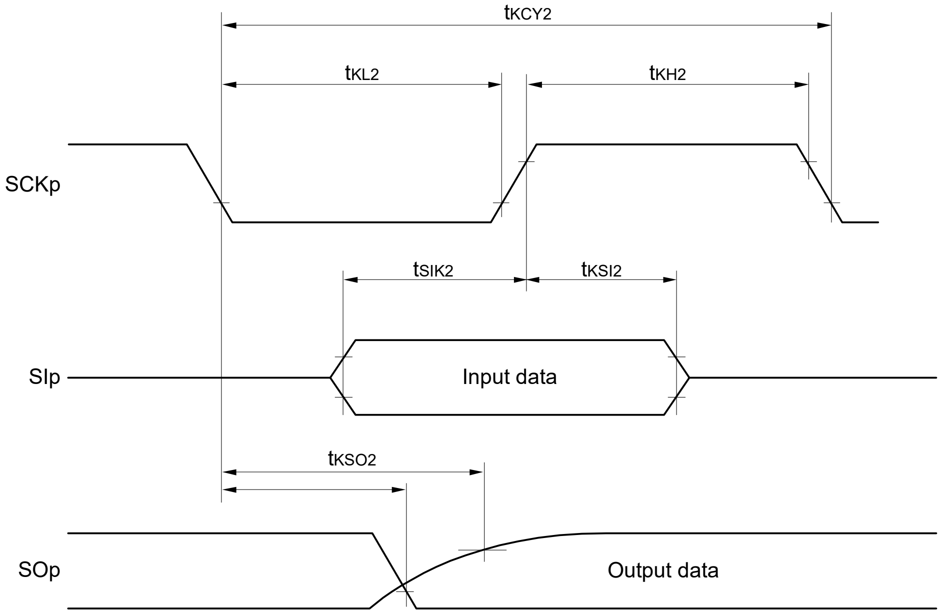


Remark 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

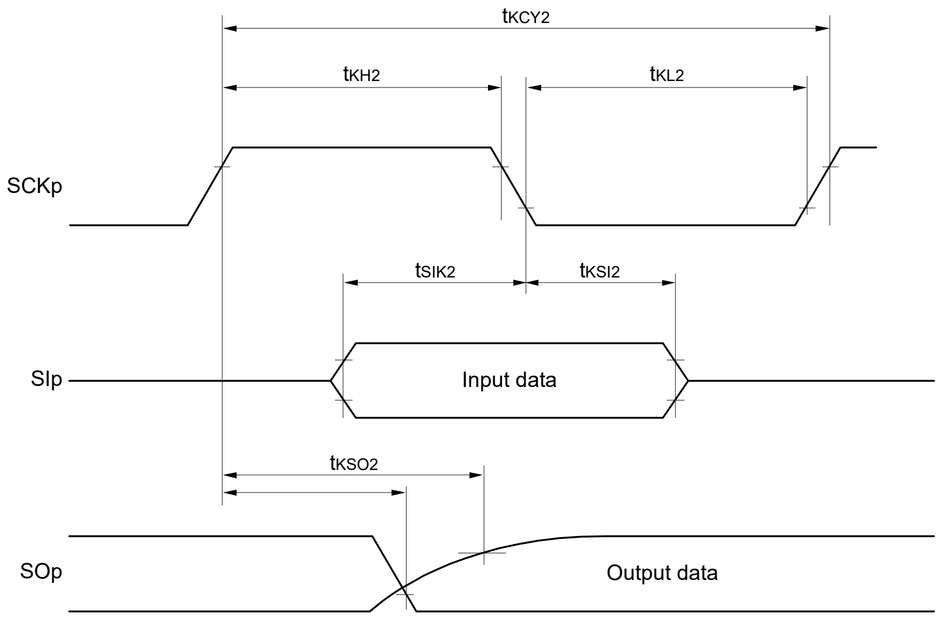
Remark 2. p: CSI number (p = 00 to 03), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(10) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (simplified I²C mode)

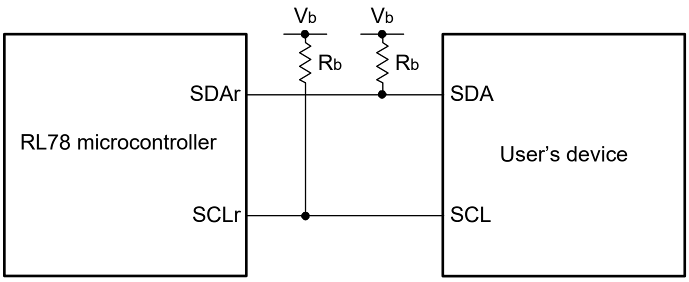
(T_A = -40 to 85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		1550		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		1550		1550		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		1550		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		1550		ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		610		610		610		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		610		610		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		610		610		610		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		610		610		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		610		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 2		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 3		$1/f_{MCK}$ + 190 Note 2		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
		1.8 V ≤ EV_{DD} < 4.0 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		$1/f_{MCK}$ + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ EV_{DD} < 4.0V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	0	355	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

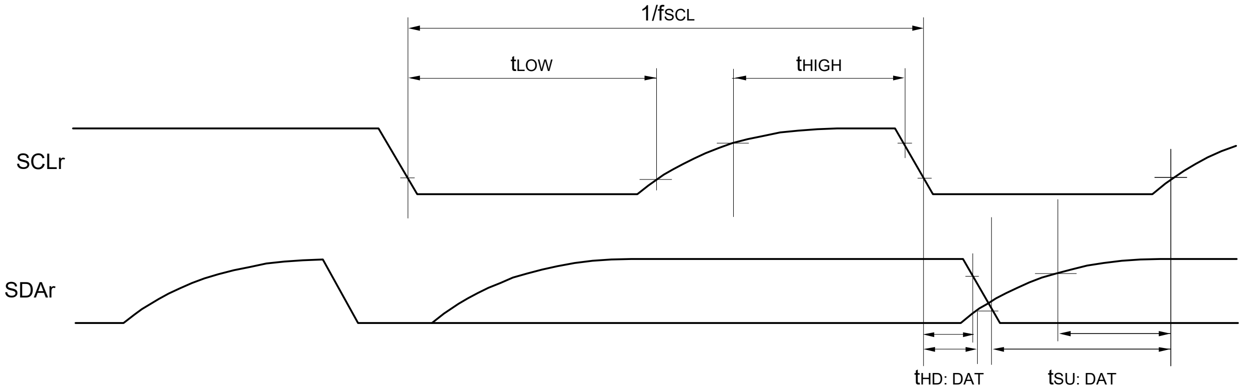
Note 1. The value must be equal to or less than $f_{MCK}/4$.
Note 2. Use it with $EV_{DD} \geq V_b$.
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Simplified I2C mode connection diagram (during communication at different potential)



Simplified I2C mode serial transfer timing (during communication at different potential)



Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 3), mn = 00 to 03)

2.5.2 Serial interface IICA

(1) I²C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.8 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.6 V ≤ EV_{DD} ≤ 5.5 V	—		0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		250		250		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		0	3.45	0	3.45	0	3.45	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		μs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^{2}C fast mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:\ STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
Hold time Note 1	$t_{HD:\ STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:\ DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		100		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		100		ns
Data hold time (transmission) Note 2	$t_{HD:\ DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:\ STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:\ DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	1000	—		—		—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		—		—		—		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		50		—		—		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.45	—		—		—		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		—		—		—		μs

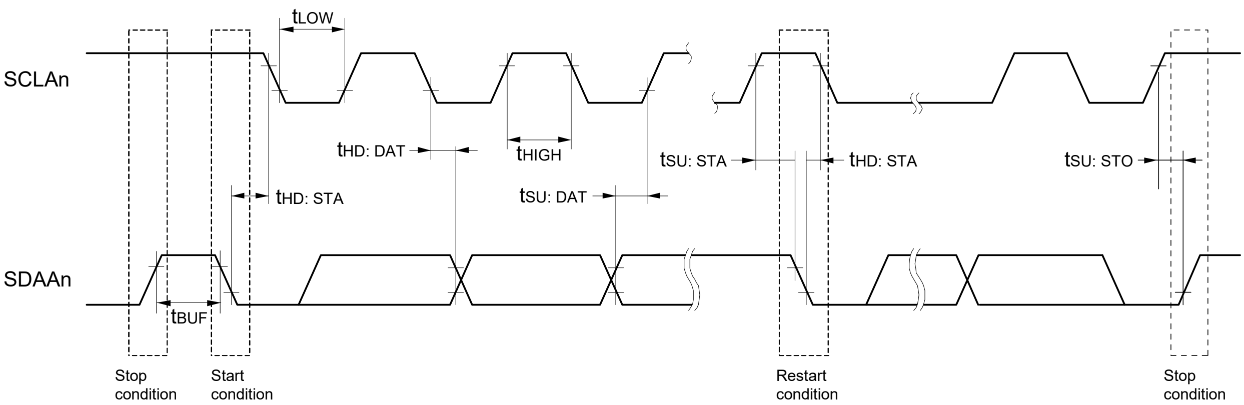
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-)= AV_{REFM}
ANI0 to ANI3	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI22	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 and ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±2.0	LSB
Analog input voltage	V_{AIN}	ANI2 and ANI3		0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 5. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(2) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EVDD ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5		1.2	±8.5	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	μs
			1.6 V ≤ VDD ≤ 5.5 V	57		95	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution EVDD ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution EVDD ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EVDD ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution EVDD ≤ AVREFP = VDD Notes 3, 4	1.8 V ≤ AVREFP ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AVREFP ≤ 5.5 V Note 5			±2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI22		0		AVREFP and EVDD	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EVDD ≤ AVREFP ≤ VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. When AVREFP < EVDD ≤ VDD, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AVREFP = VDD.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3		0		V_{DD}	V
		ANI16 to ANI22		0		EV_{DD}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 4			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).
Note 4. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 and ANI3, ANI16 to ANI22

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} ≤ V_{DD}, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	t_{CONV}		17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}				±0.60	% FSR
Integral linearity error Note 1	ILE				±2.0	LSB
Differential linearity error Note 1	DLE				±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 5.5 V	5			μs
		1.8 V ≤ V_{DD} < 2.4 V	10			μs

2.6.3 D/A converter characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{SS} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs
			1.6 V ≤ V_{DD} < 2.7 V			6	μs

2.6.4 Comparator

(Comparator 0: T_A = -40 to +85°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)
(Comparator 1: T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	V_{IREF0}	IVREF0 pin		0		V_{DD} - 1.4 Note 1	V
	V_{IREF1}	IVREF1 pin		1.4 Note 1		V_{DD}	V
	V_{ICMP}	IVCMP0 pin		-0.3		V_{DD} + 0.3	V
		IVCMP1 pin		-0.3		EV_{DD} + 0.3	V
Output delay	td	V_{DD} = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			1.5	μs
			Comparator low-speed mode, standard mode		3		μs
			Comparator low-speed mode, window mode		4		μs
Operation stabilization wait time	t_{CMP}			100			μs
Reference voltage declination in channel 0 of internal DAC Note 2	⊿VIDAC					± 2.5	LSB

Note 1. In window mode, make sure that V_{REF1} - V_{REF0} ≥ 0.2 V.

Note 2. Only in CMP0

2.6.5 PGA

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9 × V_{DD}/Gain	V
Output voltage range	V_{IOHPGA}			0.93 × V_{DD}			V
	V_{IOLPGA}					0.07 × V_{DD}	V
Gain error		x4, x8				±1	%
		x16				±1.5	%
		x32				±2	%
Slew rate	SR_{RPGA}	Rising When V_{IN} = 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/µs
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling When V_{IN}= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
Reference voltage stabilization wait time[Note]	t_{PGA}	x4, x8				5	µs
		x16, x32				10	µs

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

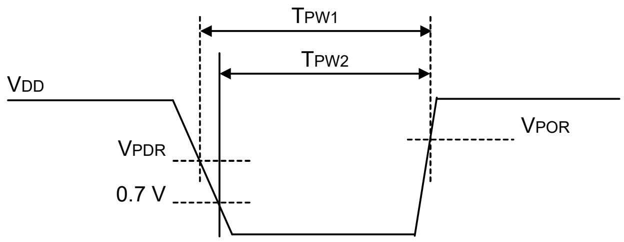
2.6.6 POR circuit characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW1}	Other than STOP/SUB HALT/SUB RUN	300			μs
	T_{PW2}	STOP/SUB HALT/SUB RUN	300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \le EV_{DD} \le V_{DD} \le$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVDA1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVDB1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

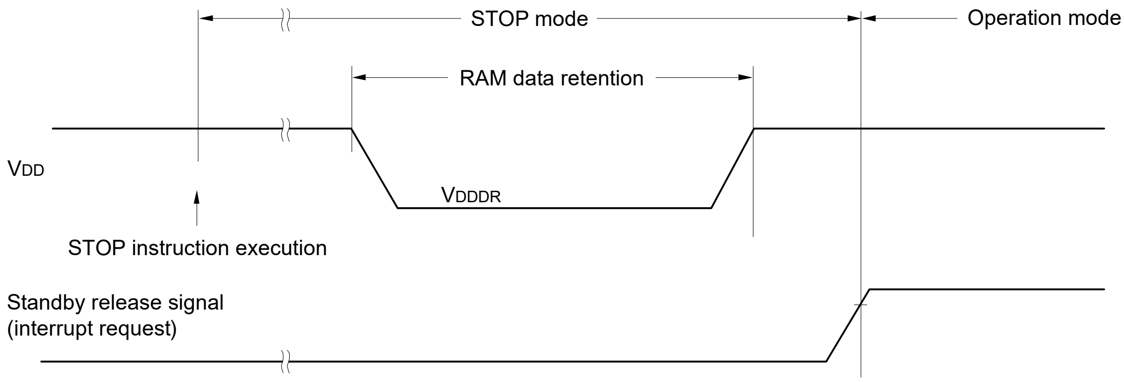
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK			1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	TA = 25°C		1,000,000		
		Retained for 5 years	TA = 85°C	100,000			
		Retained for 20 years	TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
Note 2. When using flash memory programmer and Renesas Electronics self-programming library
Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified Note 1	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends Note 1	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) Notes 1, 2	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

Note 1. Deassertion of the POR and LVD reset signals must precede deassertion of the pin reset signal.
Note 2. This excludes the flash firmware processing time (723 μs).

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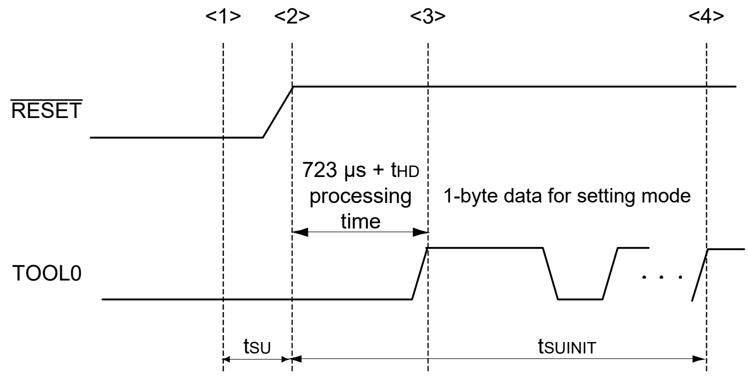


<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (T_A = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications (T_A = −40 to +105°C)
R5F105xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G11 User's Manual.

Caution 3. Please contact Renesas Electronics sales office for derating of operation under T_A = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Caution 4. When operating temperature exceeds 85°C, only HS (high-speed main) mode can be used as the flash operation mode. Regulator mode should be used with the normal setting (MCSEL = 0).

Caution 5. The EV_{DD} pin is not present on products with 24 or less pins. Accordingly, replace EV_{DD} with V_{DD} and the voltage condition 1.6 ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V with 1.6 ≤ V_{DD} ≤ 5.5 V.

Remark When the products "G: Industrial applications" is used in the range of T_A = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)**.

Fields of application	A: Consumer applications	G: Industrial applications
Operating ambient temperature	T_A = −40 to +85°C	T_A = −40 to +105°C
Operating mode Operating Voltage Range	HS (High-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz LS (Low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz LV (Low-voltage main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 4 MHz	Only in HS (High-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
High-speed on-chip oscillator clock to an accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V: ±1.0% @ T_A = -20 to +85°C ±1.5% @ T_A = -40 to -20°C 1.6 V ≤ V_{DD} < 1.8 V: ±5.0% @ T_A = -20 to +85°C ±5.5% @ T_A = -40 to -20°C	2.4 V ≤ V_{DD} ≤ 5.5 V: ±2.0% @ T_A = +85 to +105°C ±1.0% @ T_A = -20 to +85°C ±1.5% @ T_A = -40 to -20°C
Serial array unit	UART CSI: f_{CLK}/2 (12 Mbps are supported), f_{CLK}/4 Simplified I^2C	UART CSI: f_{CLK}/4 Simplified I^2C
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fast mode
Voltage Detector	• Rising: 1.67 V to 4.06 V (14 levels) • Falling: 1.63 V to 3.98 V (14 levels)	• Rising: 2.61 V to 4.06 V (8 levels) • Falling: 2.55 V to 3.98 V (8 levels)

Remark The electrical characteristics for "G: Industrial applications" differ from those for "A: Consumer applications" when the product is in use in an ambient temperature over 85°C. For details, see **3.1** to **3.10** in the following pages.

3.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, EV_{DD}	$V_{DD} \leq EV_{DD}$	-0.5 to + 6.5	V
	AV_{REFP}		0.3 to V_{DD} + 0.3 Note 2	V
	AV_{REFM}		-0.3 to V_{DD} + 0.3 Note 2 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to + 2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P20 to P23, P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P23	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI22	-0.3 to EV_{DD} + 0.3 and -0.3 to $AV_{REF}(+)$ + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI3	-0.3 to V_{DD} + 0.3 and -0.3 to $AV_{REF}(+)$ + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00, P01, P30 to P33, P40, P51 to P56	-40	mA
		Total of all pins -170 mA	P00, P01, P40	-70	mA
			P30 to P33, P51 to P56	-100	mA
	I_{OH2}	Per pin	P20 to P23	-0.5	mA
		Total of all pins		-2	mA
Output current, low	I_{OL1}	Per pin	P00, P01, P30 to P33, P40, P51 to P56	40	mA
		Total of all pins 170 mA	P00, P01, P40	70	mA
			P30 to P33, P51 to P56	100	mA
	I_{OL2}	Per pin	P20 to P23	1	mA
		Total of all pins		4	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1 characteristics

<R> **(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **3.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

3.2.2 On-chip oscillator characteristics

<R> **(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V	1		24	MHz
		2.4 V ≤ V_{DD} ≤ 5.5 V	1		16	
High-speed on-chip oscillator clock frequency accuracy		T_A = +85°C to +105°C	-2		2	%
		T_A = -20°C to +85°C	-1		1	%
		T_A = -40°C to -20°C	-1.5		1.5	%
Middle-speed on-chip oscillator oscillation frequency Note 2	f_{IM}		1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy			-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMT}			0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMV}	T_A = 25°C		0.02		%/V
Low-speed on-chip oscillator clock frequency Note 2	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **3.4 AC Characteristics** for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				-3.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-12.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-10.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-5.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-19.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-42.5	mA
	I_{OH2}	Per pin for P20 to P23				-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-0.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OH} = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				8.5 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-36.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			9.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				76.0	mA
	I_{OL2}	Per pin for P20 to P23				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			1.6	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(3/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0.8 EV_{DD}		EV_{DD}	V
	V_{IH2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P23 (digital input)		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0		0.2 EV_{DD}	V
	V_{IL2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IH3}	P20 to P23 (digital input)		0		0.3 V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution **The maximum value of V_{IH} of pins P00, P01, P20, P30 to P33, P40 and P51 to P56 is V_{DD} or EV_{DD}, even in the N-ch open-drain mode.**
(P20: V_{DD}
P00, P01, P30 to P33, P40, P51 to P56: EV_{DD})

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	EV_{DD} - 0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	EV_{DD} - 0.6			V
			2.4 V ≤ EV_{DD} ≤ 5.5 V I_{OH} = -1.5 mA	EV_{DD} - 0.5			V
	V_{OH2}	P20 to P23	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 400 μA			0.4	V

Caution **P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P23, P125, P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122, X1, X2, EXCLK	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P20 to P23, P125, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				-1	μA
	I_{LIL3}	P121, P122, X1, X2, EXCLK	$V_I = V_{SS}$	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00, P01, P30 to P33, P40, P51 to P56, P125	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.7		mA
						V_{DD} = 3.0 V			1.7		
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.4		
						V_{DD} = 3.0 V			1.4		
			Normal operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.5	7.3	mA
						V_{DD} = 3.0 V			3.5	7.3	
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.2	6.7	
						V_{DD} = 3.0 V			3.2	6.7	
					f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V			2.4	4.9	
						V_{DD} = 3.0 V			2.4	4.9	
			Normal operation	HS (high-speed main) mode	f_{MX} = 20 MHz Note 2	V_{DD} = 5.0 V	Square wave input		2.7	5.7	mA
							Resonator connection		2.8	5.8	
						V_{DD} = 3.0 V	Square wave input		2.7	5.7	
							Resonator connection		2.8	5.8	
					f_{MX} = 10 MHz Note 2	V_{DD} = 5.0 V	Square wave input		1.8	3.4	
							Resonator connection		1.9	3.5	
						V_{DD} = 3.0 V	Square wave input		1.8	3.4	
							Resonator connection		1.9	3.5	
			Normal operation	Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 4				1.8	5.9	μA
					f_{IL} = 15 kHz, T_A = +25°C Note 4				1.9	5.9	
					f_{IL} = 15 kHz, T_A = +85°C Note 4				2.3	8.7	
					f_{IL} = 15 kHz, T_A = +105°C Note 4				3.0	20.9	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)
Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)
Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency
Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)
Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3 f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V			0.59	3.45	mA
					V_{DD} = 3.0 V			0.59	3.45	
				f_{HOCO} = 24 MHz Note 3 f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V			0.41	2.85	
					V_{DD} = 3.0 V			0.41	2.85	
				f_{HOCO} = 16 MHz Note 3 f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V			0.39	2.08	
					V_{DD} = 3.0 V			0.39	2.08	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 3	V_{DD} = 5.0 V	Square wave input		0.20	2.45	mA
						Resonator connection		0.40	2.57	
					V_{DD} = 3.0 V	Square wave input		0.20	2.45	
						Resonator connection		0.40	2.57	
				f_{MX} = 10 MHz Note 3	V_{DD} = 5.0 V	Square wave input		0.15	1.28	
						Resonator connection		0.30	1.36	
					V_{DD} = 3.0 V	Square wave input		0.15	1.28	
						Resonator connection		0.30	1.36	
			Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 5				0.48	1.22	μA
				f_{IL} = 15 kHz, T_A = +25°C Note 5				0.55	1.22	
				f_{IL} = 15 kHz, T_A = +85°C Note 5				0.80	3.30	
				f_{IL} = 15 kHz, T_A = +105°C Note 5				2.00	17.3	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(3/3)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD3} Note 2	STOP mode Note 3	T_A = -40°C		0.19	0.51	μA
			T_A = +25°C		0.25	0.51	
			T_A = +50°C		0.28	1.10	
			T_A = +70°C		0.38	1.90	
			T_A = +85°C		0.60	3.30	
			T_A = +105°C		1.5	17.0	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. The values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 3, 4	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)			0.02		μA
8-bit interval timer operating current Notes 1, 9	I_{TMT}	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)	8-bit counter mode × 2-channel operation		0.04		μA
			16-bit counter mode operation		0.03		μA
Watchdog timer operating current	I_{WDT} Notes 1, 3, 5	f_{IL} = 15 kHz f_{MAIN} stopped (per unit)			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	During maximum-speed conversion	Normal mode, AV_{VREFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{VREFP} = V_{DD} = 3.0 V		0.5	0.7	mA
Internal reference voltage (1.45 V) current Notes 1, 10	I_{ADREF}				85.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				85.0		μA
D/A converter operating current	I_{DAC} Note 1	Per channel				1.5	mA
PGA operating current	I_{PGA} Notes 1, 2				480	700	μA
Comparator operating current	I_{CMP} Note 8	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Comparator high-speed mode Window mode		12.5		μA
			Comparator low-speed mode Window mode		3.0		
			Comparator high-speed mode Standard mode		6.5		
			Comparator low-speed mode Standard mode		1.9		
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Comparator high-speed mode Window mode		8.0		
			Comparator low-speed mode Window mode		2.2		
			Comparator high-speed mode Standard mode		4.0		
			Comparator low-speed mode Standard mode		1.3		
LVD operating current	I_{LVD} Notes 1, 7				0.10		μA
Self-programming operating current	IFSP Notes 1, 12				2.0	12.20	mA
BGO current	IBGO Notes 1, 11				2.0	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation f_{IH} = 24 MHz, AVREFP = V_{DD} = 3.0 V	Mode transition Note 13		0.50	1.10	mA
			The A/D conversion operations are performed		1.20	1.54	mA
		CSI/UART operation f_{IH} = 24 MHz			0.70	1.54	mA
	ISNOZM Note 1	ADC operation f_{IM} = 4 MHz, AVREFP = V_{DD} = 3.0 V	Mode transition Note 13		0.05	0.13	mA
			The A/D conversion operations are performed		0.67	0.84	mA
		CSI operation, f_{IM} = 4 MHz			0.06	0.15	mA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. Operable range is 2.7 to 5.5 V.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and high-speed system clock are stopped.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

Note 8. Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{CMP} when the comparator circuit is in operation.

Note 9. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 10. Current consumed by generating the internal reference voltage (1.45 V).

Note 11. Current flowing during programming of the data flash.

Note 12. Current flowing during self-programming.

Note 13. For transition time to the SNOOZE mode, see **24.3.3 SNOOZE mode** in the RL78/G11 User's Manual.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is T_A = 25°C

3.4 AC Characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

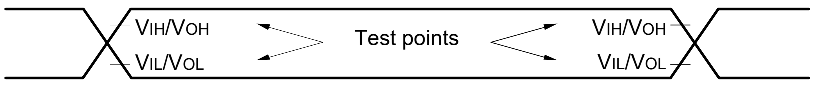
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation	f_{IL}	2.4 V ≤ V_{DD} ≤ 5.5 V		66.7		μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1		20	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1		16	MHz
External system clock input high-/low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
TI00 to TI03 input high-/low-level width	t_{TIH}, t_{TIL} Note 1				1/f_{MCK} + 10			ns
<R> TO00 to TO03, TKBO0, and TKBO1 output frequency Note 2	f_{TO}	TO00 to TO03, TKBO0, and TKBO1 (in the case of output from port pins other than P20)	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	
				2.4 V ≤ EV_{DD} < 2.7 V			4	
		TKBO1 (in the case of output from P20)	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	MHz
				2.7 V ≤ V_{DD} < 4.0 V			1.2	
				2.4 V ≤ V_{DD} < 2.7 V			1	
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	
				2.4 V ≤ EV_{DD} < 2.7 V			4	
<R> Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2, INTP9		2.4 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP3 to INTP8, INTP10, INTP11		2.4 V ≤ EV_{DD} ≤ 5.5 V	1			
Key interrupt input low-level width	t_{KR}	KR0 to KR7		2.4 V ≤ EV_{DD} ≤ 5.5 V	250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Note 1. Following conditions must be satisfied on low level interface of EV_{DD} < V_{DD}.
2.4 V ≤ EV_{DD} ≤ 2.7 V: MIN.125 ns

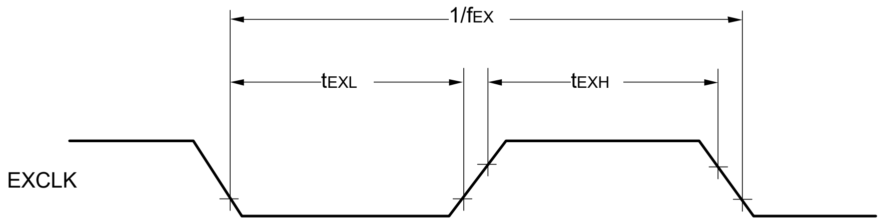
Note 2. When duty is 50%.

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

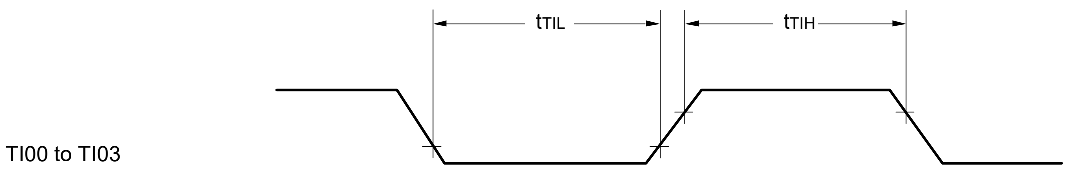
AC Timing Test Points

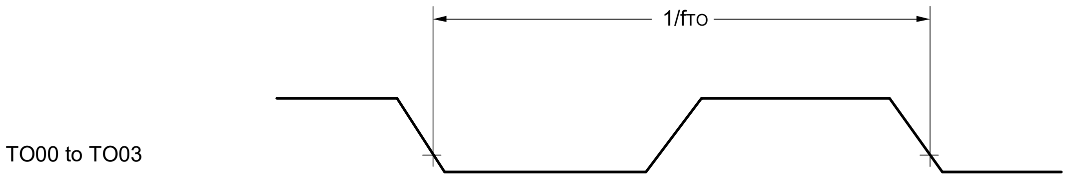


External System Clock Timing

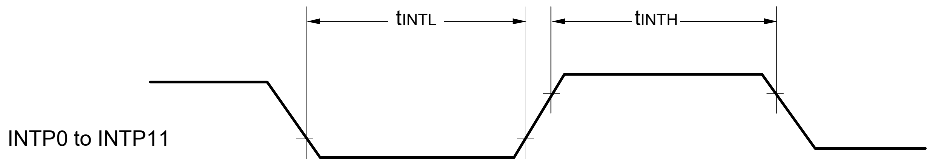


TI/TO Timing

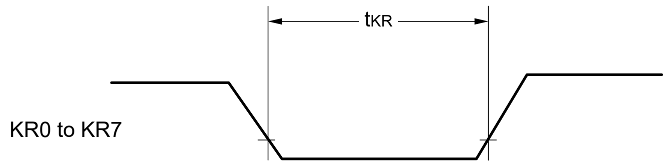




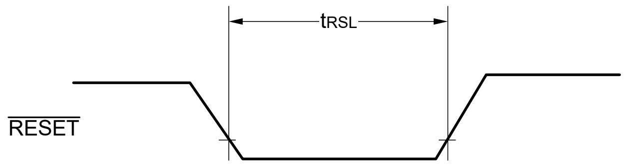
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points

3.5.1 Serial array unit

(1) during communication at same potential (UART mode)
When P01, P30, P31 and P54 are used as TxDq pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate				f_{MCK}/12Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode:
2.4 V ≤ EV_{DD} ≤ 2.7 V: MAX. 1.3 Mbps

Caution **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

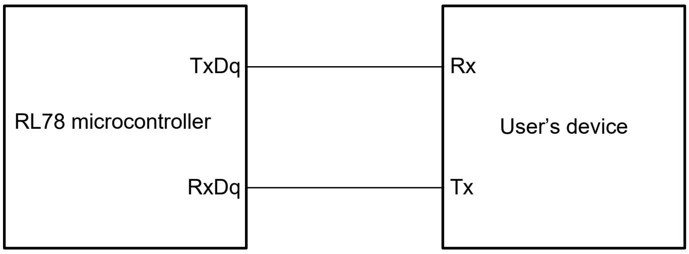
When P20 is used as TxD1 pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

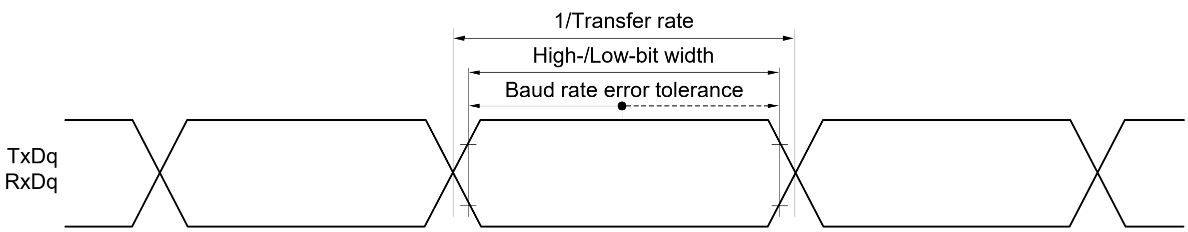
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/16Note	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.5	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/20Note	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.2	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/16Note	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 16 MHz		1.0	Mbps

<R> **Note** Transfer rate in the SNOOZE mode is 4800 bps only. When f_{HOCO} = 48 MHz, SNOOZE mode is not supported.

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

When P01, P32, P53, P54 and P56 are used as SOmn pins

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	250		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2$ - 24		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2$ - 36		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		$t_{KCY1}/2$ - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		66		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V				ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		133		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	1000		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1200		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 24		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		133		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			180	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

When P01, P32, P53, P54 and P56 are used as SOmn pins
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V	f_{MCK} > 16 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 2.7 V		12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD} < 4.0 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ EV_{DD} < 2.7 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD} < 2.7 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK} + 66	ns
			2.4 V ≤ EV_{DD} < 2.7 V		2/f_{MCK} + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	240		ns
			2.4 V ≤ V_{DD} < 2.7 V	400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	$1/f_{MCK}$ + 240		ns
			2.4 V ≤ V_{DD} < 2.7 V	$1/f_{MCK}$ + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	$1/f_{MCK}$ + 240		ns
			2.4 V ≤ V_{DD} < 2.7 V	$1/f_{MCK}$ + 400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	240		ns
			2.4 V ≤ V_{DD} < 2.7 V	400		ns

Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5, 12)

When P20 is used as SO10 pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	20/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	18/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V	f_{MCK} > 16 MHz	20/fMCK and 1000		ns
			f_{MCK} ≤ 16 MHz	18/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 2.7 V		18/f_{MCK} and 1200		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} < 4.0 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ V_{DD} < 2.7 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 190	ns
			2.4 V ≤ V_{DD} < 2.7 V		2/f_{MCK} + 250	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

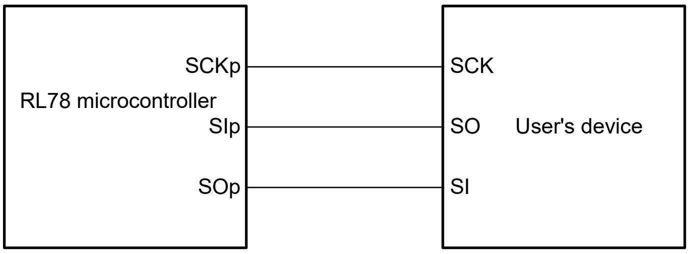
Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

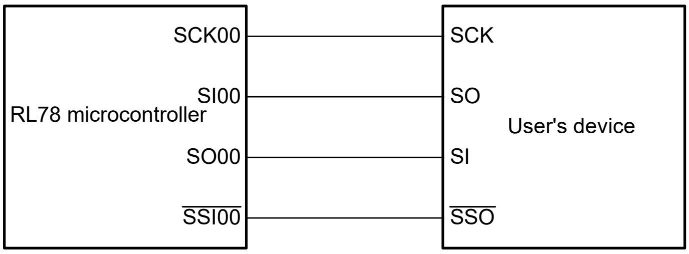
Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

CSI mode connection diagram (during communication at same potential)

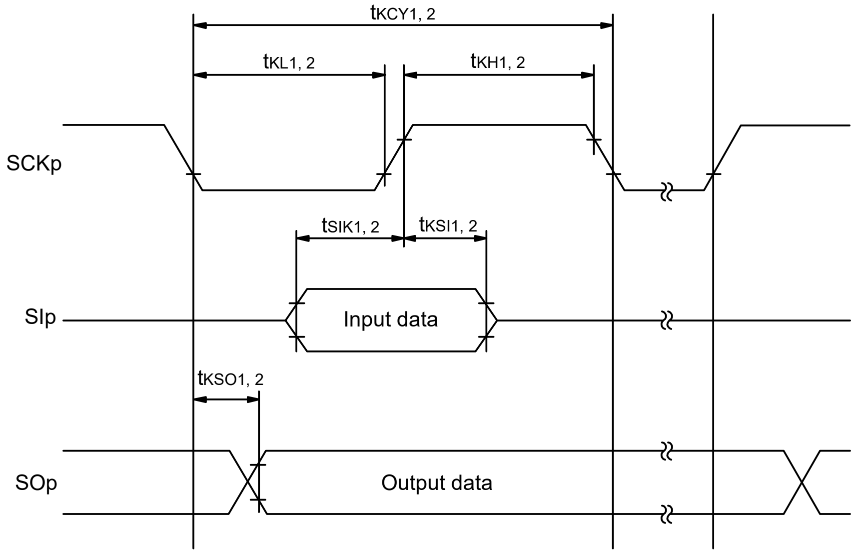


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

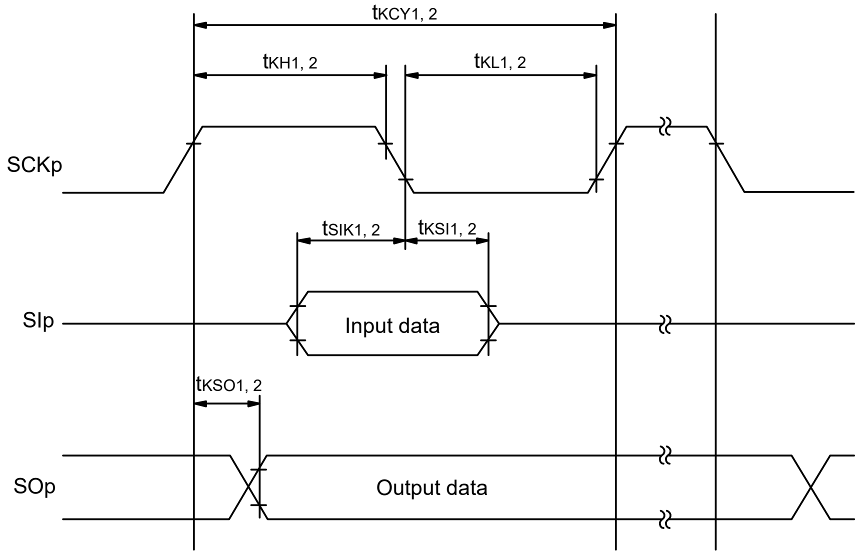


Remark p: CSI number (p = 00, 01, 10 and 11)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

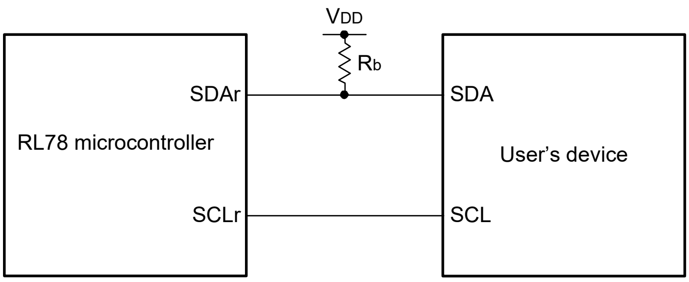
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 220 Note 2		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 580 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

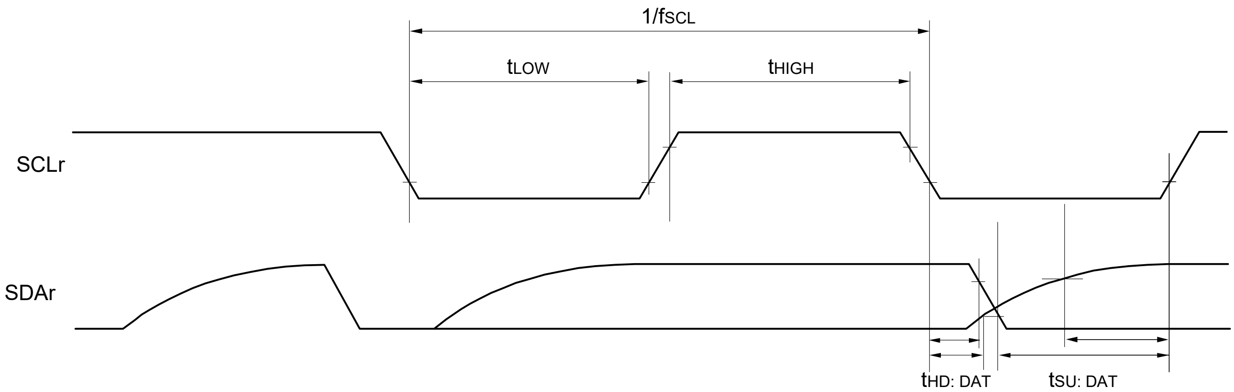
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution **Select the normal input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 3), mn = 00 to 03)

(5) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (UART mode) (dedicated baud rate generator output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions			HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
Transfer rate		Reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V			$f_{MCK}/12$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		2.0	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/12$ Note 1	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		2.0	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/12$ Notes 1, 2	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with EV_{DD} ≥ Vb.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM numbers (g = 0, 2, 3, 5, 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions			HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
Transfer rate		Transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			Note 1	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.6 Note 2	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			Note 3	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			Notes 5, 6	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with EV_{DD} ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V $\le EV_{DD} <$ 3.3 V and 1.6 V $\le V_b \le$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

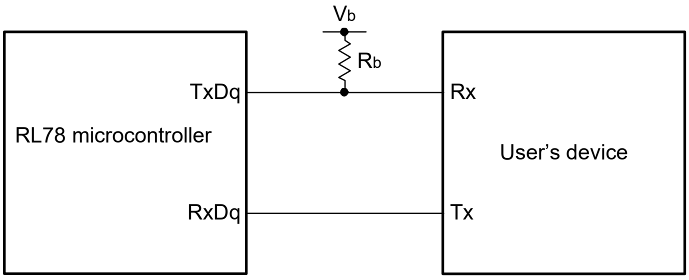
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

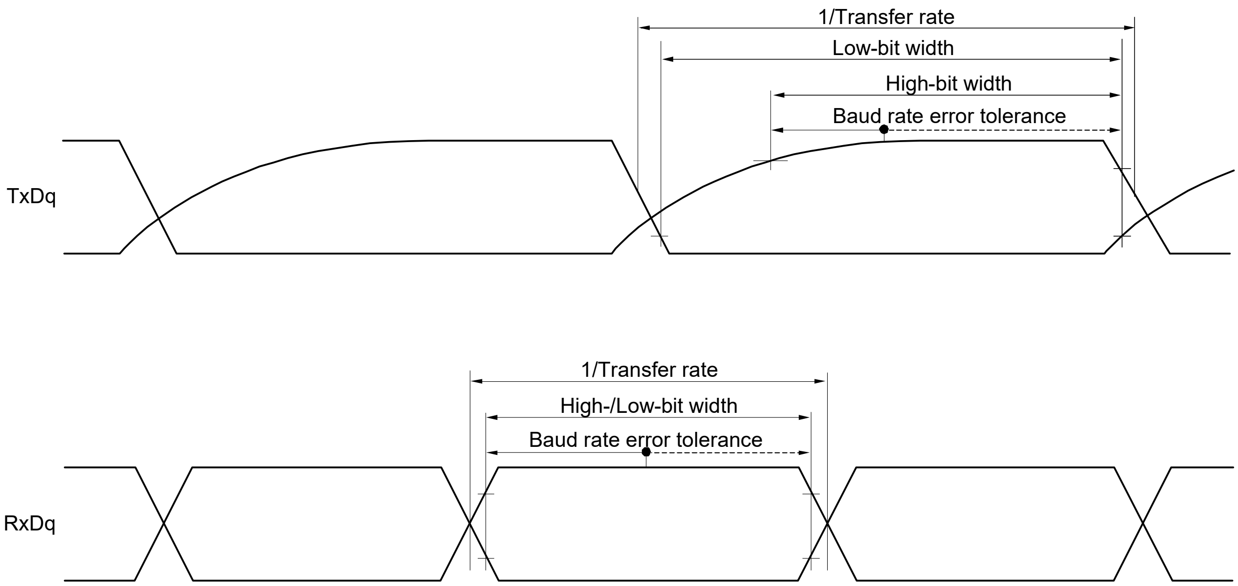
Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(6) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 150		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 340		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 916		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 100		ns

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

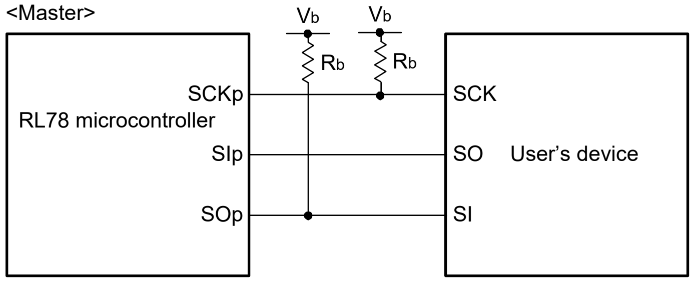
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		966	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	88		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		50	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ			ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
Note 3. Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

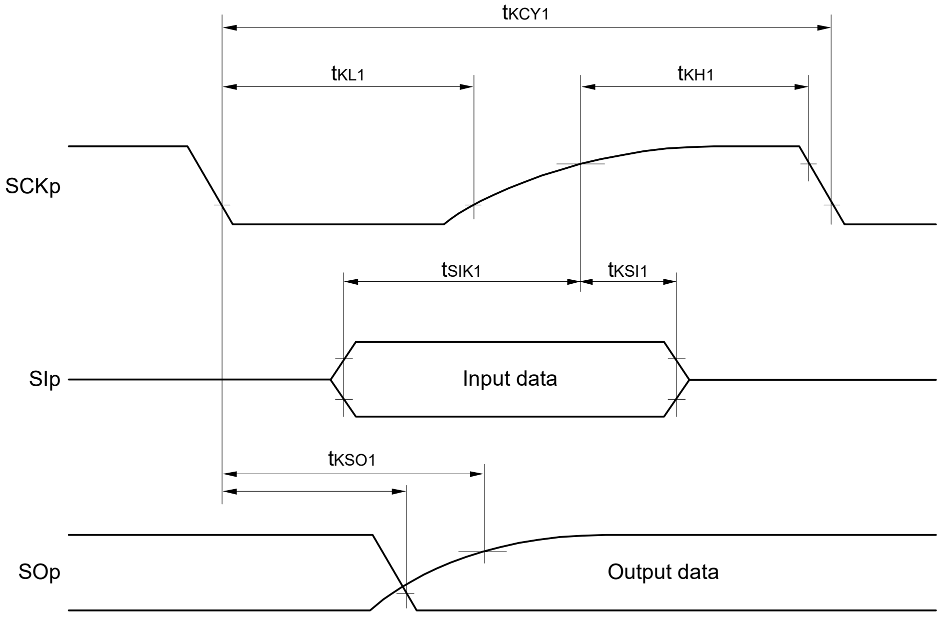


Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

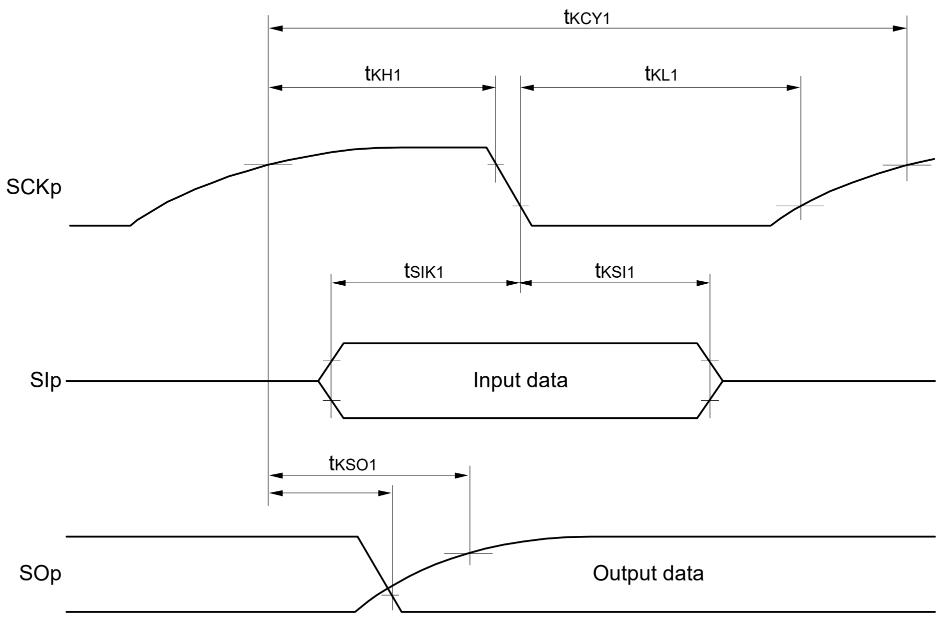
Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $EV_{DD} \geq V_b$.

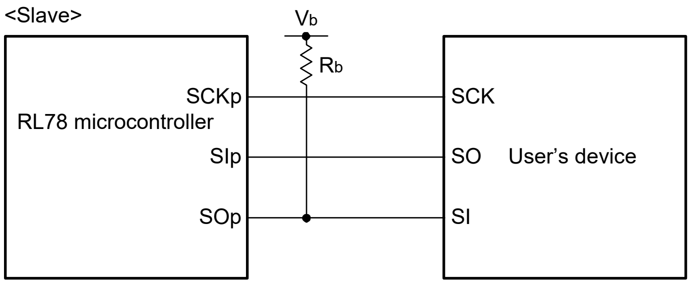
Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)

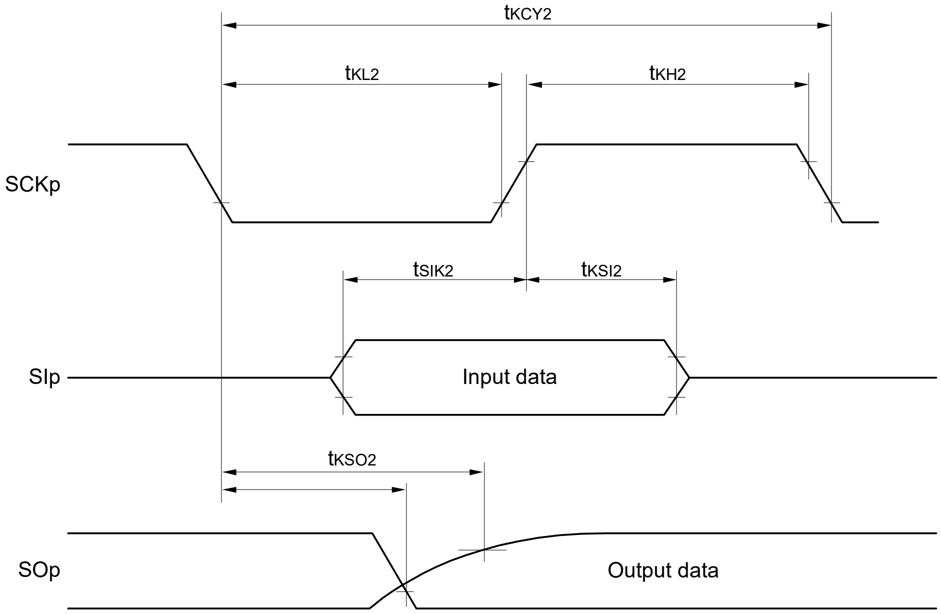


Remark 1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

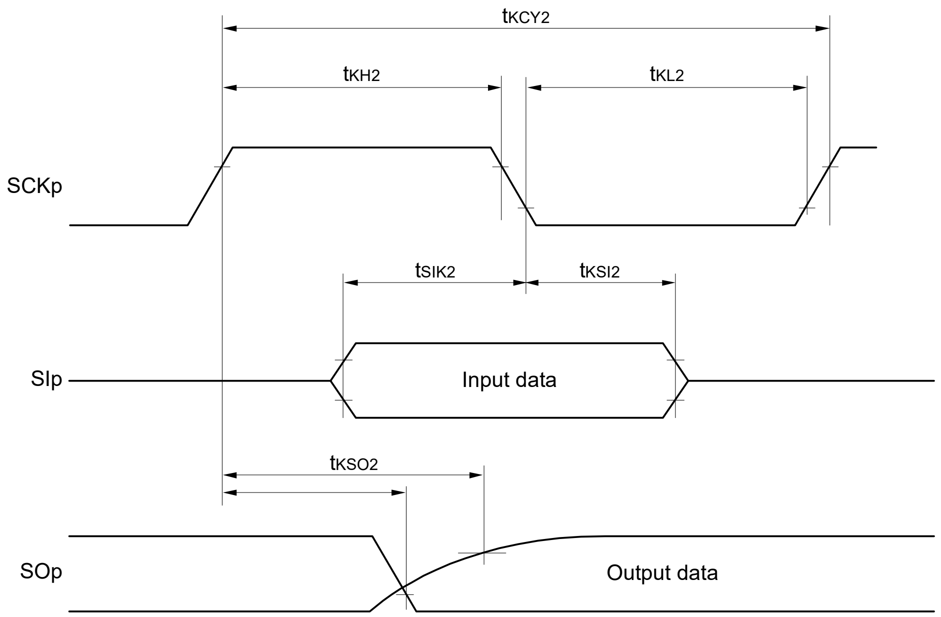
Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (simplified I^{2}C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	4600		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	620		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	2700		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 3		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note 3		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

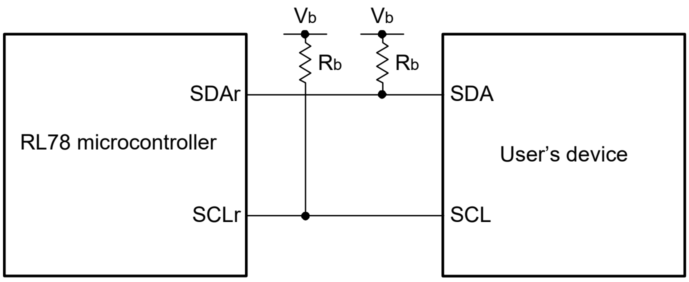
Note 1. The value must be equal to or less than $f_{MCK}/4$.

Note 2. Use it with $EV_{DD} \geq V_b$.

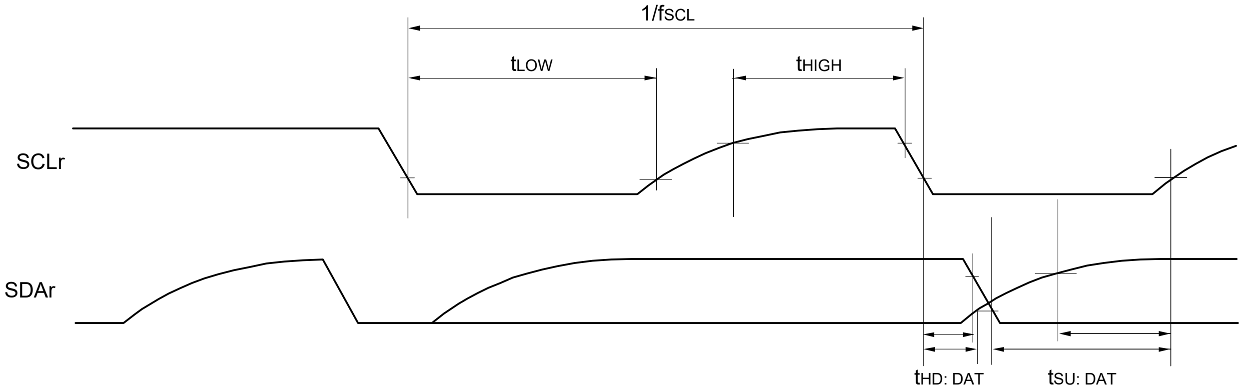
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 3), mn = 00 to 03)

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		μs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

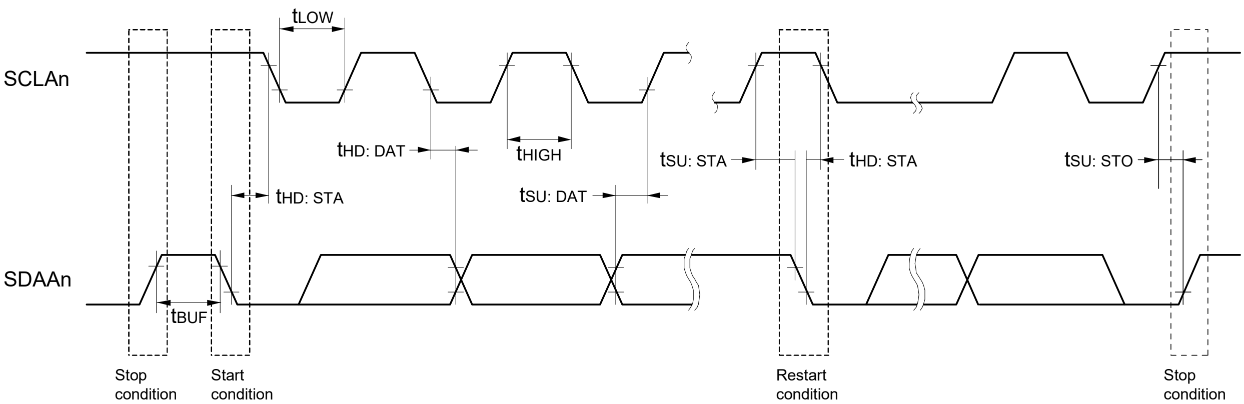
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-)= AVREFM
ANI0 to ANI3	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI22	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 and ANI3	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	μs
			1.8 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V			±1.5	LSB
Analog input voltage	VAIN	ANI2 and ANI3		0		AVREFP	V
		Internal reference voltage (2.4 V ≤ VDD ≤ 5.5 V)		VBGR Note 4			V
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 5.5 V)		VTMPS25 Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 3. When AVREFP < VDD, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.
Note 4. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI22		0		AV_{REFP} and EV_{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI3		0		V_{DD}	V
		ANI16 to ANI22		0		EV_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).
Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.
Note 3. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0 to ANI3, ANI16 to ANI22

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} ≤ V_{DD} = 0 V,
Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	t_{CONV}		17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}				±0.60	% FSR
Integral linearity error Note 1	ILE				±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 3.6 V	5			μs

3.6.3 D/A converter characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{SS} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs
			2.4 V ≤ V_{DD} < 2.7 V			6	μs

3.6.4 Comparator

(Comparator 0: T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)
(Comparator 1: T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	V_{IREF0}	IVREF0 pin		0		V_{DD} - 1.4 Note 1	V
	V_{IREF1}	IVREF1 pin		1.4 Note 1		V_{DD}	V
	V_{ICMP}	IVCMP0 pin		-0.3		V_{DD}+0.3	V
		IVCMP1 pin		-0.3		EV_{DD}+0.3	V
Output delay	td	V_{DD} = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			1.5	μs
			Comparator low-speed mode, standard mode		3		μs
			Comparator low-speed mode, window mode		4		μs
Operation stabilization wait time	t_{CMP}			100			μs
Reference voltage declination in channel 0 of internal DAC Note 2	⊿VIDAC					±2.5	LSB

Note 1. In window mode, make sure that V_{REF1} - V_{REF0} ≥ 0.2 V.
Note 2. Only in CMP0

3.6.5 PGA

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9 × V_{DD}/Gain	V
Output voltage range	V_{IOHPGA}			0.93 × V_{DD}			V
	V_{IOLPGA}					0.07 × V_{DD}	V
Gain error		x4, x8				±1	%
		x16				±1.5	%
		x32				±2	%
Slew rate	SR_{RPGA}	Rising When V_{IN} = 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/μs
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling When V_{IN}= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
Reference voltage stabilization wait time[Note]	t_{PGA}	x4, x8				5	μs
		x16, x32				10	μs

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

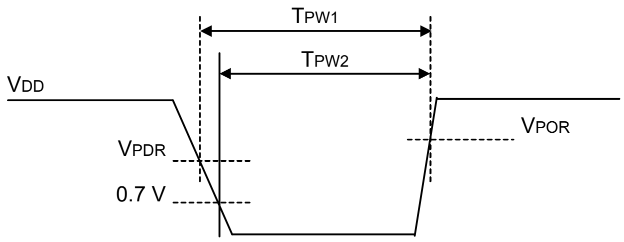
3.6.6 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOR	Power supply rise time	1.47	1.51	1.55	V
	VPDR	Power supply fall time Note 1	1.46	1.50	1.56	V
Minimum pulse width Note 2	TPW1	Other than STOP/SUB HALT/SUB RUN	300			μs
	TPW2	STOP/SUB HALT/SUB RUN	300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
				Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
				Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

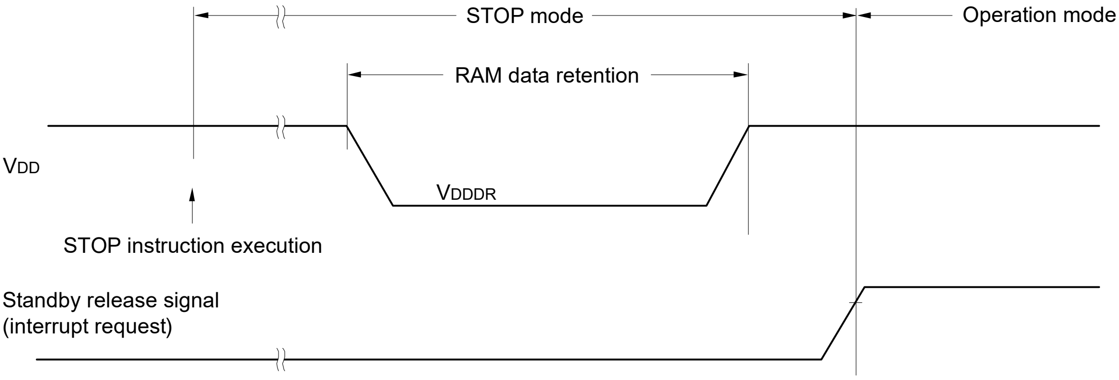
Caution **Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.**

3.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK			1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	TA = 25°C		1,000,000		
		Retained for 5 years	TA = 85°C	100,000			
		Retained for 20 years	TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

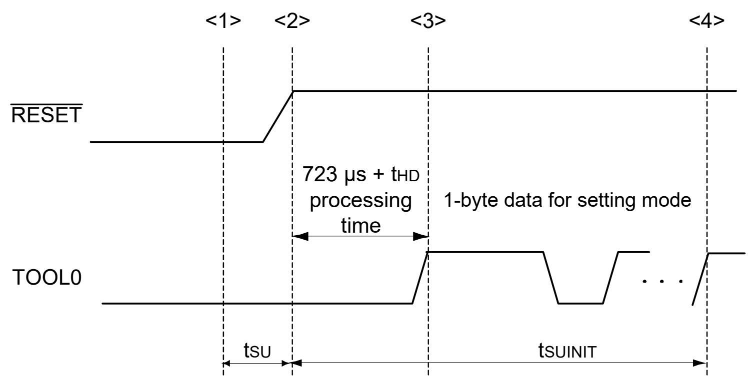
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified Note 1	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends Note 1	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) Notes 1, 2	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms

Note 1. Deassertion of the POR and LVD reset signals must precede deassertion of the pin reset signal.

Note 2. This excludes the flash firmware processing time (723 μs).

<R>



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

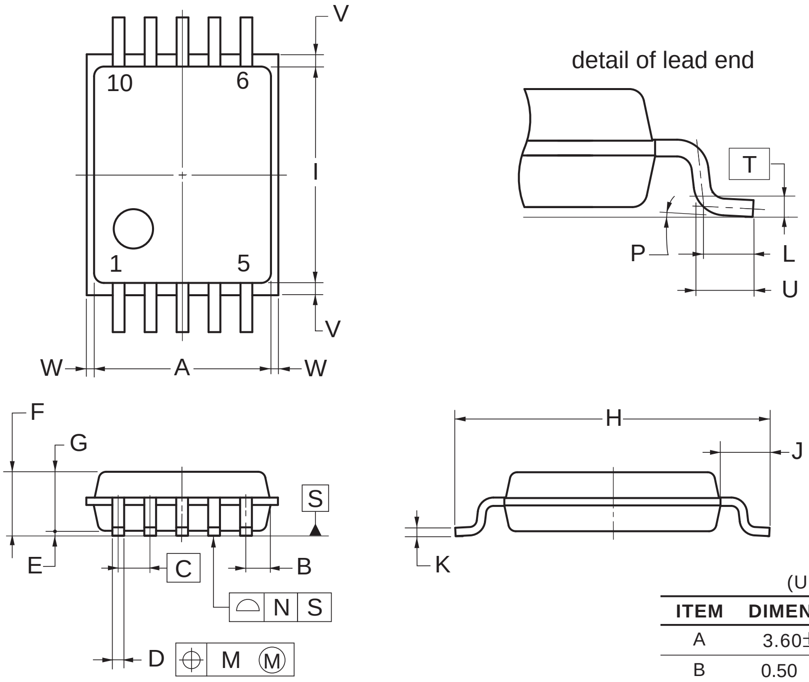
Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 10-pin products

R5F1051AGSP, R5F1051AASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

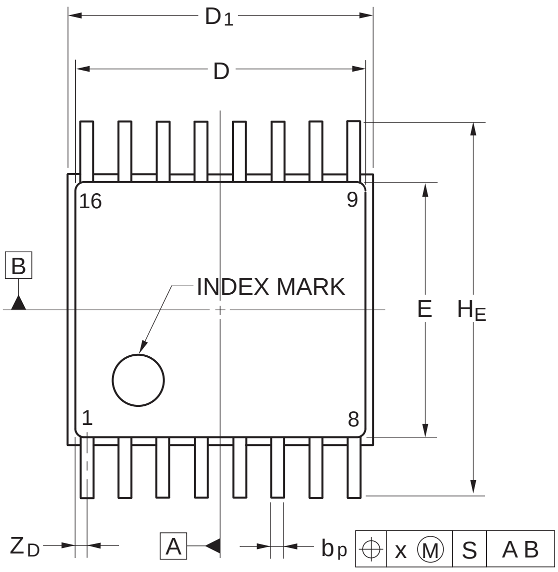
NOTE

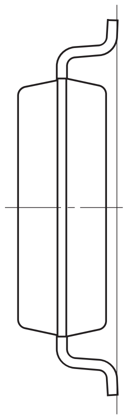
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

4.2 16-pin products

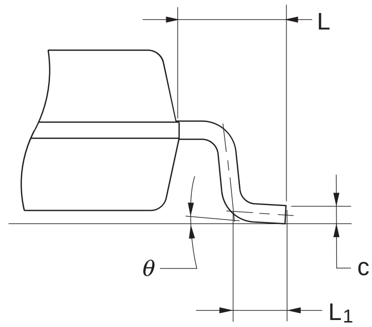
R5F1054AGSP, R5F1054AASP

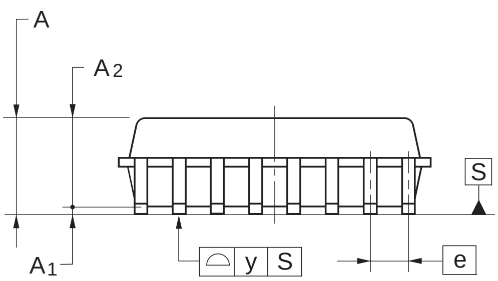
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB	0.08



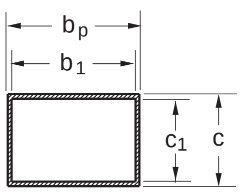


detail of lead end





Terminal cross section

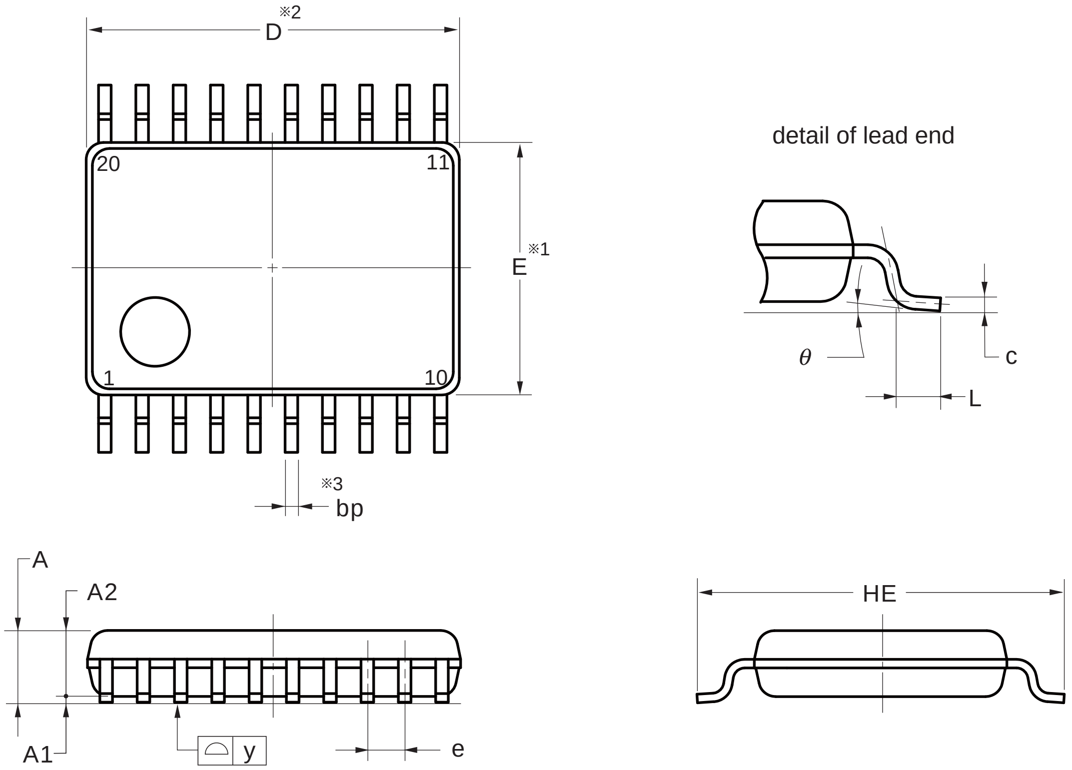


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
$\boxed{e}$	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—

4.3 20-pin products

R5F1056AGSP, R5F1056AASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



(UNIT:mm)

ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	$0.22^{+0.10}_{-0.05}$
c	$0.15^{+0.05}_{-0.02}$
L	0.50±0.20
y	0.10
θ	0° to 10°

NOTE

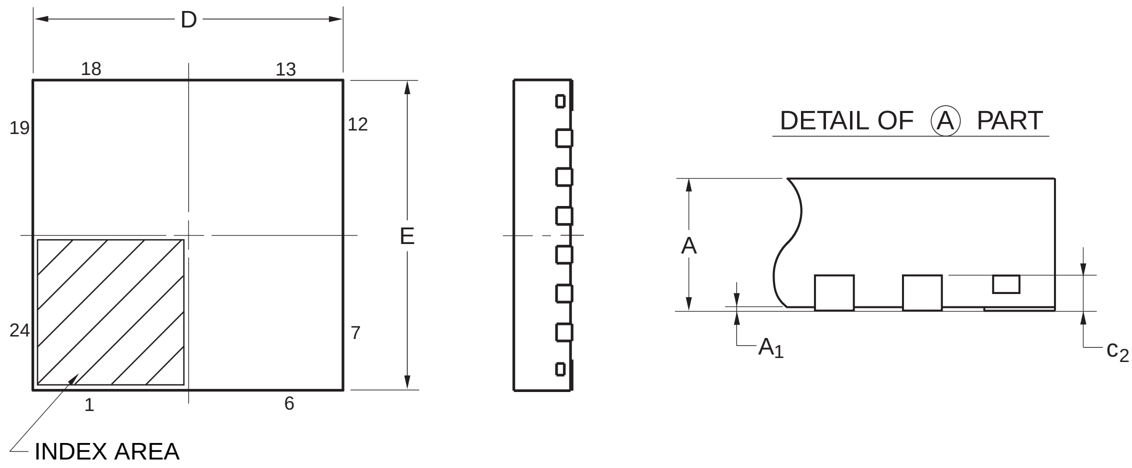
1.Dimensions “※1” and “※2” do not include mold flash.

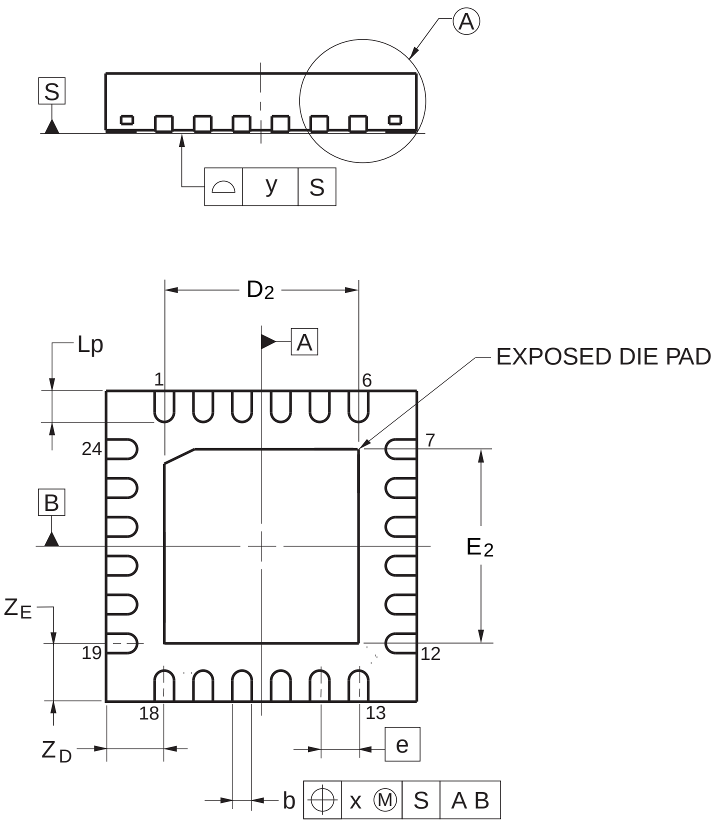
2.Dimension “※3” does not include trim offset.

4.4 24-pin products

R5F1057AGNA, R5F1057AANA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04



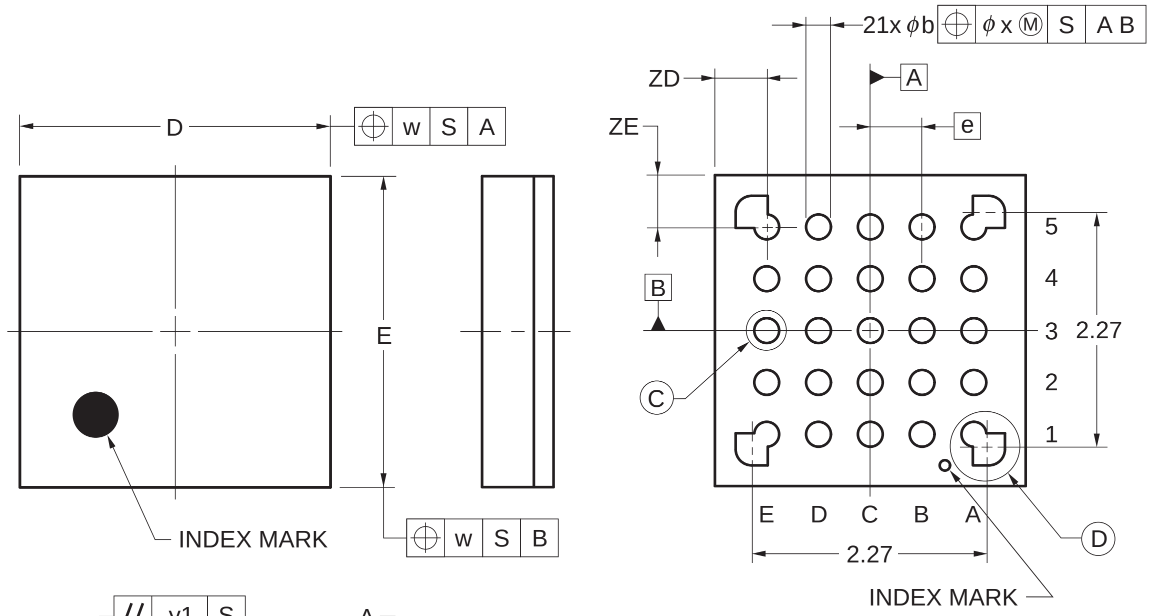


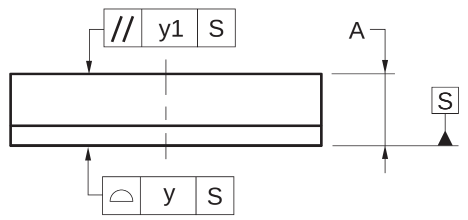
Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.95	4.00	4.05
E	3.95	4.00	4.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	2.50	—
E_2	—	2.50	—

4.5 25-pin products

R5F1058AGLA, R5F1058AALA

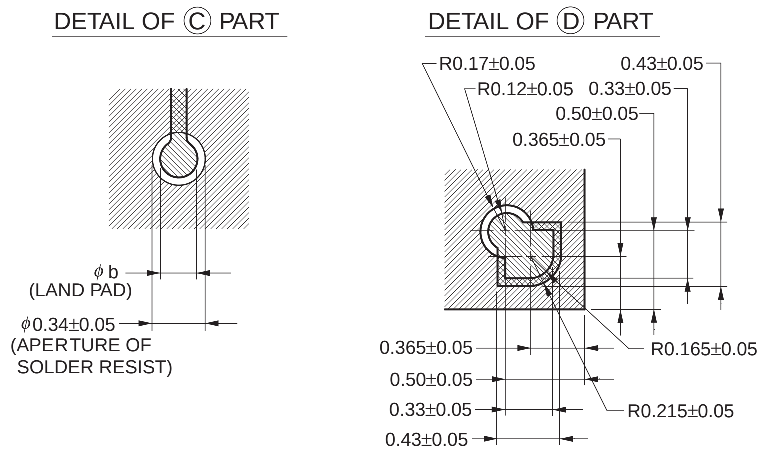
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01





ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

(UNIT:mm)



Rev.	Date	Description	
		Page	Summary
0.50	Mar 31 2016	—	First Edition issued
1.00	Sep 28 2016	p.7	Modification of Pin Configuration in 1.3.3 25-pin products
		p.9	Addition of 1.5.1 20-pin products
		p.10	Addition of product name and Modification of Block Diagram in 1.5.2 24-pin, 25-pin products
		p.12	Addition of I^2C bus in 1.6 Outline of Functions
		p.15	Modification of Conditions of I_{OH1}, I_{OL1} in 2.1 Absolute Maximum Ratings
		p.16	Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D_{IMT}, D_{IMV} in 2.2.2 On-chip oscillator characteristics
		p.17	Modification of Caution in 2.3.1 Pin characteristics
		p.19	Modification of Input voltage, high and Input voltage, low in 2.3.1 Pin characteristics
		p.19, 20	Modification of Caution in 2.3.1 Pin characteristics
		p.22, 23, 24, 26, 27	Modification of specifications in 2.3.2 Supply current characteristics
		p.29, 30	Modification of specification in 2.4 AC Characteristics
		p.35	Modification of specifications in 2.5.1 Serial array unit (1)
		p.39	Modification of specifications in 2.5.1 Serial array unit (3)
		p.40, 42	Modification of specification in 2.5.1 Serial array unit (4)
		p.62	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (1)
		p.64	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (2)
		p.65	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (3)
		p.70	Modification of Conditions in 2.6.2 Temperature sensor haracteristics/internal reference voltage characteristic
		p.79	Addition of description in 3 ELECTRICAL SPECIFICATIONS (TA = -40 to +105°C)
		p.82	Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D_{IMT}, D_{IMV} in 3.2.2 On-chip oscillator characteristics
		p.83	Modification of Caution in 3.3.1 Pin characteristics
		p.85	Modification of Input voltage, high and Input voltage, low in 3.3.1 Pin characteristics
		p.85, 86	Modification of Caution in 3.3.1 Pin characteristics
		p.88 to 91	Modification of specifications in 3.3.2 Supply current characteristics
		p.97	Modification of specifications and specification table in 3.5.1 Serial array unit (1)
		p.103	Modification of specifications in 3.5.1 Serial array unit (3)
		p.125	Modification of Conditions in 3.6.1 A/D converter characteristics (4)
		p.126	Modification of Conditions in 3.6.2 Temperature sensor haracteristics/internal reference voltage characteristic
1.10	Dec 28 2016	p.4	Modification of 1.2 Ordering Information
2.00	Feb 15, 2018	Throughout	Addition of specifications of 10-pin and 16-pin products
		p.2	Modification of description in 1.1 Features
		p.6	Modification of figure in 1.3.4 24-pin products
		p.11	Modification of figure in 1.5.3 20-pin products
		p.12	Modification of figure in 1.5.4 24-pin, 25-pin products

Rev.	Date	Description	
		Page	Summary
2.00	Feb 15, 2018	p.13, 14	Modification of table in 1.6 Outline of Functions
		p.18	Modification of 2.2.2 On-chip oscillator characteristics
		p.19, 21	Modification of 2.3.1 Pin characteristics
		p.24	Modification of 2.3.2 Supply current characteristics
		p.32	Modification of 2.4 AC Characteristics
		p.79	Modification of figure in 2.10 Timing of Entry to Flash Memory Programming Modes
		p.84	Modification of 3.2.1 X1 characteristics
		p.84	Modification of 3.2.2 On-chip oscillator characteristics
		p.85, 86, 87	Modification of 3.3.1 Pin characteristics
		p.95	Modification of 3.4 AC Characteristics
		p.99	Modification of note in 3.5.1 Serial array unit (1)
		p.134	Modification of figure in 3.10 Timing of Entry to Flash Memory Programming Modes

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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