

# R2A20169NP/SA/SP

8-bit 12ch D/A Converter with Buffer Amplifiers

R03DS0020EJ0300

Rev.3.00

Jul 25, 2013

## Description

The R2A20169 is an integrated circuit semiconductor of CMOS structure with 12 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc ( 0 to 5V ), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

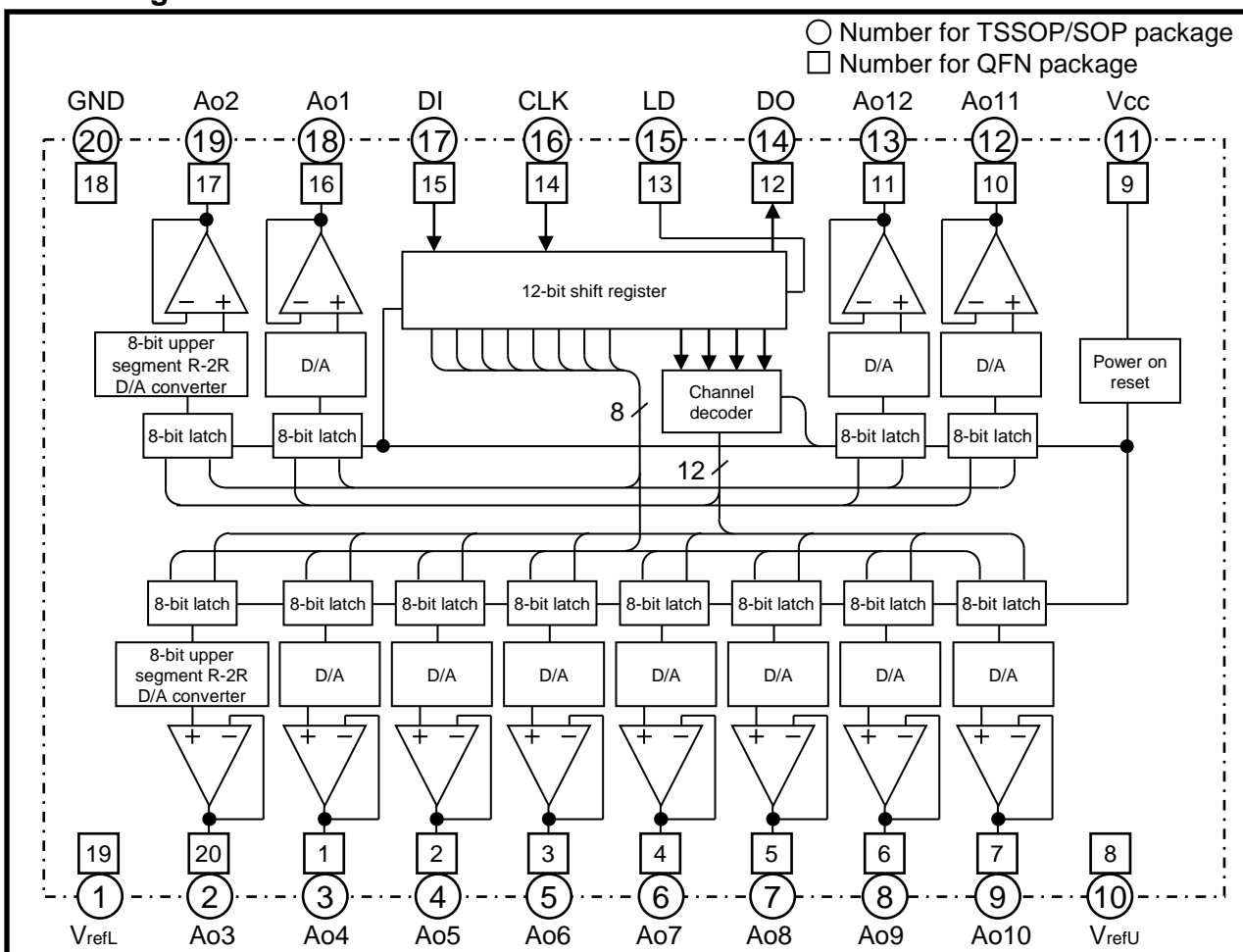
## Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire ( DI, SCK, LD )
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc ( 0 to 5V )
- High output current capacity: +/-1mA or Higher
- Very small size package line-up: QFN-20 (pin pitch: 0.5mm), TSSOP-20 (pin pitch 0.65mm)

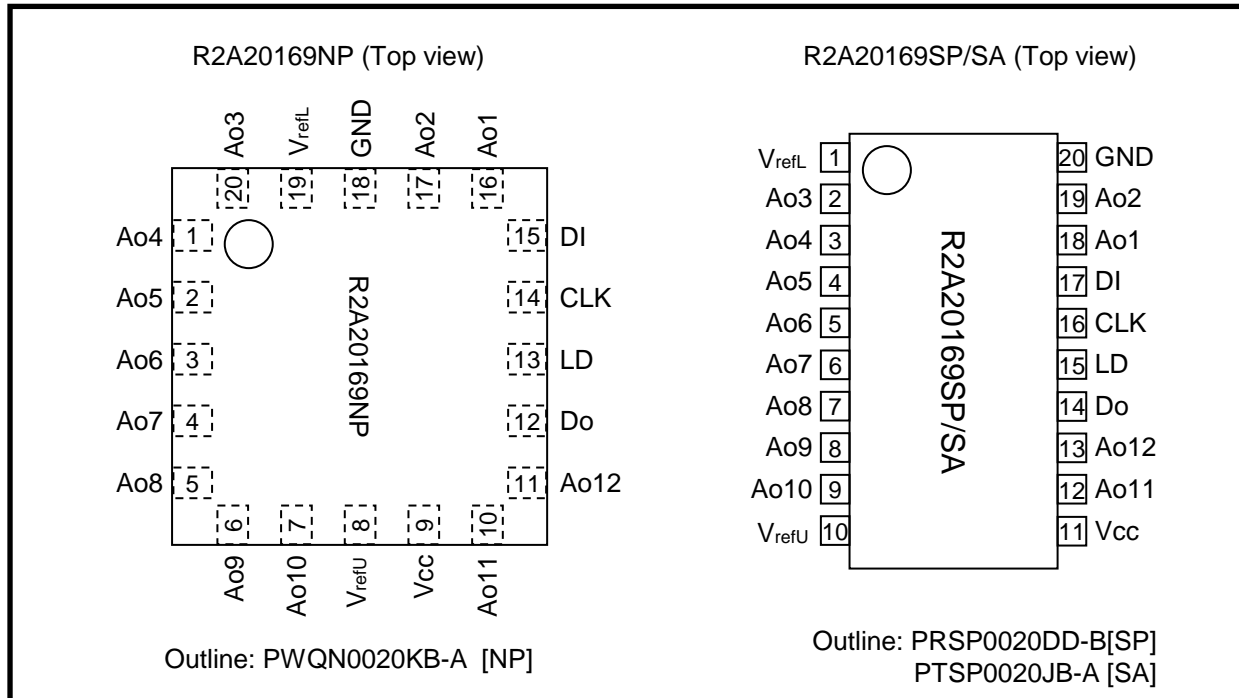
## Application

- Conversion from digital data to analog control data for home-use and industrial equipment.

## Block Diagram



## Pin Arrangement



## Pin Description

| Pin No. |              | Pin Name | Function   |
|---------|--------------|----------|--|
| [QFN]   | [TSSOP /SOP] |          |  |
| 15      | 17           | DI       | Serial data input terminal.<br>(Input serial data with a 12-bit data length.)  |
| 12      | 14           | Do       | Serial data output terminal<br>(Data is sequentially output from the MSB bit.)   |
| 14      | 16           | CLK      | Serial clock input terminal<br>(Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)          |
| 13      | 15           | LD       | Load terminal<br>(When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.) |
| 16      | 18           | Ao1      | 8-bit resolution D/A converter output terminals<br>(After power-on, all channels are reset and DAC data 00h is output.)            |
| 17      | 19           | Ao2      |  |
| 20      | 2            | Ao3      |  |
| 1       | 3            | Ao4      |  |
| 2       | 4            | Ao5      |  |
| 3       | 5            | Ao6      |  |
| 4       | 6            | Ao7      |  |
| 5       | 7            | Ao8      |  |
| 6       | 8            | Ao9      |  |
| 7       | 9            | Ao10     |  |
| 10      | 12           | Ao11     |  |
| 11      | 13           | Ao12     |  |
| 9       | 11           | Vcc      | Power supply terminal  |
| 18      | 20           | GND      | GND terminal   |
| 8       | 10           | VrefU    | D/A converter upper reference voltage input terminal   |
| 19      | 1            | VrefL    | D/A converter lower reference voltage input terminal   |

## Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

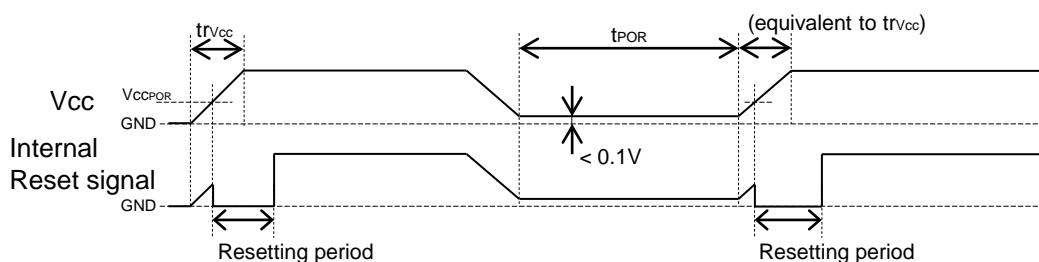
| Item                                  | Symbol  | Conditions | Ratings                       | Unit   |
|---------------------------------------|---------|------------|-------------------------------|--------|
| Supply voltage                        | Vcc     |            | -0.3 to +6.5                  | V      |
| D/A converter upper reference voltage | VrefU   |            | -0.3 to +6.5                  | V      |
| D/A converter lower reference voltage | VrefL   |            | -0.3 to +6.5                  | V      |
| Buffer amplifier output current       | IAO     | Continuous | -2.0 to +2.0                  | mA     |
| Input voltage                         | Vin     |            | -0.3 to Vcc+0.3 <+6.5         | V      |
| Output voltage                        | Vo      |            | -0.3 to Vcc+0.3 <+6.5         | V      |
| Power dissipation                     | Pd      | Ta= +85deg | 290(NP) / 150(SA) / 300(SP)   | mW     |
| Thermal derating factor               | K theta | Ta> +25deg | 7.25(NP) / 3.75(SA) / 7.5(SP) | mW/deg |
| Operating temperature                 | Topr    |            | -30 to +85                    | deg    |
| Storage temperature                   | Tstg    |            | -40 to +125                   | deg    |

## Electrical Characteristics

« Digital Part » (Vcc, VrefU = +5V +/-10%, Vcc>VrefU, GND, VrefL =0V, Ta= -30 to +85deg, Unless otherwise noted )

| Item   | Symbol | Test conditions               | Limits    |     |        | Unit |
|--|--------|-------------------------------|-----------|-----|--------|------|
|  |        |                               | Min       | Typ | Max    |      |
| Supply voltage   | Vcc    |                               | 2.7       | 5.0 | 5.5    | V    |
| Supply current   | Icc    | CLK = 1MHz, Vcc =5V, IAO =0μA | -         | 0.6 | 1.8    | mA   |
| Input leak current                                       | IILK   | VIN = 0 to Vcc                | -10       | -   | 10     | μA   |
| Input low voltage  | VIL    |                               | -         | -   | 0.2Vcc | V    |
| Input high voltage                                       | VIH    | 4.0V < Vcc                    | 0.5Vcc    | -   | -      | V    |
|  |        | Vcc < 4.0V                    | 0.8Vcc    | -   | -      | V    |
| Output low voltage                                       | VOL    | 4.0V < Vcc, IOL =2.0 mA       | -         | -   | 0.4    | V    |
|  |        | Vcc < 4.0V, IOL =1.5 mA       | -         | -   | 0.4    | V    |
| Output high voltage                                      | VOH    | Ioh = -400 μA                 | Vcc - 0.4 | -   | -      | V    |
| Supply voltage rise time *1                              | trVcc  | Vcc = 0 @ 2.7V                | 100       | -   | -      | μs   |
| Internal reset operating voltage *1                      | VCCPOR | Vcc = 0 @ 2.7V                | -         | 1.5 | 1.9    | V    |
| Power supply restart interval (Power supply OFF à ON) *1 | tPOR   | Vcc < 0.1V                    | 1         | -   | -      | ms   |

\*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (tPOR).



« Analog Part » (  $V_{CC}, V_{refU} = +5V \pm 10\%$ ,  $V_{CC} > V_{refU}$ ,  $GND, V_{refL} = 0V$ ,  $T_a = -30$  to  $+85$ deg, unless otherwise noted )

| Item   | Symbol     | Test conditions   | Limits      |     |                | Unit    |
|--|------------|---|-------------|-----|----------------|---------|
|  |            |   | Min         | Typ | Max            |         |
| Current dissipation                            | $I_{refU}$ | $V_{refU}=5V, V_{refL}=0V, I_{AO}=0\mu A$ ,<br>Data condition: at maximum current                                 | -           | 1.5 | 3.0            | mA      |
| D/A converter upper reference voltage range *2 | $V_{refU}$ | $V_{CC} \geq 4.5V$  | 3.5         | -   | $V_{CC}$       | V       |
|  |            | $V_{CC} < 4.5V$   | $0.7V_{CC}$ | -   | $V_{CC}$       |         |
| D/A converter lower reference voltage range *2 | $V_{refL}$ | $V_{CC} \geq 4.5V$  | GND         | -   | $V_{CC}-3.5$   | V       |
|  |            | $V_{CC} < 4.5V$   | GND         | -   | $0.3V_{CC}$    |         |
| Buffer amplifier output voltage range          | $V_{AO}$   | $I_{AO} = \pm 100 \mu A$  | 0.1         | -   | $V_{CC} - 0.1$ | V       |
|  |            | $I_{AO} = \pm 500 \mu A$  | 0.2         | -   | $V_{CC} - 0.2$ | V       |
| Buffer amplifier output drive range            | $I_{AO}$   | Upper side saturation voltage = 0.3V,<br>Lower side saturation voltage = 0.2V                                     | -1.0        | -   | 1.0            | mA      |
| Differential nonlinearity                      | $S_{DL}$   | $V_{refU} = 4.79V$ ,<br>$V_{refL} = 0.95V$ ,<br>$V_{CC} = 5.5V$ (15mV/LSB),<br>Without load ( $I_{AO} = 0\mu A$ ) | -0.7        | -   | 0.7            | LSB     |
| Nonlinearity                                   | $S_L$      |   | -1.0        | -   | 1.0            | LSB     |
| Zero code error                                | $S_{ZERO}$ |   | -2.0        | -   | 2.0            | LSB     |
| Full scale error                               | $S_{FULL}$ |   | -2.0        | -   | 2.0            | LSB     |
| Output capacitive load                         | $C_o$      |   | -           | -   | 0.1            | $\mu F$ |
| Buffer amplifier output impedance              | $R_o$      |   | -           | 5.0 | -              | ohm     |

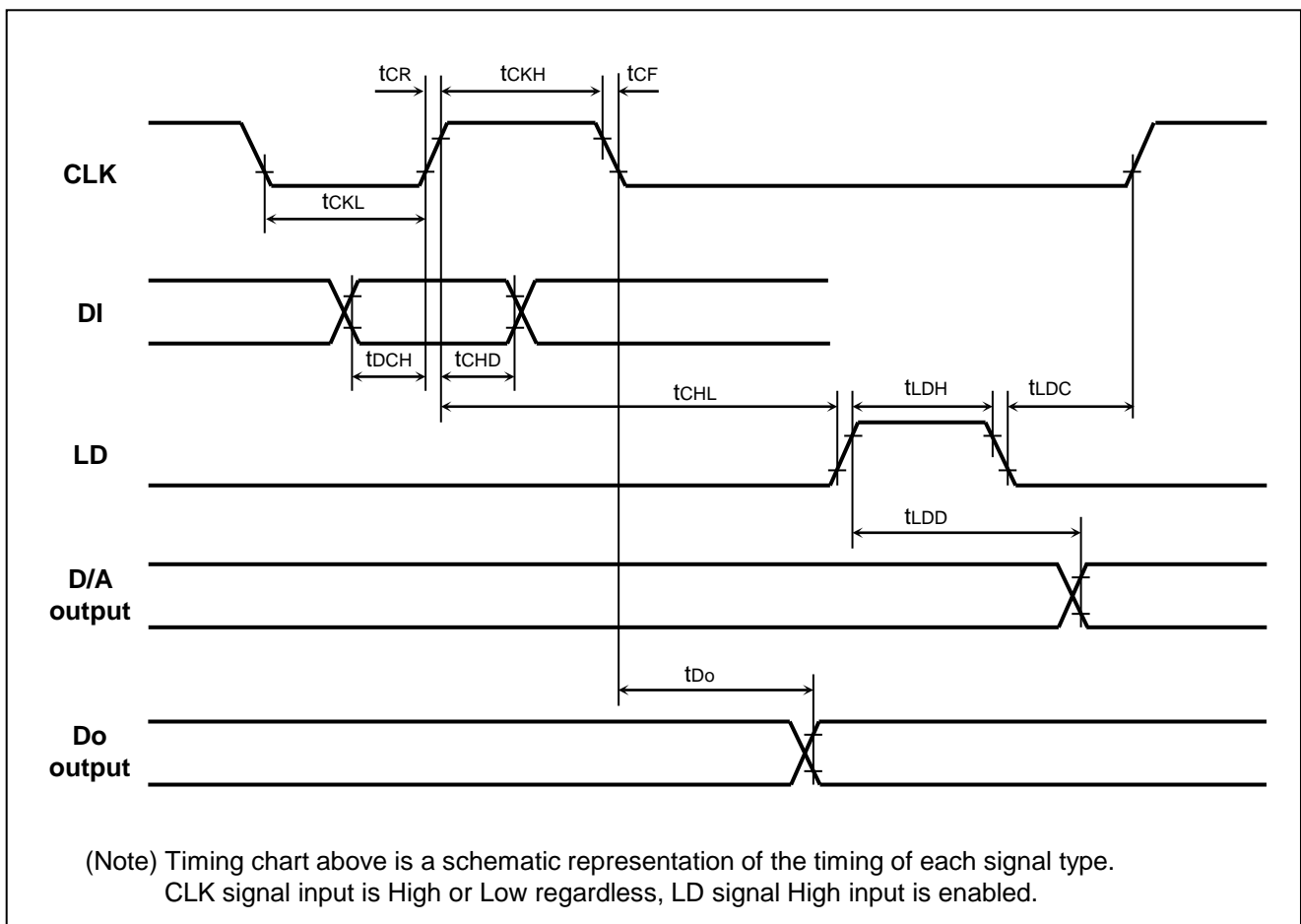
\*2 : The output does not necessary be the value with the reference voltage setting range.  
The output value is determined by the buffer amplifier output voltage range ( $V_{AO}$ ).

## AC Characteristics

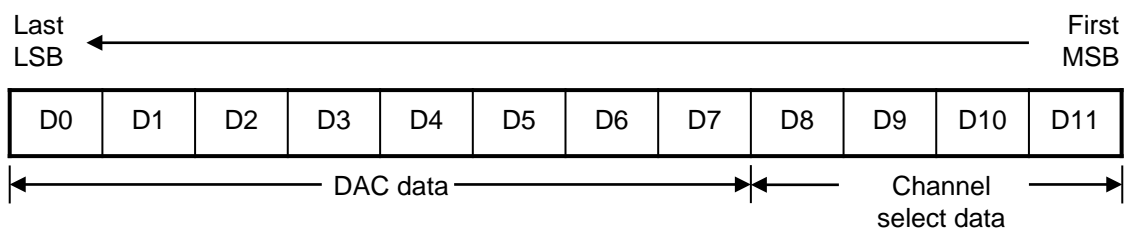
(  $V_{CC}$ ,  $V_{refU} = +5V \pm 10\%$ ,  $V_{CC} > V_{refU}$ ,  $GND = V_{refL} = 0V$ ,  $T_a = -30$  to  $+85$ deg, unless otherwise noted )

| Item                     | Symbol    | Test conditions   | Limits |     |     | Unit    |
|--------------------------|-----------|---|--------|-----|-----|---------|
|                          |           |   | Min    | Typ | Max |         |
| Clock frequency          | $f_{CLK}$ |   | -      | 1.0 | 10  | MHz     |
| Clock low pulse width    | $t_{CKL}$ |   | 40     | -   | -   | ns      |
| Clock high pulse width   | $t_{CKH}$ |   | 40     | -   | -   | ns      |
| Clock rise time          | $t_{CR}$  |   | -      | -   | 200 | ns      |
| Clock fall time          | $t_{CF}$  |   | -      | -   | 200 | ns      |
| Data setup time          | $t_{DCH}$ |   | 4      | -   | -   | ns      |
| Data hold time           | $t_{CHD}$ |   | 30     | -   | -   | ns      |
| LD setup time            | $t_{CHL}$ |   | 40     | -   | -   | ns      |
| LD hold time             | $t_{LDC}$ |   | 40     | -   | -   | ns      |
| LD high pulse width      | $t_{LDH}$ |   | 40     | -   | -   | ns      |
| Data output delay time   | $t_{DO}$  | $C_L < 100$ pF  | -10    | -   | 50  | ns      |
| D/A output settling time | $t_{LDD}$ | $T_a = 25$ deg, $C_L < 100$ pF, $V_{AO}: 0.5 \rightarrow @ 4.5V$ ,<br>The time until the output becomes the final value of 1/2 LSB. | -      | -   | 150 | $\mu$ s |

## Timing Chart



## Digital Data Format



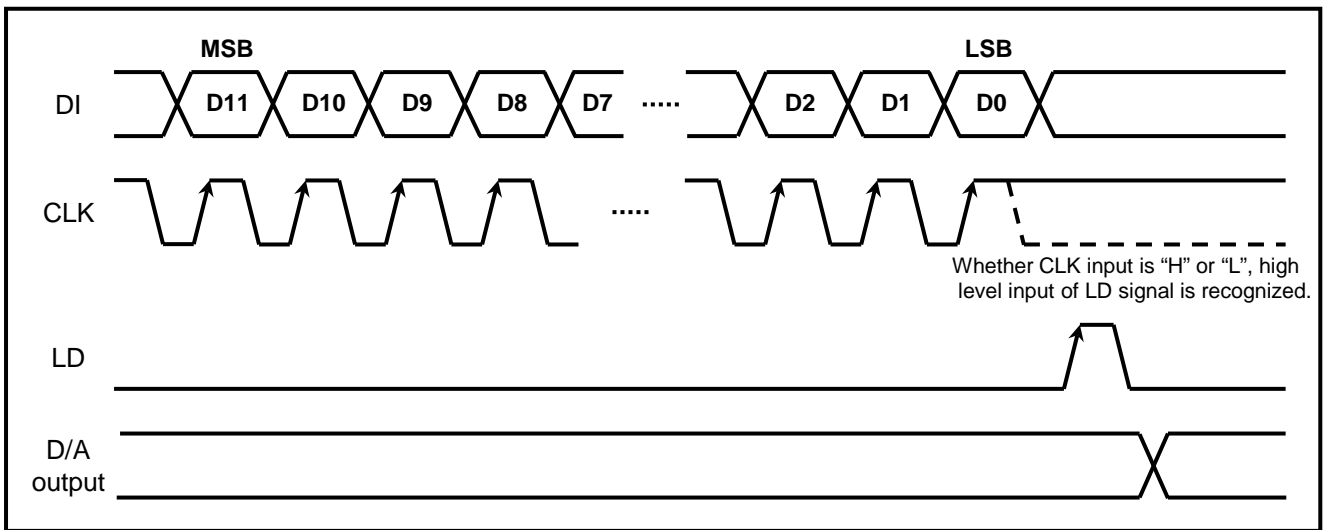
### Channel select data

| D8 | D9 | D10 | D11 | Chanel Selection |
|----|----|-----|-----|------------------|
| 0  | 0  | 0   | 0   | Don't care       |
| 0  | 0  | 0   | 1   | Ao1 select       |
| 0  | 0  | 1   | 0   | Ao2 select       |
| 0  | 0  | 1   | 1   | Ao3 select       |
| 0  | 1  | 0   | 0   | Ao4 select       |
| 0  | 1  | 0   | 1   | Ao5 select       |
| 0  | 1  | 1   | 0   | Ao6 select       |
| 0  | 1  | 1   | 1   | Ao7 select       |
| 1  | 0  | 0   | 0   | Ao8 select       |
| 1  | 0  | 0   | 1   | Ao9 select       |
| 1  | 0  | 1   | 0   | Ao10 select      |
| 1  | 0  | 1   | 1   | Ao11 select      |
| 1  | 1  | 0   | 0   | Ao12 select      |
| 1  | 1  | 0   | 1   | Don't care       |
| 1  | 1  | 1   | 0   | Don't care       |
| 1  | 1  | 1   | 1   | Don't care       |

### DAC data

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D/A Output   |
|----|----|----|----|----|----|----|----|--|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | $(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 1 + V_{\text{refL}}$   |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | $(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 2 + V_{\text{refL}}$   |
| 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | $(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 3 + V_{\text{refL}}$   |
| 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | $(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 4 + V_{\text{refL}}$   |
| :  | :  | :  | :  | :  | :  | :  | :  | :  |
| 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | $(V_{\text{refU}} - V_{\text{refL}}) / 256 \times 255 + V_{\text{refL}}$ |
| 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | $V_{\text{refU}}$  |

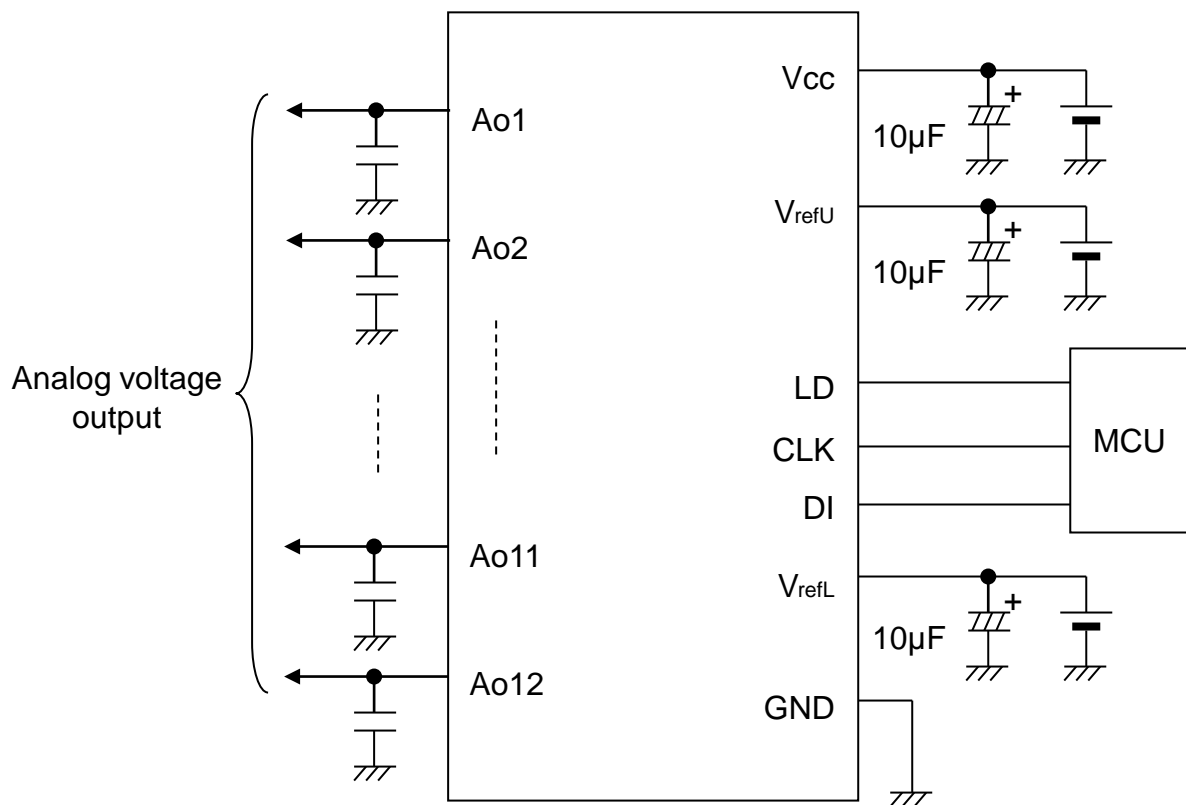
**Data Timing Chart ( Model )**



**Precaution For use**

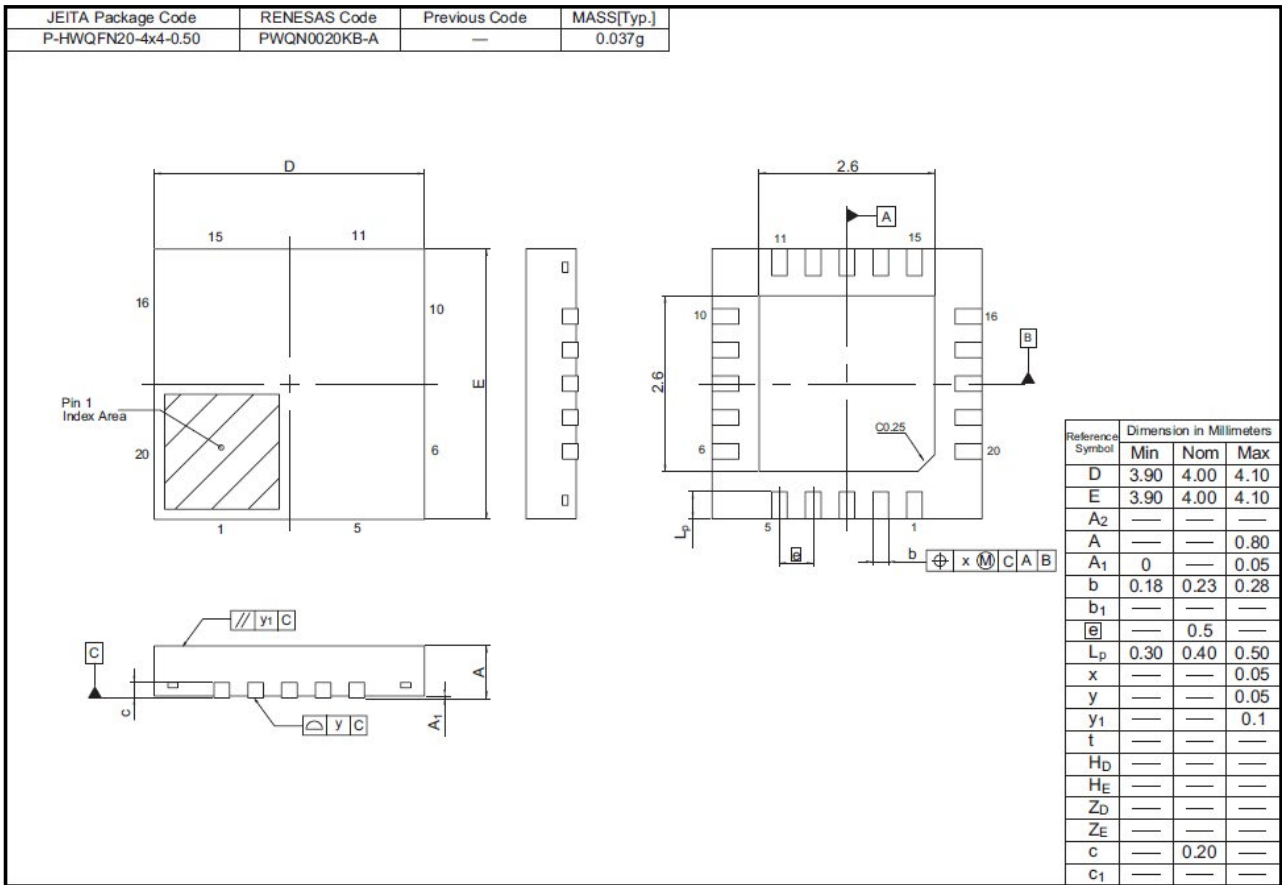
- There are three terminals ( $V_{CC}$ ,  $V_{refU}$ ,  $V_{refL}$ ) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals ( $V_{CC}$ ,  $V_{refU}$ ,  $V_{refL}$ ) and GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor ( 0.1 $\mu$ F Max ) among output to GND for every noise elimination.

**Standard Application Circuit**

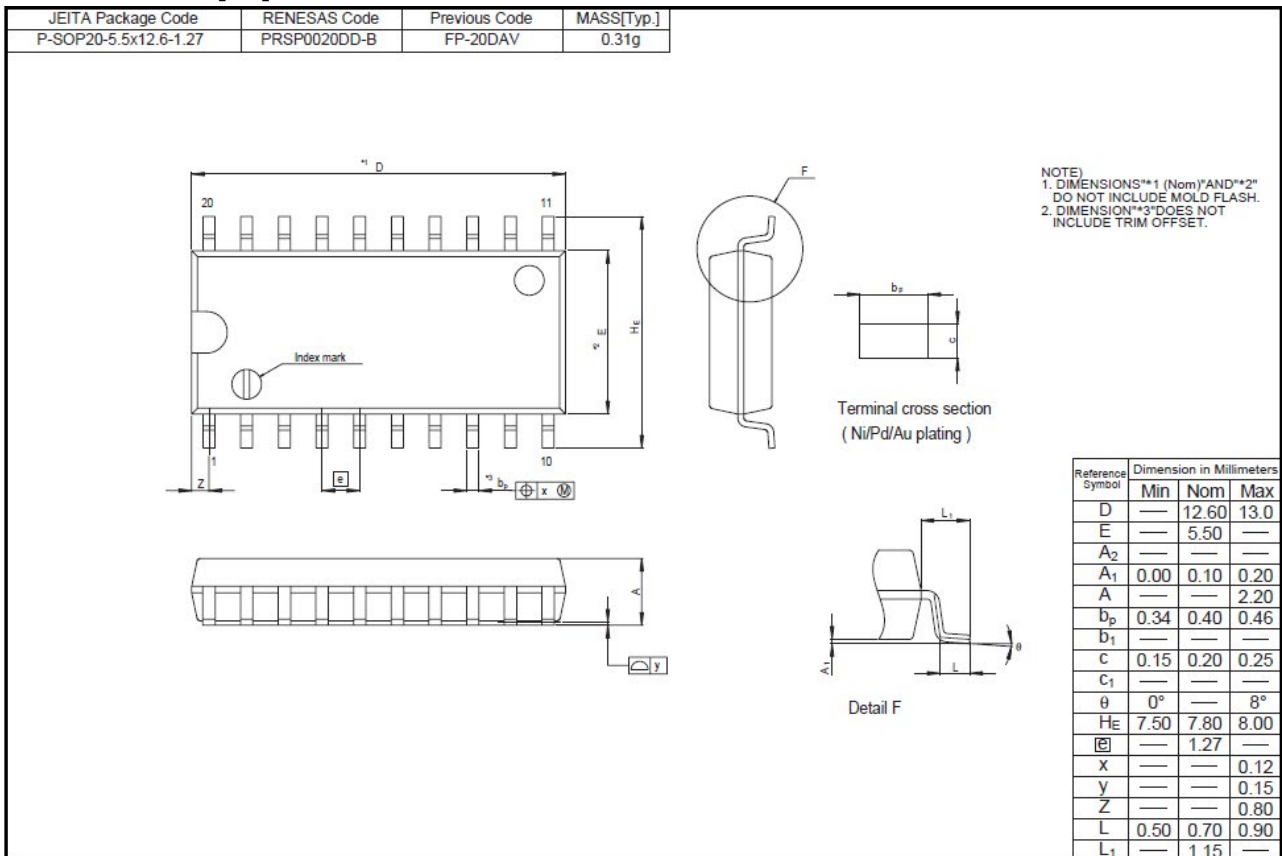


Package Dimensions

PWQN0020KB-A [NP]

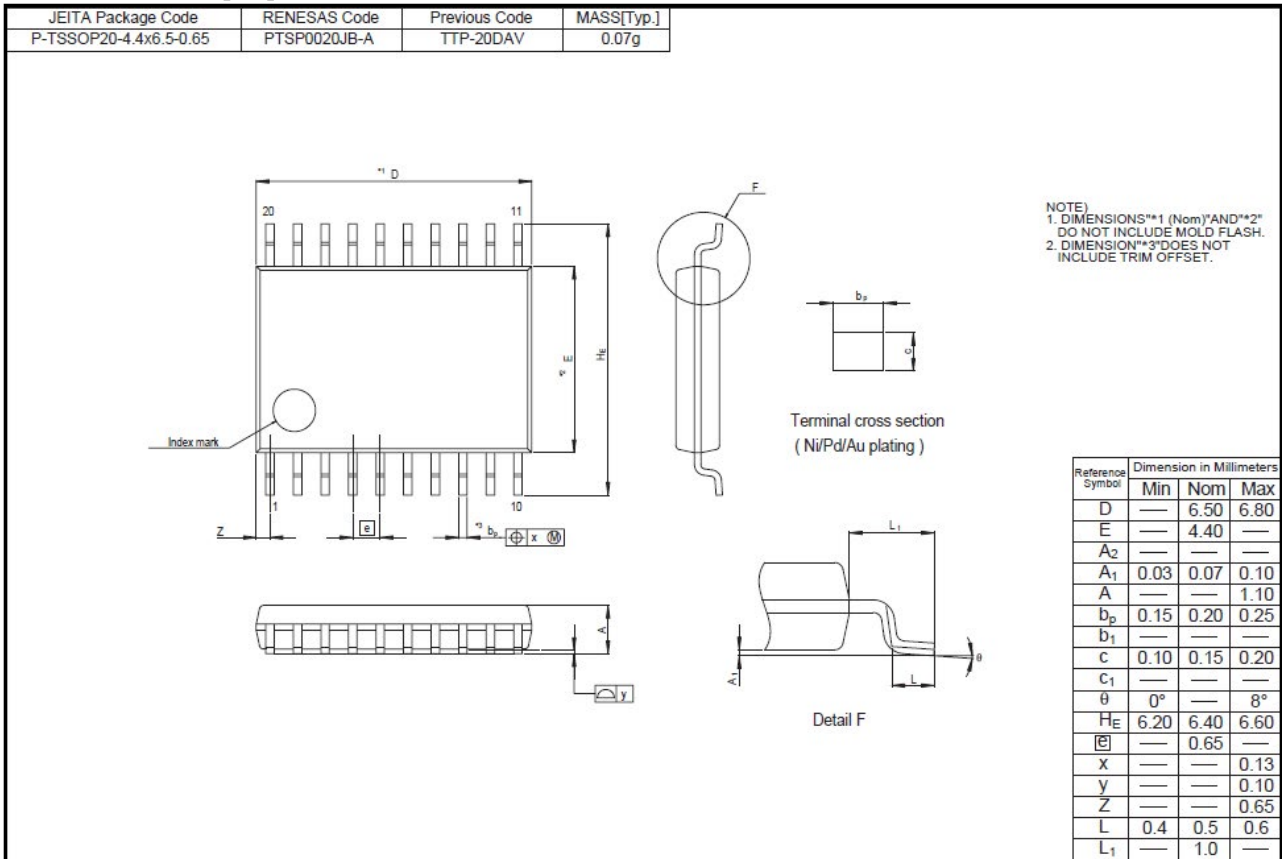


PRSP0020DD-B [SP]





**PTSP0020JB-A [SA]**



**Ordering Information**

| Order part No. | Package Name | Package Code | Package type No. | Packing/Quantity           |
|----------------|--------------|--------------|------------------|----------------------------|
| R2A20169SP#W5  | SOP-20       | PRSP0020DD-B | SP               | Embossed Taping/2,000 pcs. |
| R2A20169SA#W5  | TSSOP-20     | RTSP0020JB-A | SA               | Embossed Taping/2,000 pcs. |
| R2A20169NP#W5  | QFN-20       | PWQN0020KB-A | NP               | Embossed Taping/2,500 pcs. |

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