Hot Swappable I2C Bus/SMBus Buffer

Features

- Bidirectional buffer for SDA and SCL lines increases fan out
- Prevents SDA and SCL corruption during live board insertion and removal from backplane
- Isolates Input SDA and SCL Lines From Output
- Compatible with I2C, I2C Fast Mode and SMBus Standards (Up to 400kHz Operation)
- Built-in rise time accelerators on all SDA and SCL
- Wide Supply Voltage Range: 2.7V to 5.5V
- Active HIGH ENABLE input
- Active HIGH READY open-drain output
- High-impedance SDA and SCL pins for VCC = 0 V
- 1.1V pre-charge on all SDA and SCL lines
- Supporting clock stretching and multiple master arbitration/synchronization
- ESD protection exceeds 4000 V HBM per JESD22-A114
- Package offered:

  MSOP-8(U), UDFN-8(ZW), SOIC-8(W)

Pin Configuration

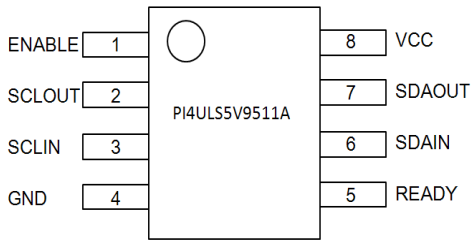


Figure 1. Top View of MSOP-8 and SOIC-8

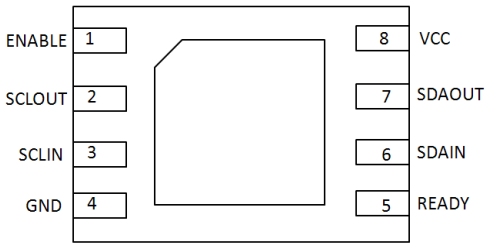


Figure 2. Top View of UDFN 2x3-8

Description

The PI6ULS5V9511A is a hot swappable I2C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PI6ULS5V-9511A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PI6ULS5V9511A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PI6ULS5V9511A incorporates a digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW, and an open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

During insertion, the PI6ULS5V9511A SDA and SCL lines are pre-charged to 1.1 V to minimize the current required to charge the parasitic capacitance of the chip.

Pin Description

Pin Name	Pin No.	Description
ENABLE	1	Chip enable.
SCLOUT	2	Serial clock output to and from the SCL bus on the card
SCLIN	3	Serial clock input to and from the SCL bus on the backplane
GND	4	Ground. Connect this pin to a ground plane for best results.
READY	5	Open-drain output .Goes LOW when SDA/SCL channels are disconnected, goes HIGH when the two sides are connected
SDAIN	6	Serial data input to and from the SDA bus on the backplane
SDAOUT	7	Serial data output to and from the SDA bus on the card
VCC	8	Power supply

Block Diagram

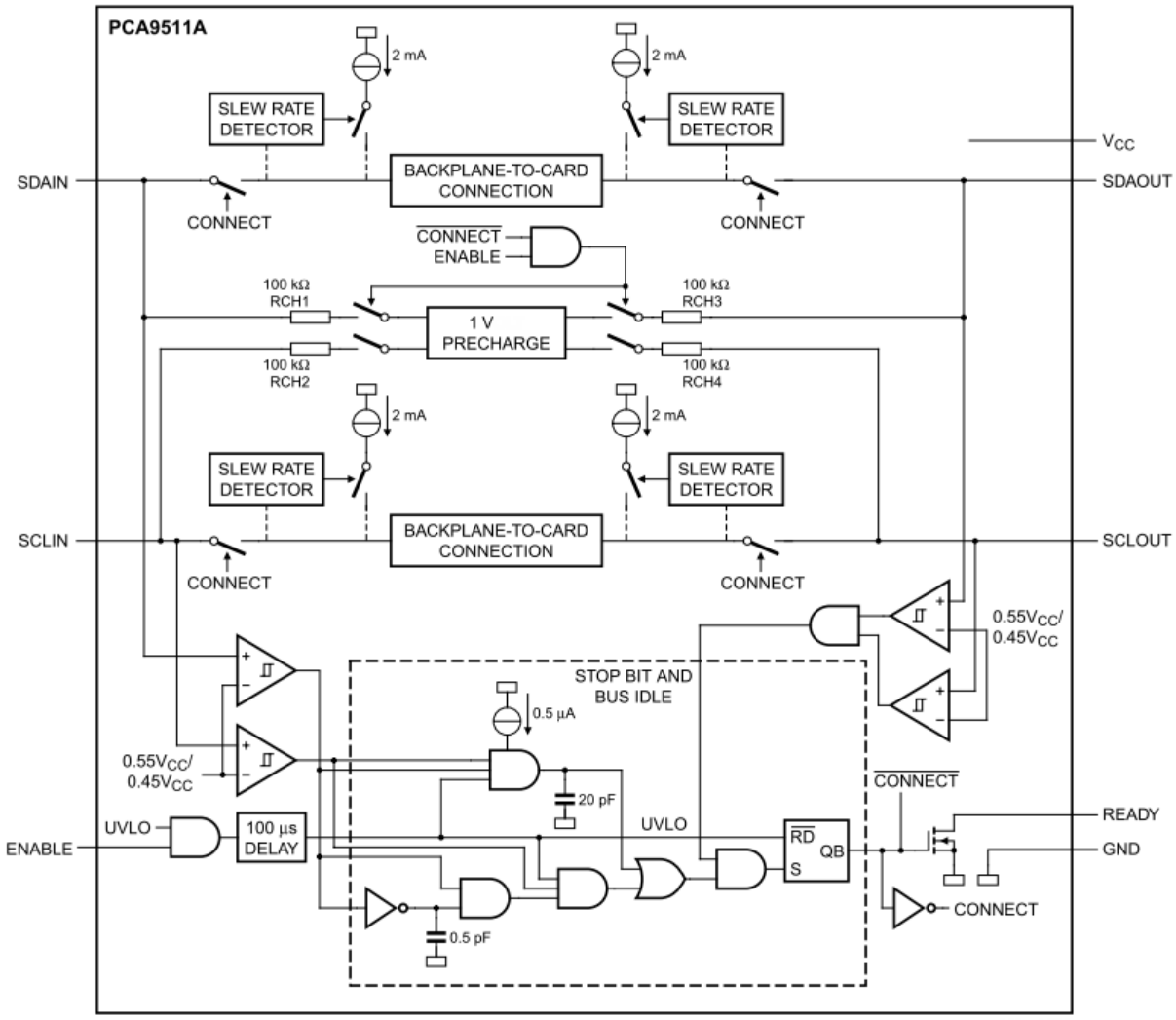


Figure 3: Block Diagram

Maximum Ratings

Supply Voltage .....–0.5V to +6.0V
DC Input Voltage ..... –0.5V to +6V
Control Input Voltage (EN) ..... –0.5V to +6V
Total power dissipation (1).....100mW
Input/output current(port 0&1).....50mA
Inputt current(EN ,VCC,GND).....50mA
ESD: HBM Mode 4000V
Storage Temperature .....–55℃ to +125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

V_{CC} = 2.7V to 5.5 V; GND = 0 V; Tamb=-40℃ to +85℃;unless otherwise specified

Symbol	Parameter	CONDITIONS	Min.	TYP	Max.	Unit
V_{CC}[1]	supply voltage port B		2.7		5.5	V
I_{CC}	supply current	VCC = 5.5 V; VSDAIN = VSCLIN = 0 V		2.8	6	mA
$I_{CC(sd)}$	Shut-down mode supply current	VENABLE = 0 V; all other pins at VCC or GND		0.1		uA

Note
[1] This specification applies over the full operating temperature range.

Electrical Characteristics

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; Tamb=-40℃ to +85℃; unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
Start-up circuitry						
V_{pch}[1]	Pre-charge voltage	SDA,SCL floating	0.8	1.1	1.2	V
$V_{IH(ENABLE)}$	HIGH-level input voltage on pin ENABLE			0.5*V_{CC}	0.7*V_{CC}	V
$V_{IL(ENABLE)}$	LOW-level input voltage on pin ENABLE		0.3 *V_{CC}	0.5 *V_{CC}		V
$I_{I(ENABLE)}$	Input current on pin ENABLE	V_{ENABLE} = 0 V to V_{CC}		±0.1	±1	uA
t_{en}[2]	Enable time			110		us
$t_{idle(READY)}$[1]	Bus idle time to READY active		50	105	200	us
$t_{dis(EN-RDY)}$	Disable time (ENABLE to READY)			30		ns
$t_{stp(READY)}$[3]	SDAIN to READY delay after STOP			1.2		us
t_{READY}[3]	SCLOUT/SDAOUT to READY delay			0.8		us
$I_{LZ(READY)}$	Off-state leakage current on pin READY	V_{ENABLE} = V_{CC}		±0.3		uA
$C_{i(ENABLE)}$[4]	Input capacitance on pin ENABLE	VI = V_{CC} or GND		1.9	4.0	pF
$C_{o(READY)}$[4]	LOW-level output voltage	VI = V_{CC} or GND		2.5	4.0	pF
$V_{OL(READY)}$[1]	LOW-level output voltage on pin READY	Ipu = 3 mA; V_{ENABLE} = V_{CC}			0.4	V

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
Rise time accelerators						
$I_{trt(pu)}$ [5][6]	Transient boosted pull-up current	Positive transition on SDA, SCL; V_{CC} = 2.7 V; slew rate = 1.25 V/µs	1	2	-	V
Input-output connection						
V_{offset} [1][7][8]	Offset voltage	10 kΩ to V_{CC} on SDA, SCL;V_{CC} = 3.3 V		110	175	mV
t_{PLH}	LOW to HIGH propagation delay	SCL to SCL and SDA to SDA;10 kΩ to V_{CC}; C_L = 100 pF each side		0		ns
t_{PHL}	HIGH to LOW propagation delay	SCL to SCL and SDA to SDA;10 kΩ to V_{CC}; C_L = 100 pF each side		70		ns
$C_{i(SCL/SDA)}$ [4]	SCL and SDA input capacitance			5	**7**	pF
V_{OL} [1]	LOW-level output voltage	V_I = 0V;SDAn,SCLn pins; I_{sink} = 3 mA; V_{CC} = 2.7 V	0		0.4	V
I_{LI}	Input leakage current	SDAn, SCLn pins; V_{CC} = 5.5 V	-1		+1	uA

Note:
[1] This specification applies over the full operating temperature range.
[2] The enable time can slow considerably for some parts when temperature is < −20 °C.
[3] Delays that can occur after ENABLE and/or idle times have passed.
[4] Guaranteed by design, not production tested.
[5] Itrt(pu) varies with temperature and VCC voltage.
[6] Input pull-up voltage should not exceed power supply voltage in operating mode because the rise time accelerator will clamp the voltage to the positive supply rail.
[7] The connection circuitry always regulates its output to a higher voltage than its input.
[8] Force V_{SDAIN} = V_{SCLIN} = 0.1 V, tie SDAOUT and SCLOUT through 10 kΩ resistor to VCC and measure the SDAOUT and SCLOUT output.

I2C Interface Timing Requirements

Symbol	Parameter	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
fscl	I2C clock frequency	0	100	0	400	kHz
t_{Low}	I2C clock high time	4.7		1.3		µs
t_{High}	I2C clock low time	4		0.6		µs
t_{SP}	I2C spike time		50		50	ns
$t_{SU:DAT}$	I2C serial-data setup time	250		100		ns
$t_{HD:DAT}$	I2C serial-data hold time	0 [1]		0 [1]		µs
tr	I2C input rise time		1000		300	ns
tf	I2C input fall time		300		300	ns
t_{BUF}	I2C bus free time between stop and start	4.7		1.3		µs
$t_{SU:STA}$	I2C start or repeated start condition setup	4.7		0.6		µs
$t_{HD:STA}$	I2C start or repeated start condition hold	4		0.6		µs
$t_{SU:STO}$	I2C stop condition setup	4		0.6		µs
$t_{VD:DAT}$	Valid-data time (high to low) [2] SCL low to SDA output low valid		1		1	µs
	Valid-data time (low to high) [2] SCL low to SDA output high valid		0.6		0.6	µs
$t_{VD:ACK}$	Valid-data time of ACK condition ACK signal from SCL low to SDA output low		1		1	µs
Cb	I2C bus capacitive load		400		400	pF

Notes:
[1] A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
[2] Data taken using a 1-kΩ pull up resistor and 50-pF load Notes

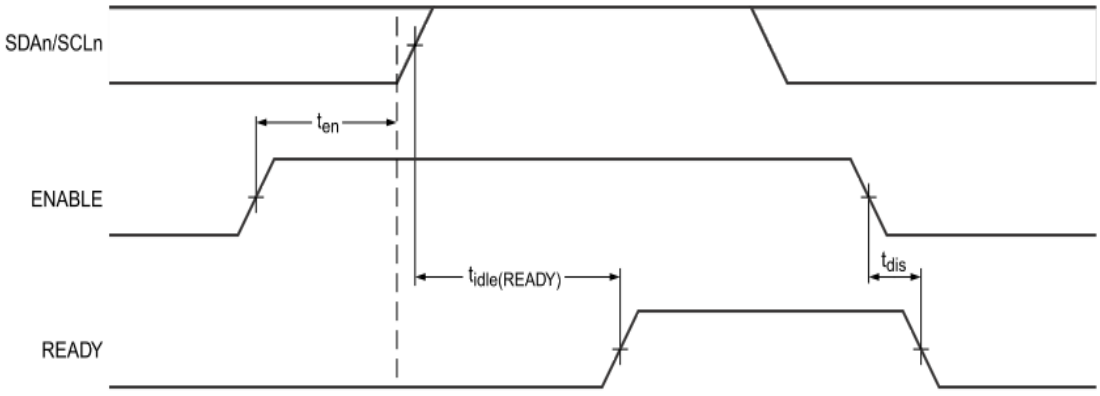
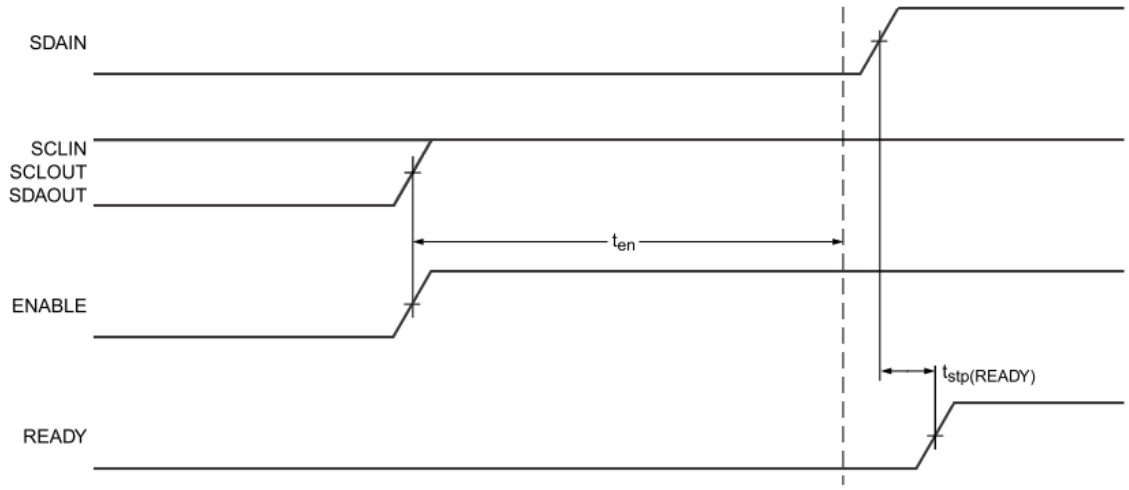
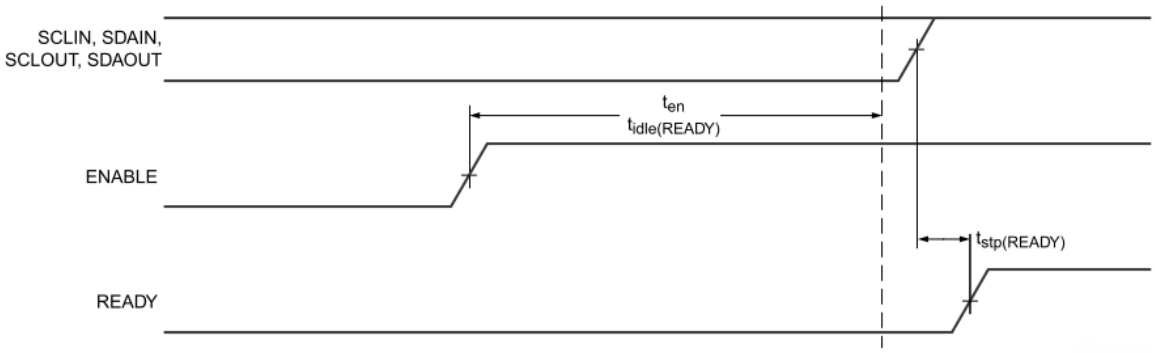


Figure 4. Timing for t_{en}, $t_{idle(READY)}$, and t_{dis}



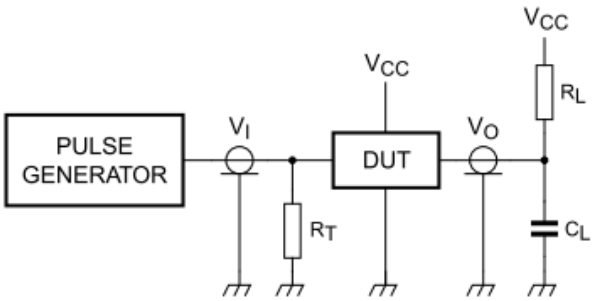
$t_{stp(READY)}$ is only applicable after the t_{en} delay.

Figure 5. $t_{stp(READY)}$ that can occur after t_{en}



$t_{stp(READY)}$ is only applicable after the t_{en} delay.

Figure 6. $t_{stp(READY)}$ delay that can occur after ten and $t_{idle(READY)}$



R_L = load resistor; 1.35 kΩ

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Figure 7: Test circuitry for switching times

Function Description

Start-Up

An undervoltage/initialization circuit holds the parts in a disconnected state which presents high-impedance to all SDA and SCL pins during power-up. A LOW on the ENABLE pin also forces the parts into the low current disconnected state when the ICC is essentially zero. As the power supply is brought up and the ENABLE is HIGH or the part is powered and the ENABLE is taken from LOW to HIGH it enters an initialization state where the internal references are stabilized and the precharge circuit is enabled. At the end of the initialization state the 'Stop Bit And Bus Idle' detect circuit is enabled. With the ENABLE pin HIGH long enough to complete the initialization state (ten) and remaining HIGH when all the SDA and SCL pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, SDAIN is connected to SDAOUT and SCLIN is connected to SCLOUT. The 1 V precharge circuitry is activated during the initialization and is deactivated when the connection is made. The precharge circuitry pulls up the SDA and SCL pins to 1 V through individual 100 kΩ nominal resistors. This precharges the pins to 1 V to minimize the worst case disturbances that result from inserting a card into the backplane where the backplane and the card are at opposite logic levels.

Connect Circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical with each acting as a bidirectional buffer that isolates the input capacitance from the output bus capacitance while communicating the logic levels. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the part. The same is also true for the SCL pins. Noise between 0.7VCC and VCC is generally ignored because a falling edge is only recognized when it falls below 0.7VCC with a slew rate of at least 1.25 V/µs. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load initially, because it does not start until the first falling pin is below 0.7VCC. The first falling pin may have a fast or slow slew rate, if it is faster than the pull down slew rate then the initial pull-down rate will continue. If the first falling pin has a slow slew rate then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first. Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same value for instance, 10 mV by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving that pin will rise until the internal driver pulls it down to the offset voltage. When the last external driver stops driving a LOW, that pin will rise up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/µs, when the pin voltage exceeds 0.6 V for the PI6ULS5V9511A, the rise time accelerator's circuits are turned on and the pull-down driver is turned off.

Maximum Number of Devices in Series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{offset}) is 0.150 V with a 10 kΩ pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is that the I2C-bus specification of 3 mA will produce $V_{OL} < 0.4$ V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming $V_{OL} = 0.1$ V and $V_{offset} = 0.1$ V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

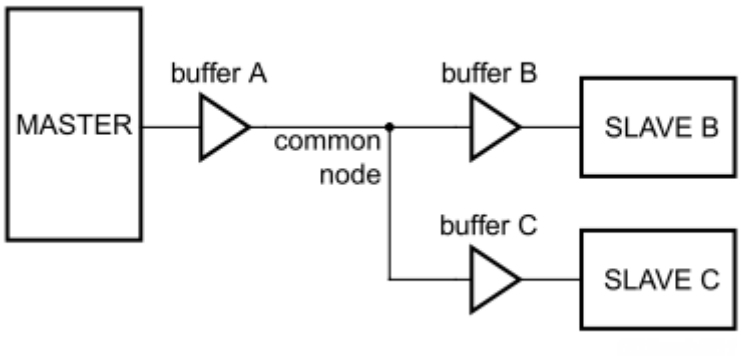


Figure 8: System with 3 buffers connected to common node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 8. Consider if the VOL at the input of buffer A is 0.3 V and the VOL of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe VIL at the input of buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of buffer B and buffer C would be -0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.5 V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

Propagation Delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same. The t_{PHL} can never be negative because the output does not start to fall until the input is below 0.7VCC, and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, VCC and process, as well as the load current and the load capacitance.

Rise Time Accelerators

During positive bus transitions a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PI6ULS5V9511A is exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators.

The built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines requires the bus pull-up voltage and supply voltage (VCC) to be the same.

READY Digital Output

This pin provides a digital flag which is LOW when either ENABLE is LOW or the start-up sequence described earlier in this section has not been completed. READY goes HIGH when ENABLE is HIGH and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3 mA while holding 0.4 V on the pin. Connect a resistor of 10 kΩ to VCC to provide the pull-up.

ENABLE Low Current Disable

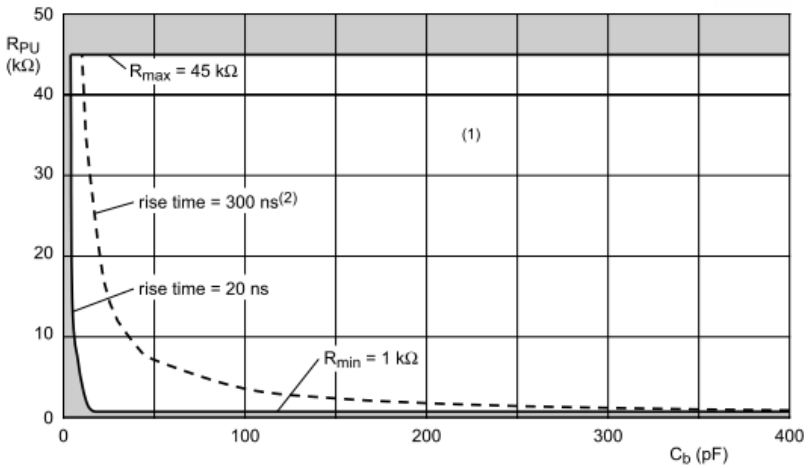
Grounding the ENABLE pin disconnects the backplane side from the card side, disables the rise time accelerators, drives READY LOW, disables the bus precharge circuitry, and puts the part in a low current state. When the pin voltage is driven all the way to VCC, the part waits for data transactions on both the backplane and card sides to be complete before reconnecting the two sides.

Resistor Pull-up Value Selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula in bellow.

$$R \leq 800 \times 10^3 (\frac{VCC(\min) - 0.6}{C})$$

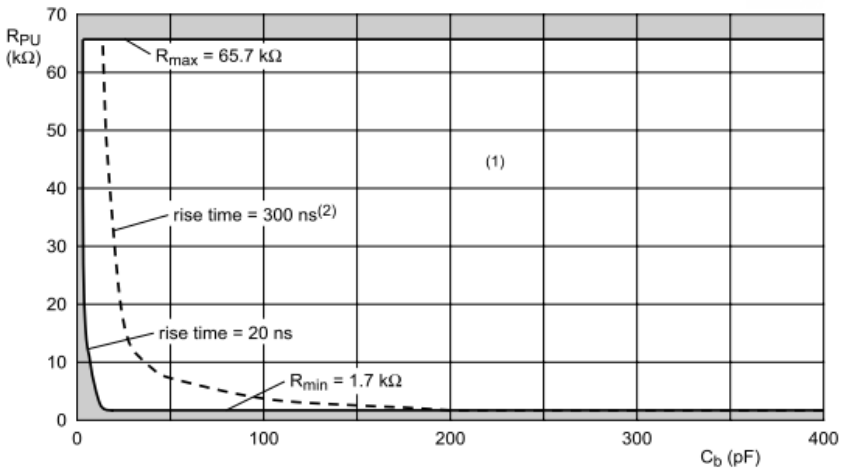
Where R is the pull-up resistor value in Ω, VCC(min) is the minimum VCC voltage in volts, and C is the equivalent bus capacitance in picofarads (pF). In addition, regardless of the bus capacitance, always choose R ≤ 65.7 kΩ for VCC = 5.5 V maximum, R ≤ 45 kΩ for VCC = 3.6 V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage.



(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with PI6ULS5V9511A.

(2) Rise time without PI6ULS5V9511A.

Figure 9. Bus requirements for 3.3 V systems



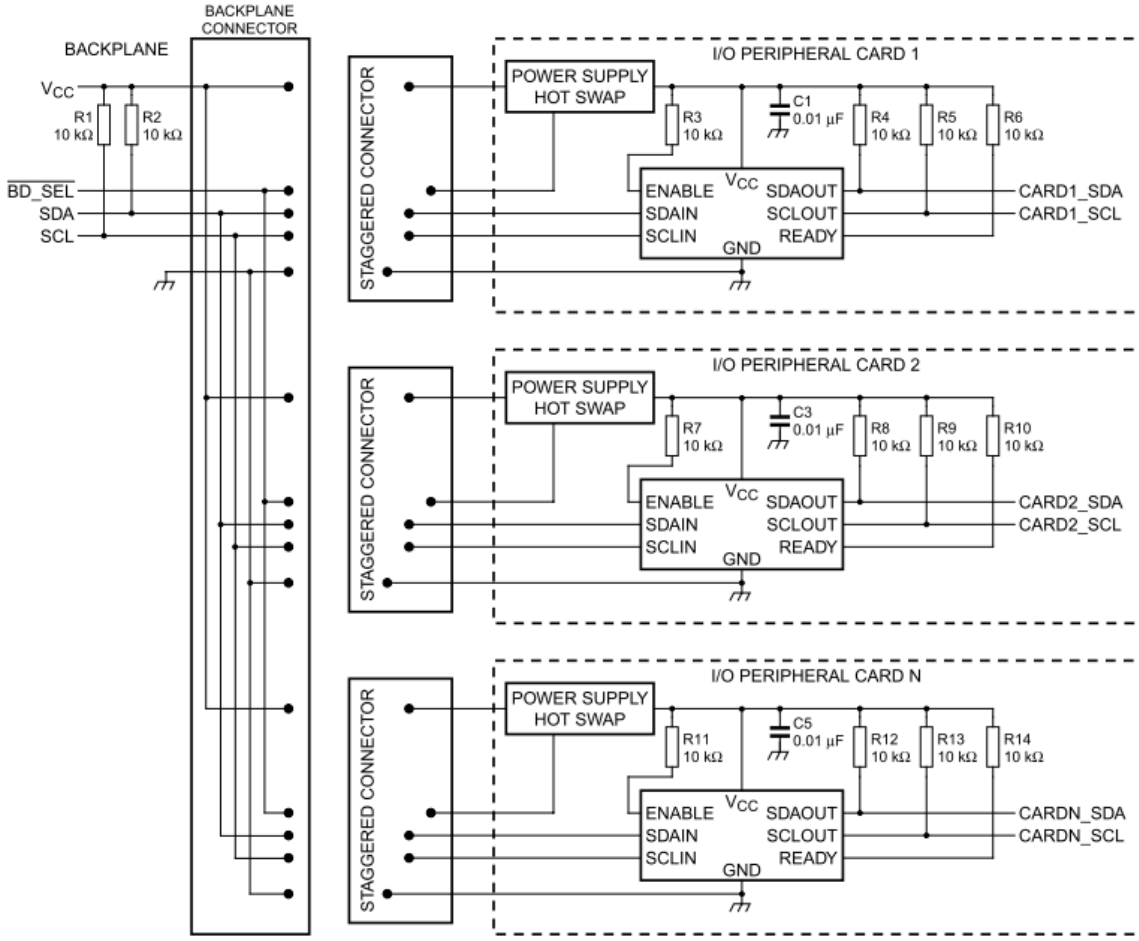
(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with PI6ULS5V9511A.

(2) Rise time without PI6ULS5V9511A.

Figure 10. Bus requirements for 5 V systems

Hot Swapping and Capacitance Buffering Application

Figure 11 through Figure 14 illustrate the usage of the PI6ULS5V9511A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PI6ULS5V9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.



Remark: The PI6ULS5V9511A can be used in any combination depending on the number of rise time accelerators that are needed by the system. Normally only one PI6ULS5V9511A would be required per bus.

Figure 11. Hot Swapping multiple I/O Cards into a Backplane using the PI6ULS5V9511A in a cPCI, VME and Advanced TCA System

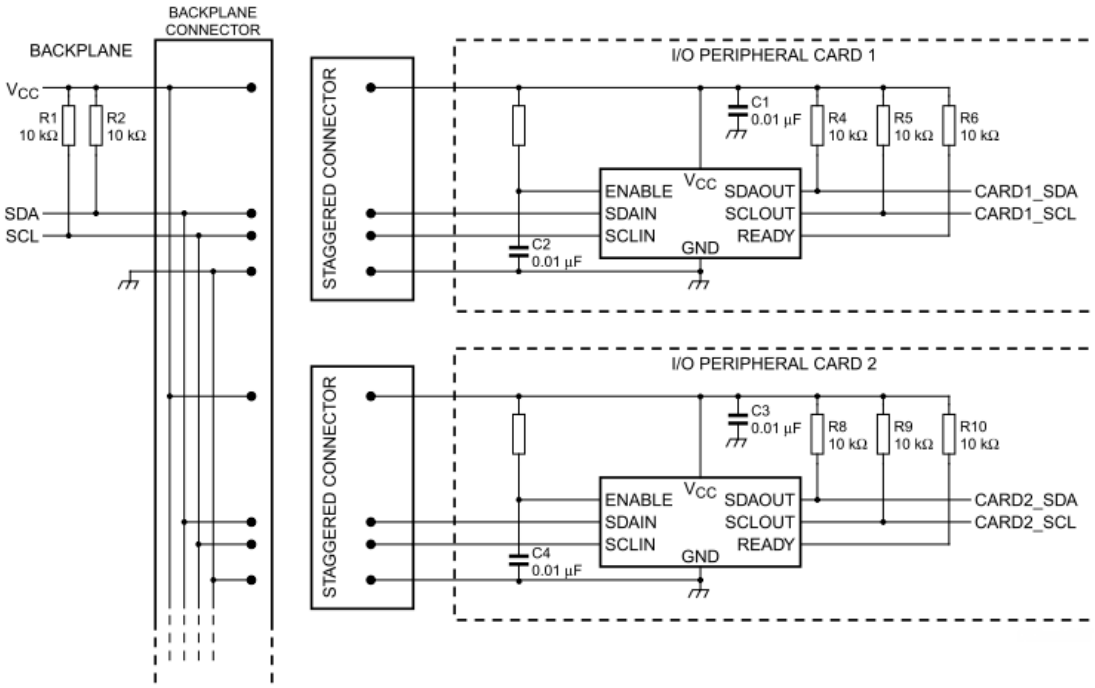


Figure 12. Hot Swapping Multiple I/O Cards into a Backplane Using the PI6ULS5V9511A in a PCI System

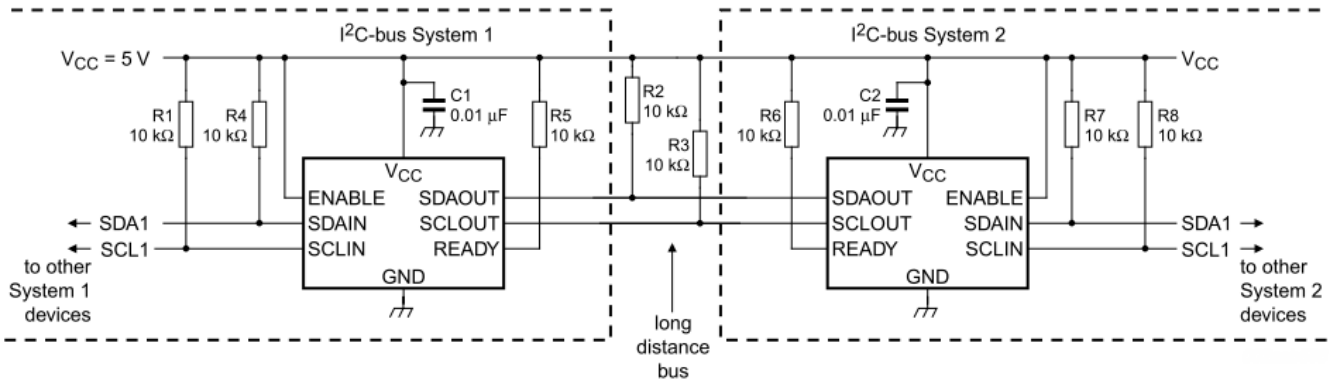
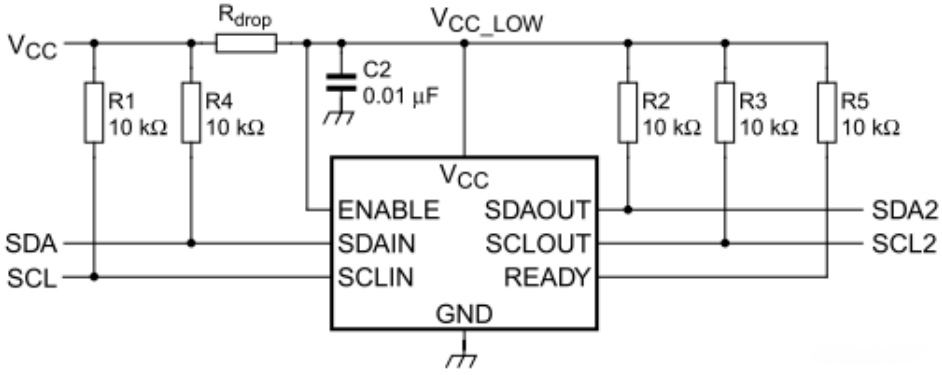


Figure13. Repeater / Bus Extender Application using the PI6ULS5V9511A



$V_{CC} > V_{CC\_LOW}$

R_{drop} is the line loss of V_{CC} in the backplane.

Figure 14. System with Disparate V_{CC} Voltages

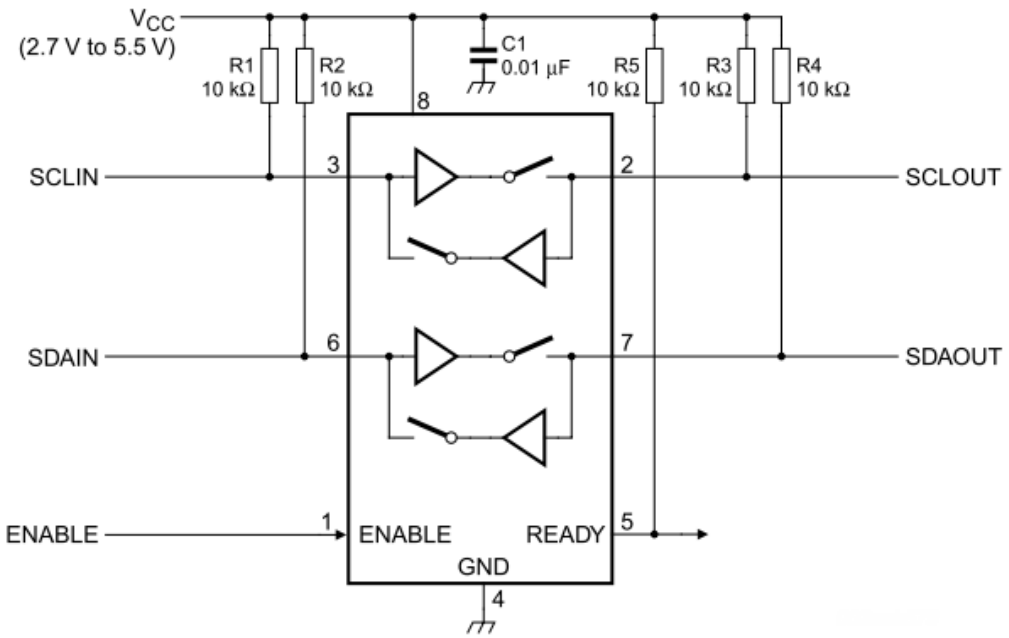
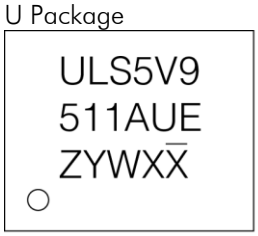


Figure 15. Typical A

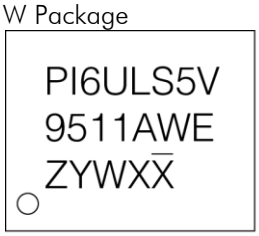
Part Marking

U Package



Z: Die Rev
YW: Year & Work week
1st X: Assembly Code
2nd X: Wafer Fab site Code

W Package



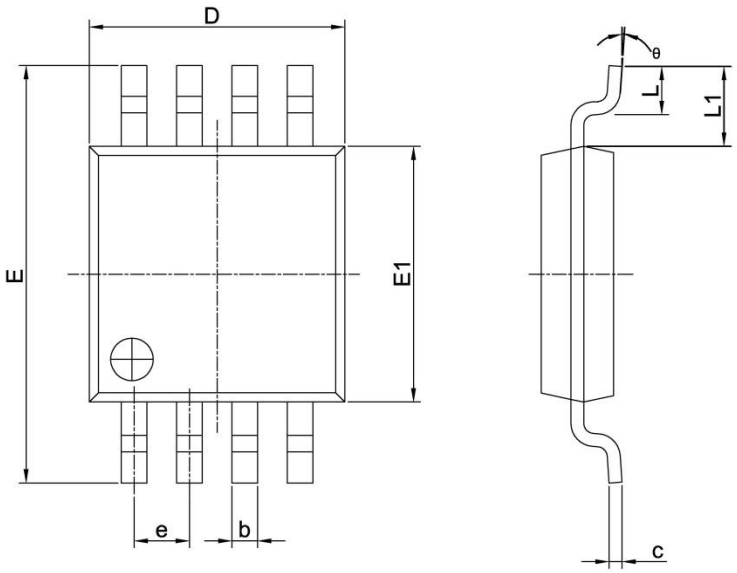
Z: Die Rev
YW: Year & Work week
1st X: Assembly Code
2nd X: Wafer Fab site Code

ZW Package

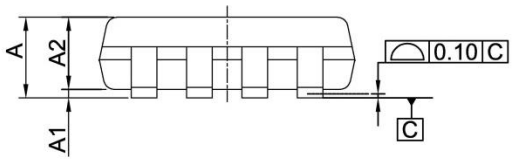
Z: Die Rev
YW: Year & Work week
1st X: Assembly Code
2nd X: Wafer Fab site Code

Packaging Mechanical

MSOP-8 (U)



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

DATE: 11/03/16

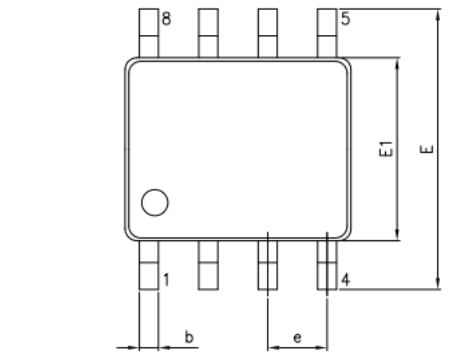
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

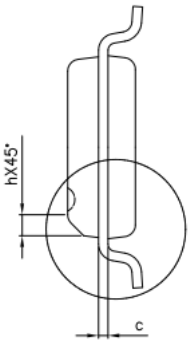
PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: G

16-0242

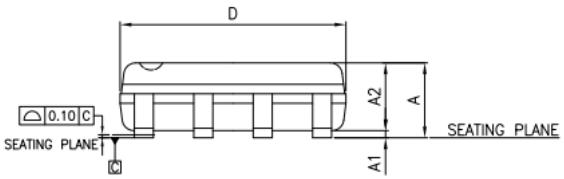
SOIC-8 (W)

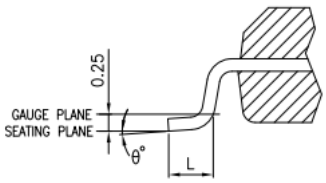




SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm





NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity

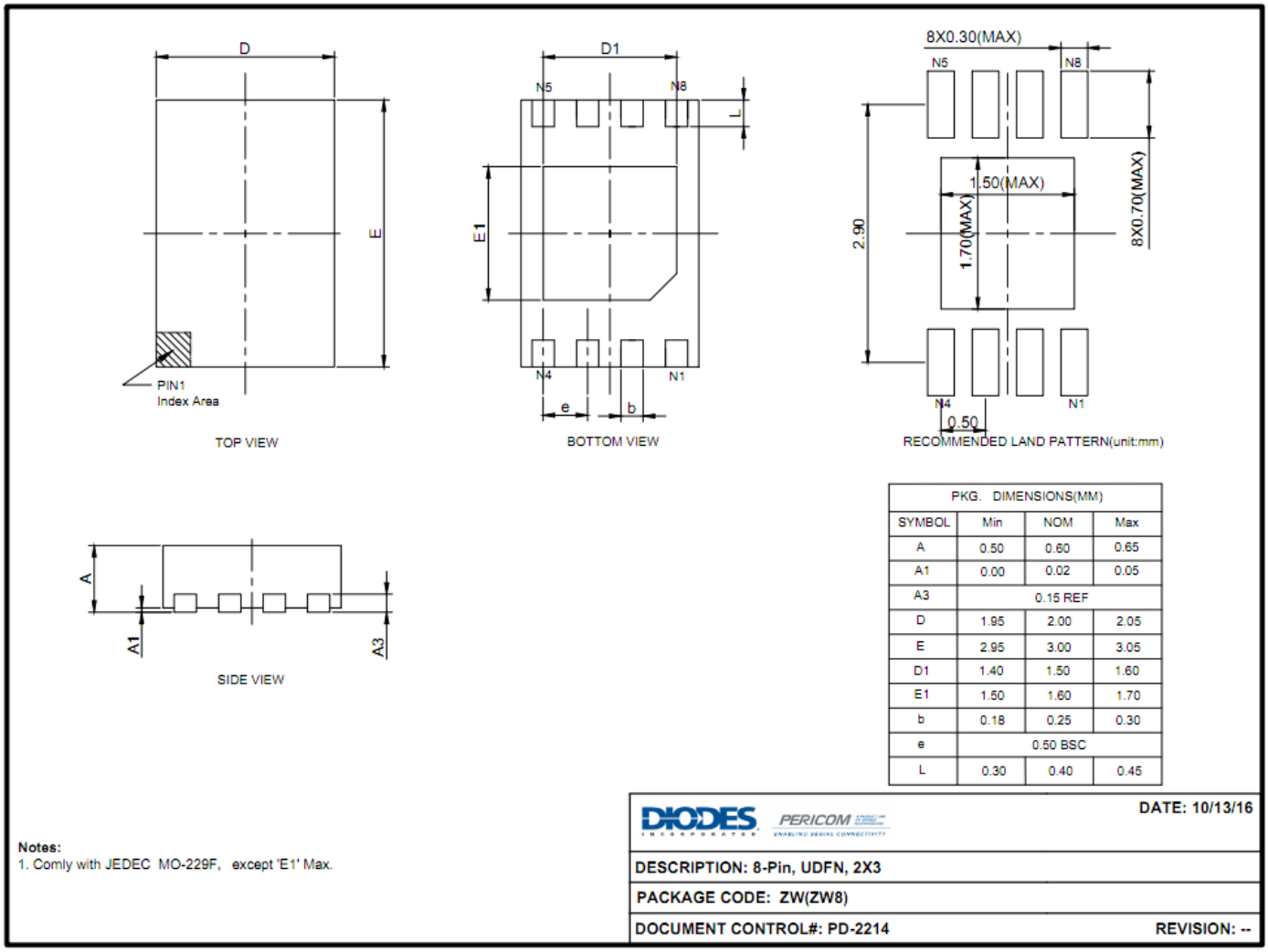
DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: G

UDFN-8 (ZW)



PKG. DIMENSIONS(MM)			
SYMBOL	Min	NOM	Max
A	0.50	0.60	0.65
A1	0.00	0.02	0.05
A3		0.15 REF	
D	1.95	2.00	2.05
E	2.95	3.00	3.05
D1	1.40	1.50	1.60
E1	1.50	1.60	1.70
b	0.18	0.25	0.30
e		0.50 BSC	
L	0.30	0.40	0.45

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Numbers	Package Code	Package
PI6ULS5V9511AUEX	U	8-Pin, Mini Small Outline Package (MSOP)
PI6ULS5V9511AWEX	W	8-Pin, 150mil-Wide (SOIC)
PI6ULS5V9511AZWEX	ZW	8-Pin, 2x3 (UDFN)

Notes:

- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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