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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: [info@chipsmall.com](mailto:info@chipsmall.com) Web: [www.chipsmall.com](http://www.chipsmall.com)

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# STD95N4F3 STP95N4F3 - STU95N4F3

N-channel 40V - 5.4mΩ - 80A - DPAK - TO-220 - IPAK  
STripFET™ Power MOSFET

## Features

| Type      | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> | P <sub>w</sub> |
|-----------|------------------|---------------------|----------------|----------------|
| STD95N4F3 | 40V              | <6.5mΩ              | 80A            | 110W           |
| STP95N4F3 | 40V              | <6.5mΩ              | 80A            | 110W           |
| STU95N4F3 | 40V              | <6.5mΩ              | 80A            | 110W           |

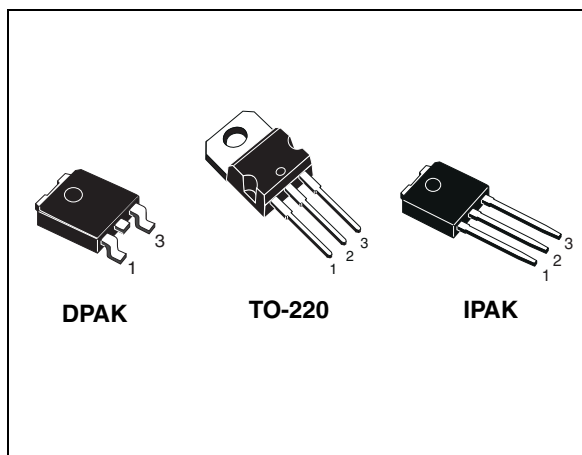
- Standard threshold drive
- 100% avalanche tested

## Description

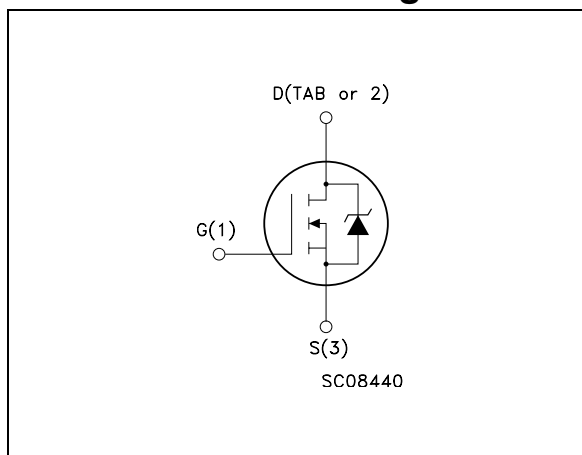
This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics unique "Single Feature Size™" strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

## Applications

- Switching application
  - Automotive



## Internal schematic diagram



## Order codes

| Part number | Marking | Package | Packaging   |
|-------------|---------|---------|-------------|
| STD95N4F3   | 95N4F3  | DPAK    | Tape & reel |
| STP95N4F3   | 95N4F3  | TO-220  | Tube        |
| STU95N4F3   | 95N4F3  | IPAK    | Tube        |

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol             | Parameter                                               | Value      | Unit |
|--------------------|---------------------------------------------------------|------------|------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS}=0$ )                     | 40         | V    |
| $V_{GS}$           | Gate-source voltage                                     | $\pm 20$   | V    |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25^\circ\text{C}$  | 80         | A    |
| $I_D$              | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 65         | A    |
| $I_{DM}^{(2)}$     | Drain current (pulsed)                                  | 320        | A    |
| $P_{TOT}$          | Total dissipation at $T_C = 25^\circ\text{C}$           | 110        | W    |
|                    | Derating factor                                         | 0.73       | W/°C |
| $dv/dt^{(3)}$      | Peak diode recovery voltage slope                       | 8          | V/ns |
| $E_{AS}^{(4)}$     | Single pulse avalanche energy                           | 400        | mJ   |
| $T_j$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature   | -55 to 175 | °C   |

1. Current limited by package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 80\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{jmax}$
4. Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 40\text{ A}$ ,  $V_{DD} = 30\text{ V}$

**Table 2. Thermal resistance**

| Symbol              | Parameter                                      | Value  |      |      | Unit |
|---------------------|------------------------------------------------|--------|------|------|------|
|                     |                                                | TO-220 | IPAK | DPAK |      |
| $R_{thj-case}$      | Thermal resistance junction-case max           | 1.36   |      |      | °C/W |
| $R_{thj-a}$         | Thermal resistance junction-ambient max        | 62.5   | 100  | --   | °C/W |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-ambient max        | --     | --   | 50   | °C/W |
| $T_l$               | Maximum lead temperature for soldering purpose | 300    | 275  | --   | °C   |

1. When mounted on 1inch<sup>2</sup> FR-4 2Oz Cu board

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. Static**

| Symbol        | Parameter                                        | Test conditions                                                                              | Min. | Typ. | Max.      | Unit                           |
|---------------|--------------------------------------------------|----------------------------------------------------------------------------------------------|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 250\mu\text{A}$ , $V_{GS} = 0$                                                        | 40   |      |           | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{Max rating}$ ,<br>$V_{DS} = \text{Max rating}$ , $T_c = 125^{\circ}\text{C}$ |      |      | 10<br>100 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{V}$                                                                    |      |      | $\pm 200$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$                                                   | 2    |      | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{V}$ , $I_D = 40\text{A}$                                                   |      | 5.4  | 6.5       | m $\Omega$                     |

**Table 4. Dynamic**

| Symbol         | Parameter                    | Test conditions                                           | Min | Typ. | Max. | Unit |
|----------------|------------------------------|-----------------------------------------------------------|-----|------|------|------|
| $g_{fs}^{(1)}$ | Forward transconductance     | $V_{DS} = 25\text{V}$ , $I_D = 40\text{A}$                |     | 100  |      | S    |
| $C_{iss}$      | Input capacitance            | $V_{DS} = 25\text{V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$ |     | 2200 |      | pF   |
| $C_{oss}$      | Output capacitance           |                                                           |     | 580  |      | pF   |
| $C_{rss}$      | Reverse transfer capacitance |                                                           |     | 40   |      | pF   |
| $Q_g$          | Total gate charge            | $V_{DD} = 20\text{V}$ , $I_D = 80\text{A}$                |     | 40   | 54   | nC   |
| $Q_{gs}$       | Gate-source charge           | $V_{GS} = 10\text{V}$                                     |     | 11   |      | nC   |
| $Q_{gd}$       | Gate-drain charge            | (see Figure 13)                                           |     | 8    |      | nC   |

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%



**Table 5. Switching on/off (inductive load)**

| Symbol                | Parameter                        | Test conditions                                                                 | Min. | Typ.     | Max. | Unit     |
|-----------------------|----------------------------------|---------------------------------------------------------------------------------|------|----------|------|----------|
| $t_{d(on)}$<br>$t_r$  | Turn-on delay time<br>Rise time  | $V_{DD}=20V$ , $I_D=40A$ ,<br>$R_G=4.7\Omega$ , $V_{GS}=10V$<br>(see Figure 15) |      | 15<br>50 |      | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off delay time<br>Fall time | $V_{DD}=20V$ , $I_D=40A$ ,<br>$R_G=4.7\Omega$ , $V_{GS}=10V$<br>(see Figure 15) |      | 40<br>15 |      | ns<br>ns |

**Table 6. Source drain diode**

| Symbol                            | Parameter                                                                    | Test conditions                                                                                 | Min. | Typ.            | Max.      | Unit          |
|-----------------------------------|------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|------|-----------------|-----------|---------------|
| $I_{SD}$<br>$I_{SDM}^{(1)}$       | Source-drain current<br>Source-drain current (pulsed)                        |                                                                                                 |      |                 | 80<br>320 | A<br>A        |
| $V_{SD}^{(2)}$                    | Forward on voltage                                                           | $I_{SD}=80A$ , $V_{GS}=0$                                                                       |      |                 | 1.5       | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}=80A$ ,<br>$di/dt = 100A/\mu s$ ,<br>$V_{DD}=30V$ , $T_J=150^\circ C$<br>(see Figure 14) |      | 45<br>60<br>2.8 |           | ns<br>nC<br>A |

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 $\mu s$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

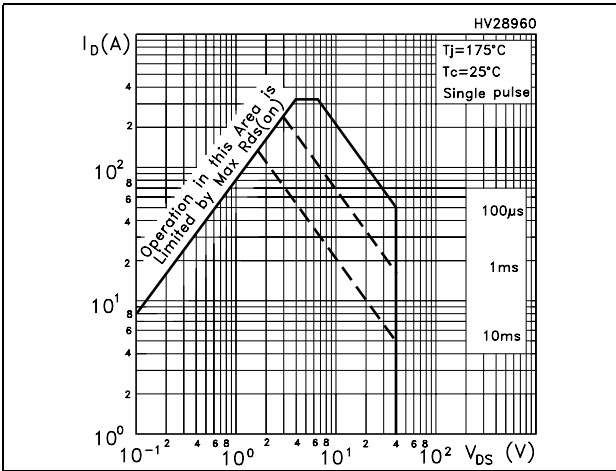


Figure 2. Thermal impedance

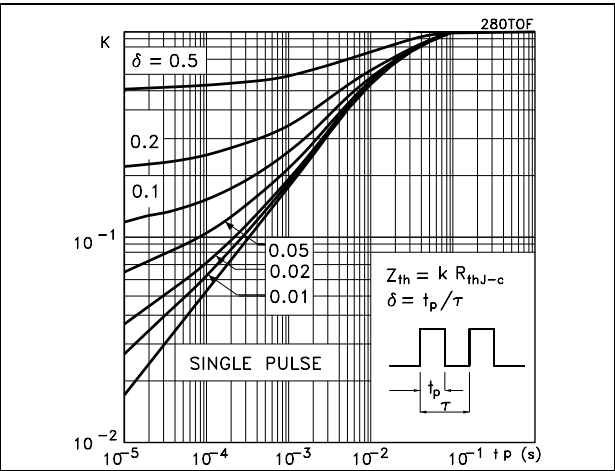


Figure 3. Output characteristics

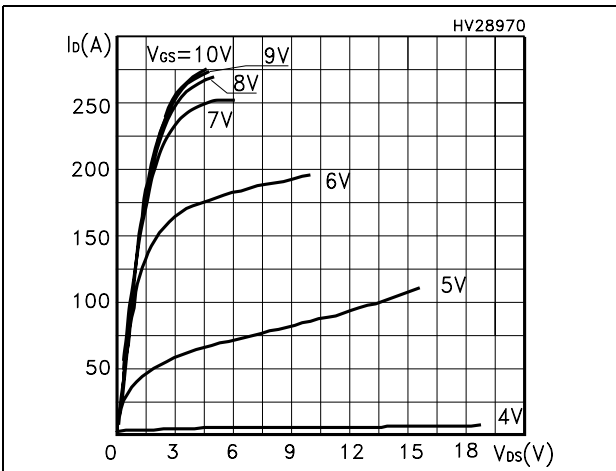


Figure 4. Transfer characteristics

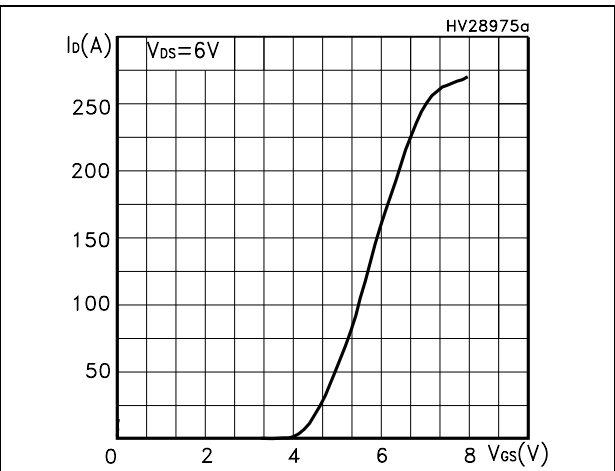


Figure 5. Static drain-source on resistance

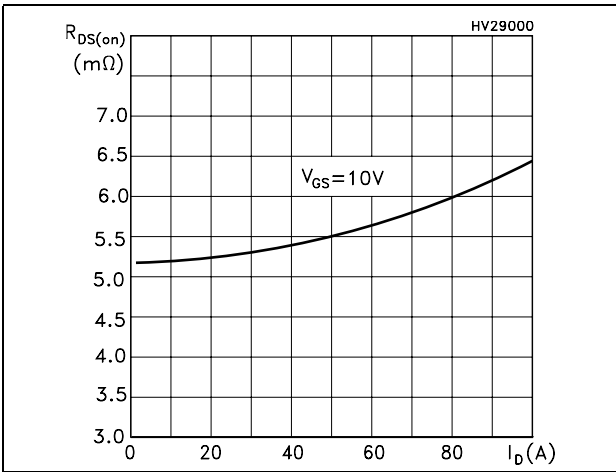


Figure 6. Normalized BVDSS vs temperature

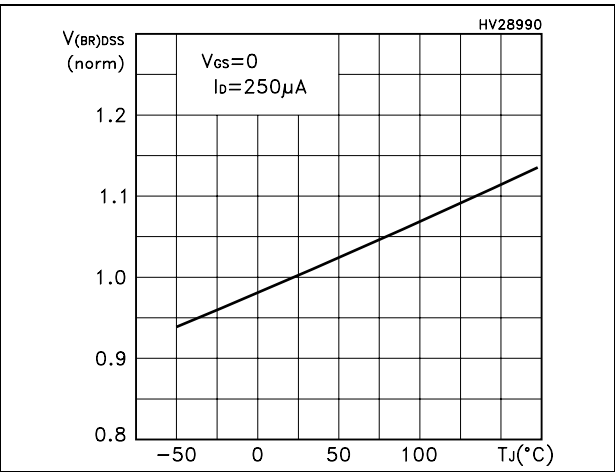


Figure 7. Gate charge vs gate-source voltage      Figure 8. Capacitance variations

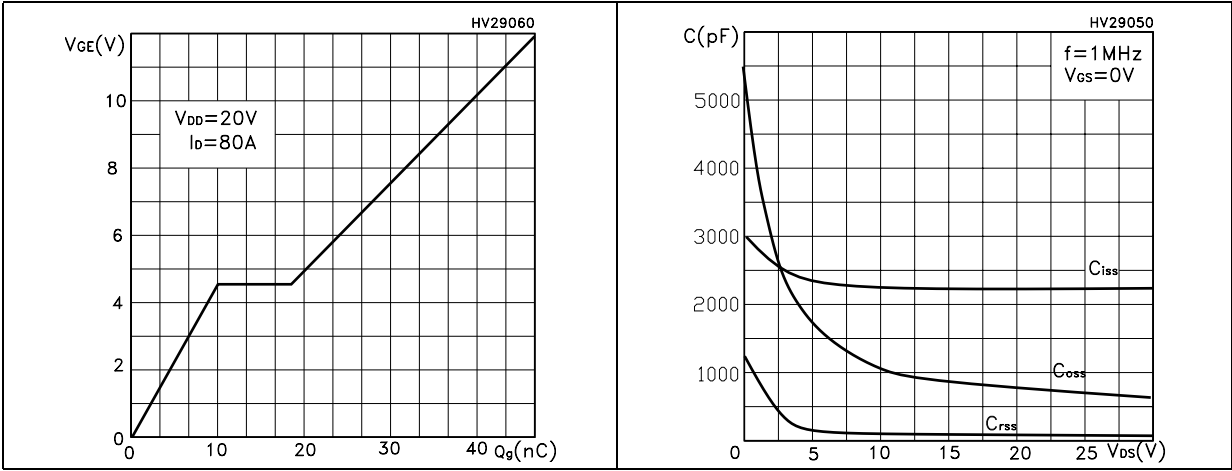


Figure 9. Normalized gate threshold voltage vs temperature      Figure 10. Normalized on resistance vs temperature

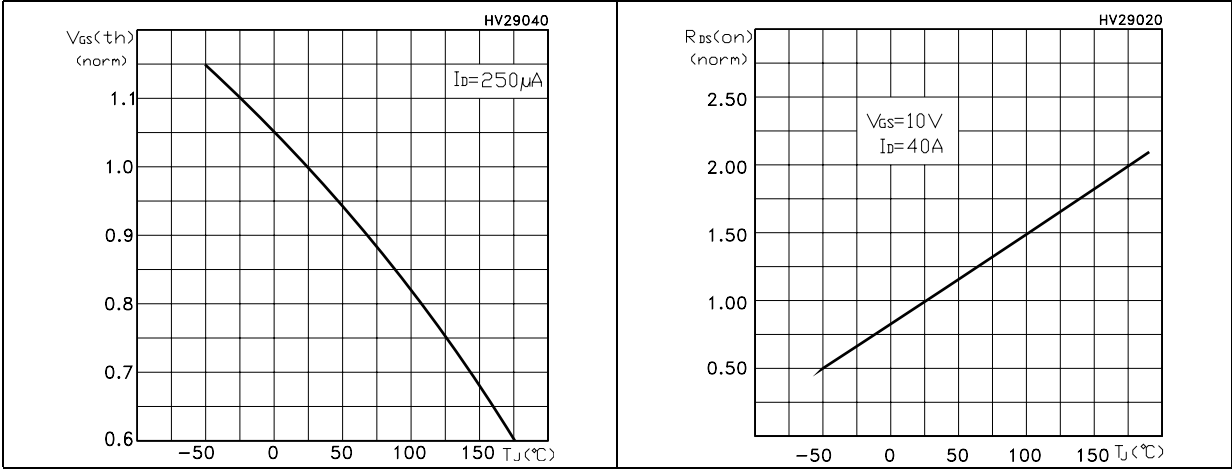
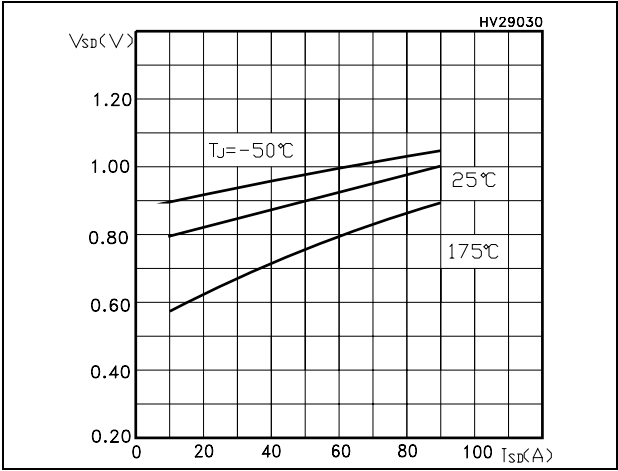


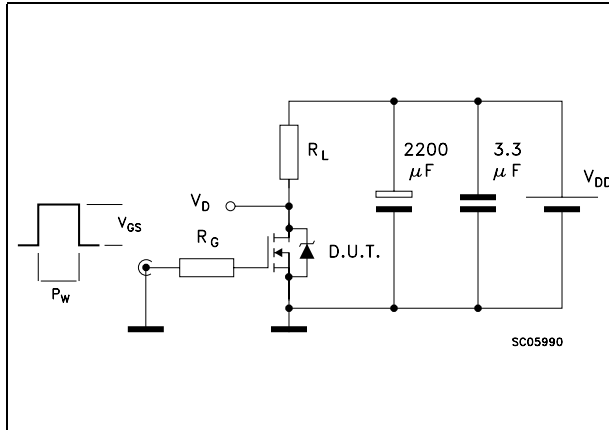
Figure 11. Source-drain diode forward characteristics



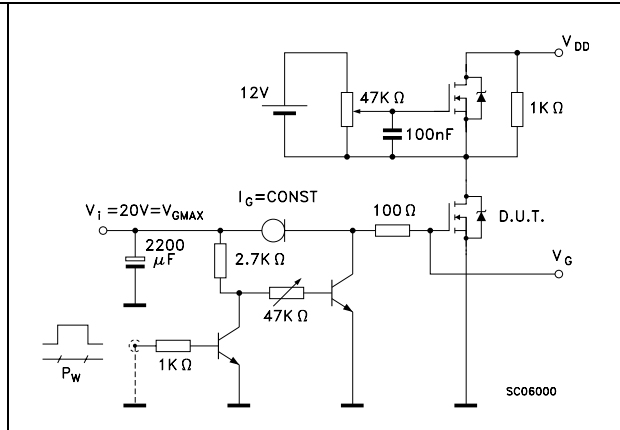


### 3 Test circuit

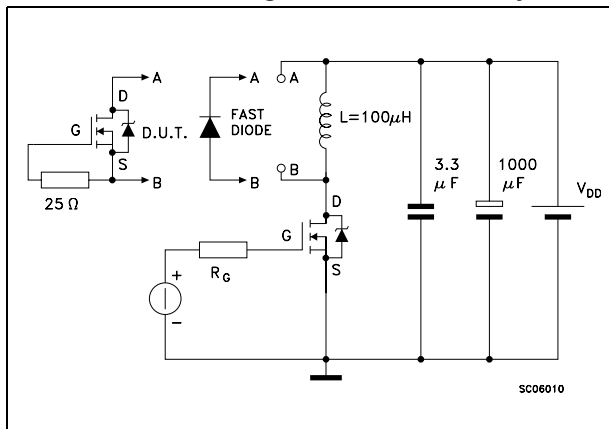
**Figure 12. Switching times test circuit for resistive load**



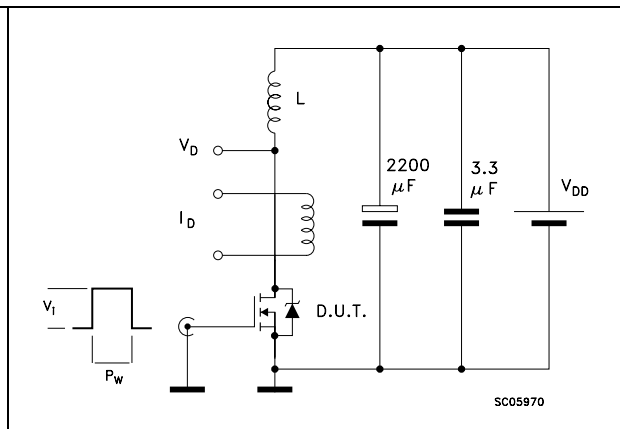
**Figure 13. Gate charge test circuit**



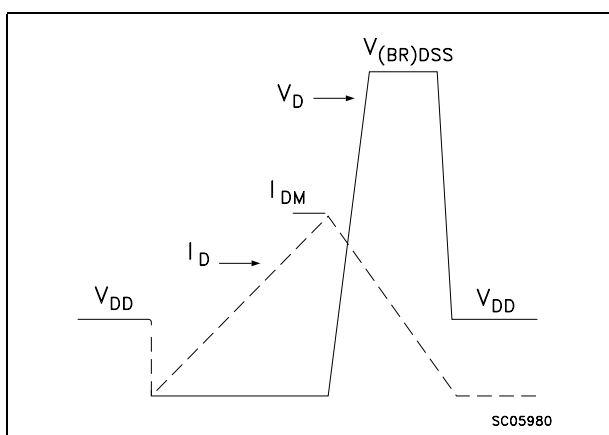
**Figure 14. Test circuit for inductive load switching and diode recovery times**



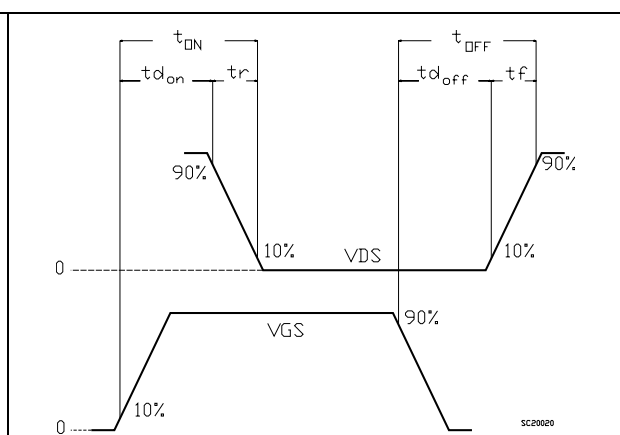
**Figure 15. Unclamped Inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

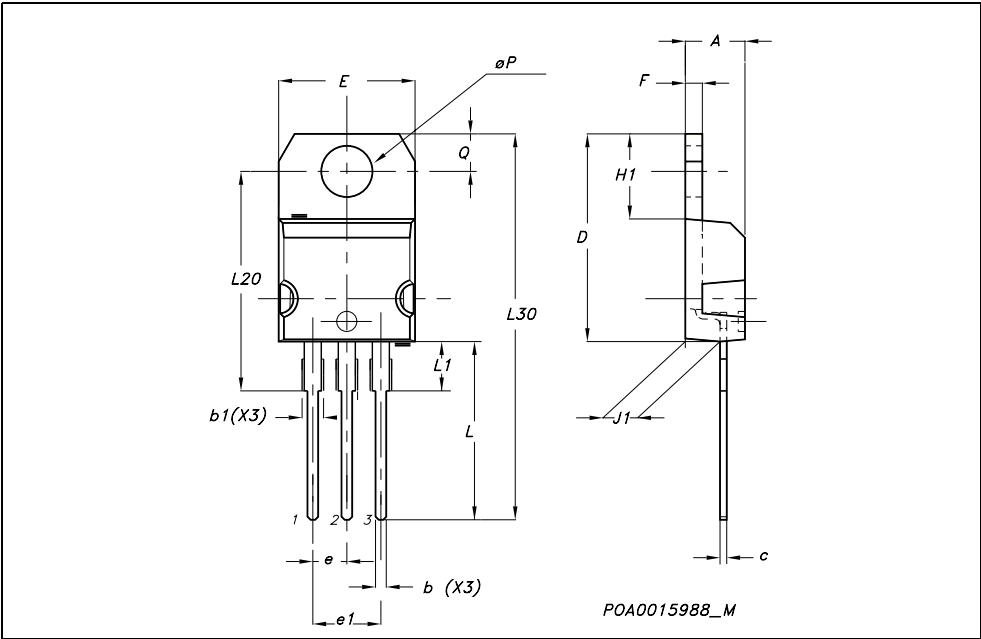
| DPAK MECHANICAL DATA |      |      |      |       |       |       |
|----------------------|------|------|------|-------|-------|-------|
| DIM.                 | mm.  |      |      | inch  |       |       |
|                      | MIN. | TYP  | MAX. | MIN.  | TYP.  | MAX.  |
| A                    | 2.2  |      | 2.4  | 0.086 |       | 0.094 |
| A1                   | 0.9  |      | 1.1  | 0.035 |       | 0.043 |
| A2                   | 0.03 |      | 0.23 | 0.001 |       | 0.009 |
| B                    | 0.64 |      | 0.9  | 0.025 |       | 0.035 |
| b4                   | 5.2  |      | 5.4  | 0.204 |       | 0.212 |
| C                    | 0.45 |      | 0.6  | 0.017 |       | 0.023 |
| C2                   | 0.48 |      | 0.6  | 0.019 |       | 0.023 |
| D                    | 6    |      | 6.2  | 0.236 |       | 0.244 |
| D1                   |      | 5.1  |      |       | 0.200 |       |
| E                    | 6.4  |      | 6.6  | 0.252 |       | 0.260 |
| E1                   |      | 4.7  |      |       | 0.185 |       |
| e                    |      | 2.28 |      |       | 0.090 |       |
| e1                   | 4.4  |      | 4.6  | 0.173 |       | 0.181 |
| H                    | 9.35 |      | 10.1 | 0.368 |       | 0.397 |
| L                    | 1    |      |      | 0.039 |       |       |
| (L1)                 |      | 2.8  |      |       | 0.110 |       |
| L2                   |      | 0.8  |      |       | 0.031 |       |
| L4                   | 0.6  |      | 1    | 0.023 |       | 0.039 |
| R                    |      | 0.2  |      |       | 0.008 |       |
| V2                   | 0°   |      | 8°   | 0°    |       | 8°    |

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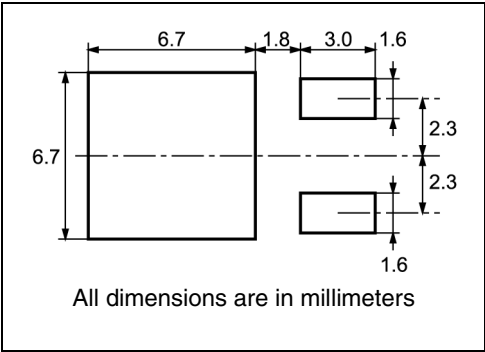
TO-220 MECHANICAL DATA

| DIM. | mm.   |       |       | inch  |       |       |
|------|-------|-------|-------|-------|-------|-------|
|      | MIN.  | TYP.  | MAX.  | MIN.  | TYP.  | MAX.  |
| A    | 4.40  |       | 4.60  | 0.173 |       | 0.181 |
| b    | 0.61  |       | 0.88  | 0.024 |       | 0.034 |
| b1   | 1.15  |       | 1.70  | 0.045 |       | 0.066 |
| c    | 0.49  |       | 0.70  | 0.019 |       | 0.027 |
| D    | 15.25 |       | 15.75 | 0.60  |       | 0.620 |
| E    | 10    |       | 10.40 | 0.393 |       | 0.409 |
| e    | 2.40  |       | 2.70  | 0.094 |       | 0.106 |
| e1   | 4.95  |       | 5.15  | 0.194 |       | 0.202 |
| F    | 1.23  |       | 1.32  | 0.048 |       | 0.052 |
| H1   | 6.20  |       | 6.60  | 0.244 |       | 0.256 |
| J1   | 2.40  |       | 2.72  | 0.094 |       | 0.107 |
| L    | 13    |       | 14    | 0.511 |       | 0.551 |
| L1   | 3.50  |       | 3.93  | 0.137 |       | 0.154 |
| L20  |       | 16.40 |       |       | 0.645 |       |
| L30  |       | 28.90 |       |       | 1.137 |       |
| øP   | 3.75  |       | 3.85  | 0.147 |       | 0.151 |
| Q    | 2.65  |       | 2.95  | 0.104 |       | 0.116 |

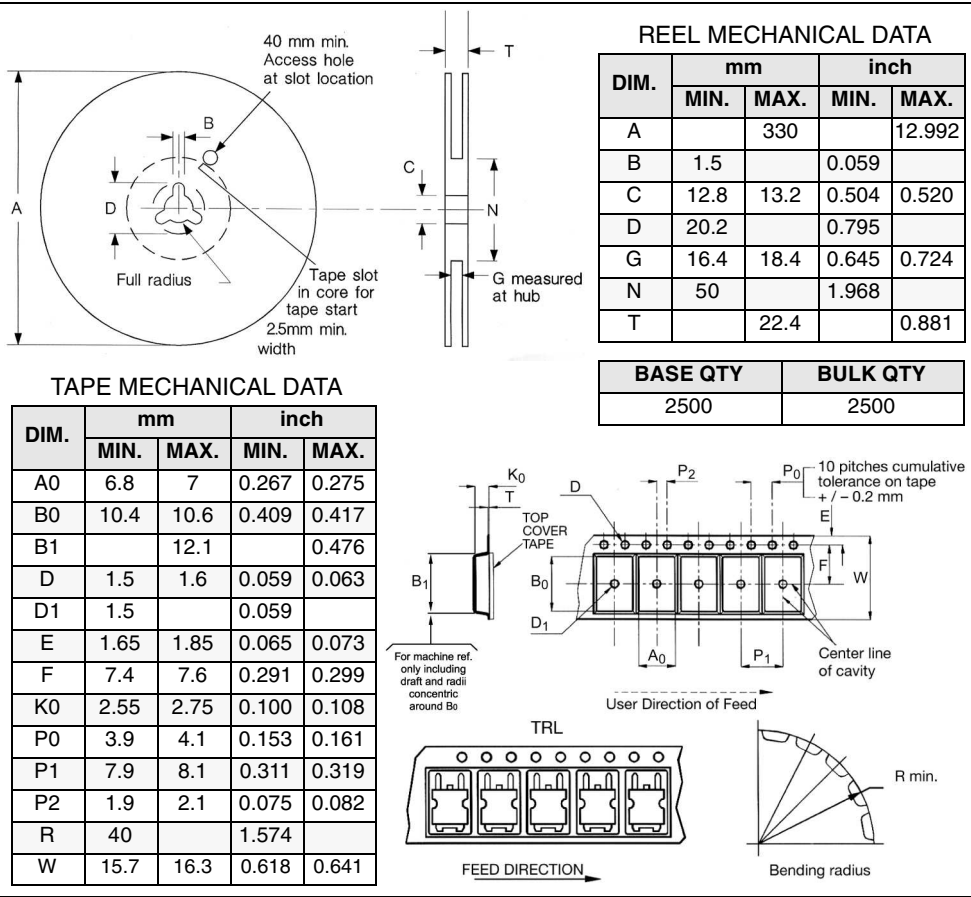


# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 7. Revision history**

| <b>Date</b> | <b>Revision</b> | <b>Changes</b>          |
|-------------|-----------------|-------------------------|
| 22-Feb-2007 | 1               | First release           |
| 15-May-2007 | 2               | Changes on applications |

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