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ZL30301

Timing over Packet (ToP) Technology

Data Sheet

September 2005

Features

- Recovers and transmits network synchronization over Ethernet, IP and MPLS Networks
- Output clocks meet ITU-T G.823 and G.824 traffic interface specifications, and ANSI T1.403 timing requirements
- Fully configurable, enabling performance to be tailored to application and network requirements
- Generates outgoing packet reference locked to the TS_CLKi electrical reference clock
- Recovers up to 4 independent clock frequencies from packet streams, in the frequency range 1.544 MHz to 10 MHz
- Average frequency accuracy better than ± 15 ppb
- Supports Master, Slave and Repeater modes of operation
- Supports user defined timing recovery algorithms
- Dual configurable packet interface:
  - Two MII interfaces
  - One MII and one GMII/TBI
- Flexible 32 bit host CPU interface (Motorola PowerQUICC™ 1 and 2 compatible)

Ordering Information

ZL30301GAG 324 PBGA Trays

-40°C to +85°C

- Flexible classification of incoming packets at layers 2, 3, 4 and 5
- Flexible, multi-protocol packet encapsulation, with support for Ethernet, VLAN, IPv4/6, MPLS, L2TPv3, UDP and RTP
- JTAG (IEEE 1149) boundary-scan interface

Applications

- GSM, UMTS air interface synchronization over a packet network
- Circuit Emulation Service over Packets (CESoP), TDM over IP (TDMoIP)
- IP-PBX
- VoIP Gateways
- Video Conferencing
- Broadband Video Distribution

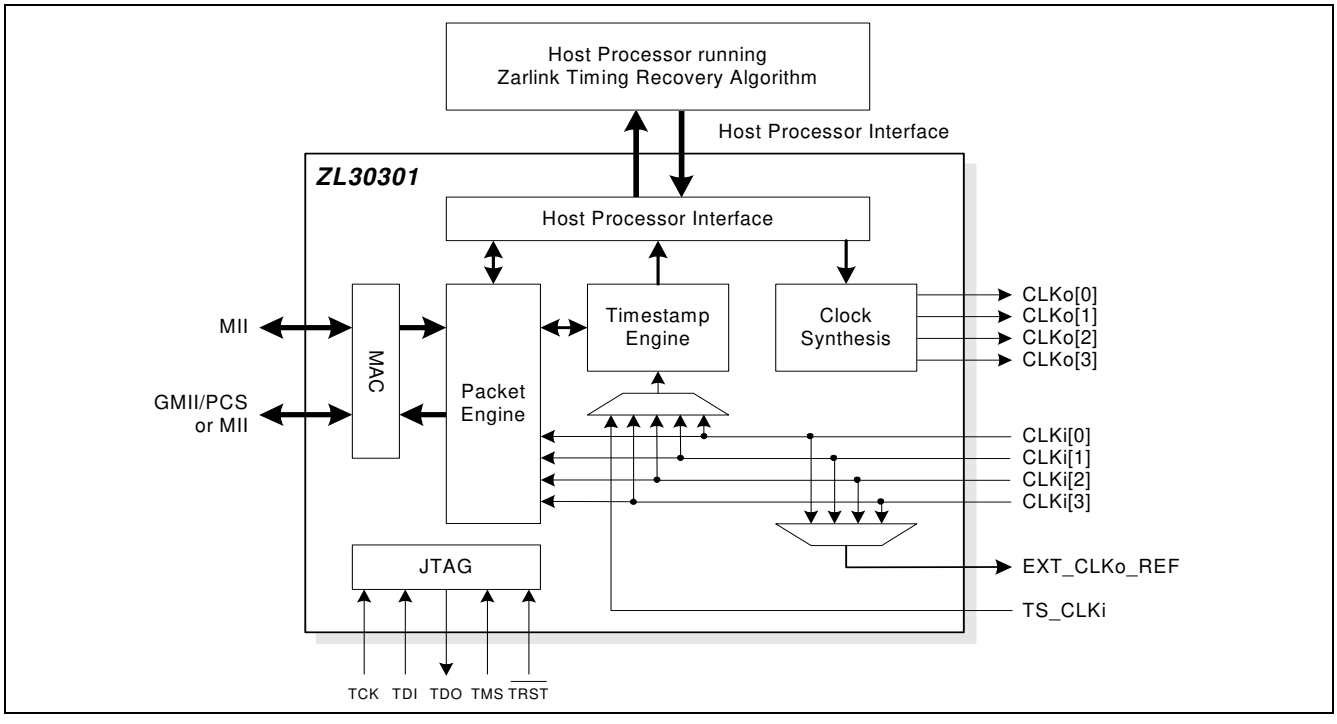

Figure 1 - ZL30301 Functional Block Diagram

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1.0 Description

Network infrastructures are gradually converging onto an asynchronous packet-based architecture. With this convergence, there are an increasing number of synchronous applications that require accurate timing to be distributed over the packet network. Examples of precision timing sensitive applications that need to transport synchronization over asynchronous packet networks include transport of TDM over packet networks, connections to 2 G and 3 G wireless base stations, Voice over IP, IP PBXs, videoconferencing and broadband video.

Zarlink's Timing over Packet (ToP) technology enables accurate timing and synchronization to be distributed across an asynchronous packet network. This patent-pending technology is implemented in the ZL3030x family of devices, which in combination with the line card microprocessor provide a complete solution for high performance clock synchronization over an asynchronous packet network. The family supports synchronization transfer across both layer 2 and layer 3 networks, using a range of standard protocols including Ethernet, VLAN, MPLS, IP, L2TPv3, UDP and RTP.

The ZL30301 recovers up to 4 independent clocks that are locked to 4 independent references. It receives synchronization information in the form of numbered and time-stamped packets, whose arrival time is cross-referenced to the local clock source. This information is transmitted to the microprocessor, which in turn controls synthesis of the recovered clock.

The ZL30301 algorithm continuously tracks the frequency offset (phase drift) between the clocks located at the master and the slave nodes connected via the packet switched network. This algorithm is tolerant of packet delay variation caused by packet queuing; the precision of the timing recovery depends on statistical properties of the propagation delay of timing packets through the network.

The device is highly configurable to ensure that in the presence of jitter and wander of the reference signals, and short network interruptions, the generated clocks meet the appropriate international standards.

The ZL30301 is designed to maintain average frequency accuracy better than +/-15 ppb with a Stratum 3 quality TCXO system clock and it is tolerant of packet network impairments. However network effects, and the behavior of the sending side of the synchronization link can degrade clock frequency accuracy.

In the event of a failure in the packet network, or the advent of severe congestion preventing or seriously delaying the delivery of timing packets, the ZL30301 will put the recovered clocks into holdover until the flow of timing packets is restored. When the device is in holdover mode the drift of the system clock directly affects the accuracy of the holdover.

The ZL30301 provides the JTAG (Joint Test Action Group) interface.

2.0 Physical Specification

The package for the ZL30301 is a 324-ball PBGA.

Features:

- Body Size: 23 mm x 23 mm (typ)
- Ball Count: 324
- Ball Pitch: 1.00 mm (typ)
- Ball Matrix: 22 x 22
- Ball Diameter: 0.60 mm (typ)
- Total Package Thickness: 2.03 mm (typ)

ZL30301 Package view from TOP side. Note that ball A1 is non-chamfered corner.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VDD_IO	M1_TXEN	M0_TXCLK	M0_RXD[7]	M0_RXD[6]	M0_RXD[4]	M0_COL	M0_GTX_CLK	M0_TXEN	DEVICE_ID[2]	CPU_DATA[28]	CPU_DATA[24]	GND	CPU_DATA[23]	GND	CPU_DATA[19]	CPU_DATA[12]	CPU_DATA[9]	CPU_DATA[8]	CPU_DATA[7]	CPU_SDACK1	VDD_IO
B	M1_TXD[2]	VDD_IO	GND	M1_TXD[0]	M1_TXD[1]	M0_CRS	M0_RXD[0]	M0_RBC1	M0_RBC0	M0_TXER	GND	M0_TXD[5]	M0_TXD[3]	M0_TXD[2]	M1_ACTIVE_LED	CPU_DATA[27]	CPU_DATA[22]	CPU_DATA[20]	CPU_DATA[13]	GND	VDD_IO	CPU_TA
C	M1_TXD[3]	GND	VDD_IO	M1_RXCLK	M1_COL	M1_TXER	M0_RXDV	M0_RXD[3]	M0_RXD[1]	M0_RXCLK	M0_TXD[7]	M0_TXD[4]	M0_TXD[0]	VDD_IO	VDD_IO	CPU_DATA[31]	M1_LINKUP_LED	CPU_DATA[29]	CPU_DATA[26]	VDD_IO	GND	CPU_DREQ1
D	M1_RXD[1]	M1_RXD[0]	M1_RXD[2]	VDD_IO	M1_RXDV	M0_RXER	VDD_IO	M0_RXD[5]	VDD_CORE	M0_RXD[2]	M0_REFCLK	M0_TXD[6]	M0_TXD[1]	VDD_CORE	VDD_CORE	VDD_IO	M0_ACTIVE_LED	VDD_CORE	VDD_IO	CPU_DATA[25]	CPU_ADDR[23]	CPU_DATA[6]
E	M1_RXD[3]	M0_GIGABIT_LED	M1_TXCLK	M1_RXER															CPU_DATA[30]	CPU_DATA[21]	CPU_DATA[15]	CPU_DATA[14]
F	NC	M1_CRS	DEVICE_ID[1]	VDD_CORE															VDD_CORE	CPU_DATA[18]	CPU_DATA[17]	CPU_DATA[16]
G	M_MDIO	DEVICE_ID[0]	M0_LINKUP_LED	VDD_IO															VDD_IO	CPU_IREQ1	CPU_DATA[11]	CPU_DATA[0]
H	M_MDC	GND	NC	VDD_CORE															CPU_DATA[10]	CPU_DATA[1]	CPU_DATA[4]	IC
J	NC	NC	NC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_DATA[5]	CPU_DATA[3]	CPU_IREQ0
K	NC	NC	NC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_DATA[2]	IC	CPU_DREQ0
L	GND	CON_L3	CON_L2	VDD_CORE					GND	GND	GND	GND	GND	GND					CPU_CLK	GND	CPU_SDACK2	IC_VDD_IO
M	CLKi[3]	IC	IC	VDD_IO					GND	GND	GND	GND	GND	GND					GND	CPU_TS_ALE	CPU_WE	CPU_OE
N	IC	CLKo[3]	IC	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_IO	CPU_ADDR[22]	CPU_CS	CPU_ADDR[19]
P	CLKi[2]	GND	VDD_IO	VDD_CORE					GND	GND	GND	GND	GND	GND					VDD_CORE	CPU_ADDR[17]	CPU_ADDR[18]	CPU_ADDR[21]
R	CLKo[2]	IC	CLKi[0]	IC															GND	CPU_ADDR[11]	CPU_ADDR[13]	CPU_ADDR[20]
T	CLKi[1]	CLKo[1]	IC	VDD_IO															VDD_IO	VDD_IO	CPU_ADDR[14]	CPU_ADDR[16]
U	IC	VDD_IO	GND	IC															VDD_CORE	JTAG_TMS	CPU_ADDR[15]	CPU_ADDR[12]
V	IC	CLKo[0]	IC	TS_CLKI															DEVICE_ID[3]	JTAG_TCK	CPU_ADDR[10]	CPU_ADDR[9]
W	IC	IC	IC	VDD_IO	VDD_IO	VDD_CORE	VDD_IO	VDD_IO	VDD_CORE	EXT_CLKo REF	IC_GND	GND	SYSTEM_CLK	VDD_CORE	IC	VDD_IO	IC	DEVICE_ID[4]	VDD_IO	JTAG_TDO	CPU_ADDR[4]	CPU_ADDR[8]
Y	IC	GND	VDD_IO	IC	IC	VDD_CORE	IC	IC	IC	IC	IC_GND	IC	GND	GND	IC	IC	TEST_MODE[1]	JTAG_TRST	IC_GND	VDD_IO	GND	CPU_ADDR[7]
AA	IC	VDD_IO	GND	VDD_IO	VDD_IO	IC	GND	A1VDD_PLL1	IC	IC	SYSTEM_DEBUG	SYSTEM_RST	GPIO[1]	GPIO[2]	GPIO[7]	IC	TEST_MODE[0]	JTAG_TDI	IC_GND	GND	VDD_IO	CPU_ADDR[6]
AB	VDD_IO	IC	IC	IC	GND	IC	IC	IC	GPIO[0]	GPIO[3]	GPIO[4]	GPIO[5]	GPIO[6]	IC	IC	IC	TEST_MODE[2]	IC_GND	CPU_ADDR[2]	CPU_ADDR[3]	CPU_ADDR[5]	VDD_IO

Figure 2 - ZL30301 Package View and Ball Positions

Ball #	ZL30301 Signal Name
A1	VDD_IO
A10	DEVICE_ID[2]
A11	CPU_DATA[28]
A12	CPU_DATA[24]
A13	GND
A14	CPU_DATA[23]
A15	GND
A16	CPU_DATA[19]
A17	CPU_DATA[12]
A18	CPU_DATA[9]
A19	CPU_DATA[8]
A20	CPU_DATA[7]
A21	CPU_SDACK1
A22	VDD_IO
A2	M1_TXEN
A3	M0_TXCLK
A4	M0_RXD[7]
A5	M0_RXD[6]
A6	M0_RXD[4]
A7	M0_COL
A8	M0_GTX_CLK
A9	M0_TXEN
B1	M1_TXD[2]
B10	M0_TXER
B11	GND
B12	M0_TXD[5]
B13	M0_TXD[3]
B14	M0_TXD[2]
B15	M1_ACTIVE_LED
B16	CPU_DATA[27]
B17	CPU_DATA[22]
B18	CPU_DATA[20]
B19	CPU_DATA[13]
B20	GND
B21	VDD_IO
B22	CPU_TA
B2	VDD_IO
B3	GND
B4	M1_TXD[0]
B5	M1_TXD[1]

Table 1 - ZL30301 Ball Signal Assignment

Ball #	ZL30301 Signal Name
B6	M0_CRS
B7	M0_RXD[0]
B8	M0_RBC1
B9	M0_RBC0
C1	M1_TXD[3]
C10	M0_RXCLK
C11	M0_TXD[7]
C12	M0_TXD[4]
C13	M0_TXD[0]
C14	VDD_IO
C15	VDD_IO
C16	CPU_DATA[31]
C17	M1_LINKUP_LED
C18	CPU_DATA[29]
C19	CPU_DATA[26]
C20	VDD_IO
C21	GND
C22	CPU_DREQ1
C2	GND
C3	VDD_IO
C4	M1_RXCLK
C5	M1_COL
C6	M1_TXER
C7	M0_RXDV
C8	M0_RXD[3]
C9	M0_RXD[1]
D1	M1_RXD[1]
D10	M0_RXD[2]
D11	M0_REFCLK
D12	M0_TXD[6]
D13	M0_TXD[1]
D14	VDD_CORE
D15	VDD_CORE
D16	VDD_IO
D17	M0_ACTIVE_LED
D18	VDD_CORE
D19	VDD_IO
D20	CPU_DATA[25]
D21	CPU_ADDR[23]
D22	CPU_DATA[6]

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
D2	M1_RXD[0]
D3	M1_RXD[2]
D4	VDD_IO
D5	M1_RXDV
D6	M0_RXER
D7	VDD_IO
D8	M0_RXD[5]
D9	VDD_CORE
E1	M1_RXD[3]
E19	CPU_DATA[30]
E20	CPU_DATA[21]
E21	CPU_DATA[15]
E22	CPU_DATA[14]
E2	M0_GIGABIT_LED
E3	M1_TXCLK
E4	M1_RXER
F1	NC
F19	VDD_CORE
F20	CPU_DATA[18]
F21	CPU_DATA[17]
F22	CPU_DATA[16]
F2	M1_CRS
F3	DEVICE_ID[1]
F4	VDD_CORE
G1	M_MDIO
G19	VDD_IO
G20	CPU_IREQ1
G21	CPU_DATA[11]
G22	CPU_DATA[0]
G2	DEVICE_ID[0]
G3	M0_LINKUP_LED
G4	VDD_IO
H1	M_MDC
H19	CPU_DATA[10]
H20	CPU_DATA[1]
H21	CPU_DATA[4]
H22	IC
H2	GND
H3	NC
H4	VDD_CORE

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
J1	NC
J10	GND
J11	GND
J12	GND
J13	GND
J14	GND
J19	VDD_CORE
J20	CPU_DATA[5]
J21	CPU_DATA[3]
J22	CPU_IREQ0
J2	NC
J3	NC
J4	VDD_CORE
J9	GND
K1	NC
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K19	GND
K20	CPU_DATA[2]
K21	IC
K22	CPU_DREQ0
K2	NC
K3	NC
K4	VDD_IO
K9	GND
L1	GND
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L19	CPU_CLK
L20	GND
L21	CPU_SDACK2
L22	IC_VDD_IO
L2	CON_L3
L3	CON_L2

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
L4	VDD_CORE
L9	GND
M1	CLKi[3]
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M19	GND
M20	CPU_TS_ALE
M21	CPU_WE
M22	CPU_OE
M2	IC
M3	IC
M4	VDD_IO
M9	GND
N1	IC
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N19	VDD_IO
N20	CPU_ADDR[22]
N21	CPU_CS
N22	CPU_ADDR[19]
N2	CLKo[3]
N3	IC
N4	VDD_CORE
N9	GND
P1	CLKi[2]
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P19	VDD_CORE
P20	CPU_ADDR[17]
P21	CPU_ADDR[18]
P22	CPU_ADDR[21]

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
P2	GND
P3	VDD_IO
P4	VDD_CORE
P9	GND
R1	CLKo[2]
R19	GND
R20	CPU_ADDR[11]
R21	CPU_ADDR[13]
R22	CPU_ADDR[20]
R2	IC
R3	CLKi[0]
R4	IC
T1	CLKi[1]
T19	VDD_IO
T20	VDD_IO
T21	CPU_ADDR[14]
T22	CPU_ADDR[16]
T2	CLKo[1]
T3	IC
T4	VDD_IO
U1	IC
U19	VDD_CORE
U20	JTAG_TMS
U21	CPU_ADDR[15]
U22	CPU_ADDR[12]
U2	VDD_IO
U3	GND
U4	IC
V1	IC
V19	DEVICE_ID[3]
V20	JTAG_TCK
V21	CPU_ADDR[10]
V22	CPU_ADDR[9]
V2	CLKo[0]
V3	IC
V4	TS_CLKI
W1	IC
W10	EXT_CLKo_REF
W11	IC_GND
W12	GND

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
W13	SYSTEM_CLK
W14	VDD_CORE
W15	IC
W16	VDD_IO
W17	IC
W18	DEVICE_ID[4]
W19	VDD_IO
W20	JTAG_TDO
W21	CPU_ADDR[4]
W22	CPU_ADDR[8]
W2	IC
W3	IC
W4	VDD_IO
W5	VDD_IO
W6	VDD_CORE
W7	VDD_IO
W8	VDD_IO
W9	VDD_CORE
Y1	IC
Y10	IC
Y11	IC_GND
Y12	IC
Y13	GND
Y14	GND
Y15	IC
Y16	IC
Y17	TEST_MODE[1]
Y18	JTAG_TRST
Y19	IC_GND
Y20	VDD_IO
Y21	GND
Y22	CPU_ADDR[7]
Y2	GND
Y3	VDD_IO
Y4	IC
Y5	IC
Y6	VDD_CORE
Y7	IC
Y8	IC
Y9	IC

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
AA1	IC
AA10	IC
AA11	SYSTEM_DEBUG
AA12	SYSTEM_RST
AA13	GPIO[1]
AA14	GPIO[2]
AA15	GPIO[7]
AA16	IC
AA17	TEST_MODE[0]
AA18	JTAG_TDI
AA19	IC_GND
AA20	GND
AA21	VDD_IO
AA22	CPU_ADDR[6]
AA2	VDD_IO
AA3	GND
AA4	VDD_IO
AA5	VDD_IO
AA6	IC
AA7	GND
AA8	A1VDD_PLL1
AA9	IC
AB1	VDD_IO
AB10	GPIO[3]
AB11	GPIO[4]
AB12	GPIO[5]
AB13	GPIO[6]
AB14	IC
AB15	IC
AB16	IC
AB17	TEST_MODE[2]
AB18	IC_GND
AB19	CPU_ADDR[2]
AB20	CPU_ADDR[3]
AB21	CPU_ADDR[5]
AB22	VDD_IO
AB2	IC
AB3	IC
AB4	IC
AB5	GND

Table 1 - ZL30301 Ball Signal Assignment (continued)

Ball #	ZL30301 Signal Name
AB6	IC
AB7	IC
AB8	IC
AB9	GPIO[0]

Table 1 - ZL30301 Ball Signal Assignment (continued)

NC - Not Connected - leave open circuit.
IC - Internally Connected - leave open circuit.
IC_GND - Internally Connected - tie to ground
IC_VDD_IO - Internally Connected - tie to VDD_IO
CON_L2 - connect to ball L2
CON_L3 - connect to ball L3

3.0 External Interface Description

The following key applies to all tables:

I	Input
O	Output
D	Internal 100 kΩ pull-down resistor present
U	Internal 100 kΩ pull-up resistor present
T	Tri-state Output

3.1 Clock Interface

All Clock Interface signals are 5 V tolerant.

All Clock Interface outputs are high impedance while System Reset is LOW.

All Clock Interface inputs have internal pull-down resistors so they can be safely left unconnected if not used.

Signal	I/O	Package Balls	Description
CLKi[3:0]	I D	[3] M1 [2] P1 [1] T1 [0] R3	Clock inputs. In master mode these input are connected to CLKo[3:0], respectively. In slave mode these inputs can be connected to CLKo[3:0] for some applications. These inputs accepts frequencies from 8 kHz up to 34.368 MHz
CLKo[3:0]	OT	[3] N2 [2] R1 [1] T2 [0] V2	Clock outputs. In slave mode, these are the recovered clocks from the packet network. These clocks may be connected to CLKi[3:0] for some applications, e.g., selection of a single output clock, or selection of a timestamp reference for a repeater function. In master mode these outputs are connected to CLKi[3:0], respectively. The recovered clocks are 8 kHz multiples in the range 1.544 MHz to 10 MHz.
TS_CLKi	I D	V4	Time Stamp clock input. In master mode and/or repeater mode, this input is multiplexed with the four input clock signals CLKi[3:0] to select the clock to be distributed over the packet network. It is used as the timestamp clock, or as a reference clock input for differential clock recovery. Acceptable frequency range: 1.544 MHz - 10 MHz (timestamp clock) or 4 MHz to 40 MHz (differential reference clock).

Table 2 - Clock Interface Pin Definition

Signal	I/O	Package Balls	Description
EXT_CLKo_REF	OT	W10	Multiplexed output signal, selecting one of the clock inputs, CLKi[3:0]. The source clock may be frequency divided internally prior to output on EXT_CLKo_REF pin. Expected frequency range: 8 kHz - 10 MHz.

Table 2 - Clock Interface Pin Definition

Note: All Clock Interface inputs have internal pull-down resistors so they can be safely left unconnected if not used.

3.2 Packet Interfaces

The ZL30301 packet interface features either 2 MII interfaces, or 1 MII and 1 GMII interfaces, or 1 MII and 1 TBI (1000 Mbps) interfaces. The TBI interface is a PCS interface supported by an integrated 1000BASE-X PCS module.

Data for all three types of packet switching is based on Specification IEEE Std. 802.3 - 2000. Only Port 0 has the 1000 Mbps capability necessary for the GMII/TBI interface.

Table 3 maps the signal pins used in the MII interface to those used in the GMII and TBI interface. Table 4 through Table 6 show all the pins and their related package balls, based on the GMII/MII configuration.

All Packet Interface signals are 5 V tolerant, and all outputs are high impedance while System Reset is LOW.

MII	GMII	TBI (PCS)
M*n*_LINKUP_LED	M*n*_LINKUP_LED	M*n*_LINKUP_LED
M*n*_ACTIVE_LED	M*n*_ACTIVE_LED	M*n*_ACTIVE_LED
-	M*n*_GIGABIT_LED	M*n*_GIGABIT_LED
-	M*n*_REFCLK	M*n*_REFCLK
M*n*_RXCLK	M*n*_RXCLK	M*n*_RBC0
M*n*_COL	M*n*_COL	M*n*_RBC1
M*n*_RXD[3:0]	M*n*_RXD[7:0]	M*n*_RXD[7:0]
M*n*_RXDV	M*n*_RXDV	M*n*_RXD[8]
M*n*_RXER	M*n*_RXER	M*n*_RXD[9]
M*n*_CRS	M*n*_CRS	M*n*_Signal_Detect
M*n*_TXCLK	-	-
M*n*_TXD[3:0]	M*n*_TXD[7:0]	M*n*_TXD[7:0]
M*n*_TXEN	M*n*_TXEN	M*n*_TXD[8]
M*n*_TXER	M*n*_TXER	M*n*_TXD[9]
-	M*n*_GTX_CLK	M*n*_GTX_CLK

Table 3 - Packet Interface Signal Mapping - MII to GMII/TBI

Note: M*n* can be either M0 or M1 for ZL30301.

Signal	I/O	Package Balls	Description
M_MDC	O	H1	MII management data clock. Common for both MII ports. It has a minimum period of 400 ns (maximum frequency 2.5 MHz), and is independent of the TXCLK and RXCLK.
M_MDIO	ID/ OT	G1	MII management data I/O. Common for both MII ports at up to 2.5 MHz. It is bi-directional between the ZL30301 and the Ethernet station management entity. Data is passed synchronously with respect to M_MDC.

Table 4 - MII Management Interface Package Ball Definition

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_LINKUP_LED	O	G3	LED drive for MAC 0 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M0_ACTIVE_LED	O	D17	LED drive for MAC 0 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off
M0_GIGABIT_LED	O	E2	LED drive for MAC 0 to indicate operation at Gbps. Logic 0 output = LED on Logic 1 output = LED off
M0_REFCLK	I D	D11	**GMII/TBI** - Reference Clock input at 125 MHz. Can be used to lock receive circuitry (RX) to M0_GTXCLK rather than recovering the RXCLK (or RBC0 and RBC1). Useful, for example, in the absence of valid serial data. **NOTE:** In **MII** mode this pin must be driven with the same clock as M0_RXCLK.
M0_RXCLK	I U	C10	GMII/MII - M0_RXCLK. Accepts the following frequencies: 25.0 MHz MII 100 Mbps 125.0 MHz GMII 1 Gbps
M0_RBC0	I U	B9	TBI - M0_RBC0. Used as a clock when in TBI mode. Accepts 62.5 MHz and is 180°C out of phase with M0_RBC1. Receive data is clocked at each rising edge of M0_RBC1 and M0_RBC0, resulting in 125 MHz sample rate.

Table 5 - MII Port 0 Interface Package Ball Definition

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_RBC1	I U	B8	TBI - M0_RBC1 Used as a clock when in TBI mode. Accepts 62.5 MHz, and is 180° out of phase with M0_RBC0. Receive data is clocked at each rising edge of M0_RBC1 and M0_RBC0, resulting in 125 MHz sample rate.
M0_COL	I D	A7	GMII/MII - M0_COL. Collision Detection. This signal is independent of M0_TXCLK and M0_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.
M0_RXD[7:0]	I U	[7] A4 [3] C8 [6] A5 [2] D10 [5] D8 [1] C9 [4] A6 [0] B7	Receive Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M0_RXCLK (GMII/MII) or the rising edges of M0_RBC0 and M0_RBC1 (TBI).
M0_RXDV / M0_RXD[8]	I D	C7	GMII/MII - M0_RXDV Receive Data Valid. Active high. This signal is clocked on the rising edge of M0_RXCLK. It is asserted when valid data is on the M0_RXD bus. TBI - M0_RXD[8] Receive Data. Clocked on the rising edges of M0_RBC0 and M0_RBC1.
M0_RXER / M0_RXD[9]	I D	D6	GMII/MII - M0_RXER Receive Error. Active high signal indicating an error has been detected. Normally valid when M0_RXDV is asserted. Can be used in conjunction with M0_RXD when M0_RXDV signal is de-asserted to indicate a False Carrier. TBI - M0_RXD[9] Receive Data. Clocked on the rising edges of M0_RBC0 and M0_RBC1.
M0_CRS / M0_Signal_Detect	I D	B6	GMII/MII - M0_CRS Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high. TBI - M0_Signal Detect Similar function to M0_CRS.
M0_TXCLK	I U	A3	**MII only** - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps

Table 5 - MII Port 0 Interface Package Ball Definition (continued)

MII Port 0			
Signal	**I/O**	**Package Balls**	**Description**
M0_TXD[7:0]	O	[7] C11 [3] B13 [6] D12 [2] B14 [5] B12 [1] D13 [4] C12 [0] C13	Transmit Data. Only half the bus (bits [3:0]) are used in MII mode. Clocked on rising edge of M0_TXCLK (MII) or the rising edge of M0_GTXCLK (GMII/TBI).
M0_TXEN / M0_TXD[8]	O	A9	GMII/MII - M0_TXEN Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M0_TXCLK with the first preamble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high. TBI - M0_TXD[8] Transmit Data. Clocked on rising edge of M0_GTXCLK.
M0_TXER / M0_TXD[9]	O	B10	GMII/MII - M0_TXER Transmit Error. Transmitted synchronously with respect to M0_TXCLK, and active high. When asserted (with M0_TXEN also asserted) the ZL30301 will transmit a non-valid symbol, somewhere in the transmitted frame. TBI - M0_TXD[9] Transmit Data. Clocked on rising edge of M0_GTXCLK.
M0_GTX_CLK	O	A8	**GMII/TBI only** - Gigabit Transmit Clock Output of a clock for Gigabit operation at 125 MHz.

Table 5 - MII Port 0 Interface Package Ball Definition (continued)

MII Port 1			
Signal	**I/O**	**Package Balls**	**Description**
M1_LINKUP_LED	O	C17	LED drive for MAC 1 to indicate port is linked up. Logic 0 output = LED on Logic 1 output = LED off
M1_ACTIVE_LED	O	B15	LED drive for MAC 1 to indicate port is transmitting or receiving packet data. Logic 0 output = LED on Logic 1 output = LED off
M1_RXCLK	I U	C4	MII only - Receive Clock. Accepts the following frequencies: 25.0 MHz MII 100 Mbps

Table 6 - MII Port 1 Interface Package Ball Definition

MII Port 1			
Signal	**I/O**	**Package Balls**	**Description**
M1_COL	I D	C5	Collision Detection. This signal is independent of M1_TXCLK and M1_RXCLK, and is asserted when a collision is detected on an attempted transmission. It is active high, and only specified for half-duplex operation.
M1_RXD[3:0]	I U	[3] E1 [1] D1 [2] D3 [0] D2	Receive Data. Clocked on rising edge of M1_RXCLK.
M1_RXDV	I D	D5	Receive Data Valid. Active high. This signal is clocked on the rising edge of M1_RXCLK. It is asserted when valid data is on the M1_RXD bus.
M1_RXER	I D	E4	Receive Error. Active high signal indicating an error has been detected. Normally valid when M1_RXDV is asserted. Can be used in conjunction with M1_RXD when M1_RXDV signal is de-asserted to indicate a False Carrier.
M1_CRS	I D	F2	Carrier Sense. This asynchronous signal is asserted when either the transmission or reception device is non-idle. It is active high.
M1_TXCLK	I U	E3	MII only - Transmit Clock Accepts the following frequencies: 25.0 MHz MII 100 Mbps
M1_TXD[3:0]	O	[3] C1 [1] B5 [2] B1 [0] B4	Transmit Data. Clocked on rising edge of M1_TXCLK.
M1_TXEN	O	A2	Transmit Enable. Asserted when the MAC has data to transmit, synchronously to M1_TXCLK with the first preamble of the packet to be sent. Remains asserted until the end of the packet transmission. Active high.
M1_TXER	O	C6	Transmit Error. Transmitted synchronously with respect to M1_TXCLK, and active high. When asserted (with M1_TXEN also asserted) the ZL30301 will transmit a non-valid symbol, somewhere in the transmitted frame.

Table 6 - MII Port 1 Interface Package Ball Definition (continued)

3.3 CPU Interface

All CPU Interface signals are 5 V tolerant.

All CPU Interface outputs are high impedance while System Reset is LOW.

Signal	I/O	Package Balls	Description
CPU_DATA[31:0]	I/ OT	[31] C16 [30] E19 [29] C18 [28] A11 [27] B16 [26] C19 [25] D20 [24] A12 [23] A14 [22] B17 [21] E20 [20] B18 [19] A16 [18] F20 [17] F21 [16] F22 [15] E21 [14] E22 [13] B19 [12] A17 [11] G21 [10] H19 [9] A18 [8] A19 [7] A20 [6] D22 [5] J20 [4] H21 [3] J21 [2] K20 [1] H20 [0] G22	CPU Data Bus. Bi-directional data bus, synchronously transmitted with CPU_CLK rising edge. NOTE: as with all ports in the ZL30301 device, CPU_DATA[0] is the least significant bit (lsb).
CPU_ADDR[23:2]	I	[23] D21 [22] N20 [21] P22 [20] R22 [19] N22 [18] P21 [17] P20 [16] T22 [15] U21 [14] T21 [13] R21 [12] U22 [11] R20 [10] V21 [9] V22 [8] W22 [7] Y22 [6] AA22 [5] AB21 [4] W21 [3] AB20 [2] AB19	CPU Address Bus. Address input from processor to ZL30301, synchronously transmitted with CPU_CLK rising edge. NOTE: as with all ports in the ZL30301 device, CPU_ADDR[2] is the least significant bit (lsb).
$\overline{\text{CPU\_CS}}$	I U	N21	CPU Chip Select. Synchronous to rising edge of CPU_CLK and active low. Is asserted with CPU_TS_ALE. Must be asserted with $\overline{\text{CPU\_OE}}$ to asynchronously enable the CPU_DATA output during a read, including DMA read.
$\overline{\text{CPU\_WE}}$	I	M21	CPU Write Enable. Synchronously asserted with respect to CPU_CLK rising edge, and active low. Used for CPU writes from the processor to registers within the ZL30301. Asserted one clock cycle after CPU_TS_ALE.

Table 7 - CPU Interface Package Ball Definition

Signal	I/O	Package Balls	Description
CPU_OE	I	M22	CPU Output Enable. Synchronously asserted with respect to CPU_CLK rising edge, and active low. Used for CPU reads from the processor to registers within the ZL30301. Asserted one clock cycle after CPU_TS_ALE. Must be asserted with CPU_CS to asynchronously enable the CPU_DATA output during a read, including DMA read.
CPU_TS_ALE	I	M20	Synchronous input with rising edge of CPU_CLK. Latch Enable (ALE), active high signal. Asserted with CPU_CS, for a single clock cycle.
CPU_SDACK1	I	A21	CPU/DMA 1 Acknowledge Input. Active low synchronous to CPU_CLK rising edge. Used to acknowledge request from ZL30301 for a DMA write transaction. Only used for DMA transfers, not for normal register access.
CPU_SDACK2	I	L21	CPU/DMA 2 Acknowledge Input Active low synchronous to CPU_CLK rising edge. Used to acknowledge request from ZL30301 for a DMA read transaction. Only used for DMA transfers, not for normal register access.
CPU_CLK	I	L19	CPU PowerQUICC™ II Bus Interface clock input. 66 MHz clock, with minimum of 6 ns high/low time. Used to time all host interface signals into and out of ZL30301 device.
CPU_TA	OT	B22	CPU Transfer Acknowledge. Driven from tri-state condition on the negative clock edge of CPU_CLK following the assertion of CPU_CS. Active low, asserted from the rising edge of CPU_CLK. For a read, asserted when valid data is available at CPU_DATA. The data is then read by the host on the following rising edge of CPU_CLK. For a write, is asserted when the ZL30301 is ready to accept data from the host. The data is written on the rising edge of CPU_CLK following the assertion. Returns to tri-state from the negative clock edge of CPU_CLK following the de-assertion of CPU_CS.

Table 7 - CPU Interface Package Ball Definition (continued)

Signal	I/O	Package Balls	Description
$\overline{\text{CPU\_DREQ0}}$	OT	K22	CPU DMA 0 Request Output Active low synchronous to CPU_CLK rising edge. Asserted by ZL30301 to request the host initiates a DMA write. Only used for DMA transfers, not for normal register access.
$\overline{\text{CPU\_DREQ1}}$	OT	C22	CPU DMA 1 Request Active low synchronous to CPU_CLK rising edge. Asserted by ZL30301 to indicate packet data is ready for transmission to the CPU, and request the host initiates a DMA read. Only used for DMA transfers, not for normal register access.
$\overline{\text{CPU\_IREQO}}$	O	J22	CPU Interrupt 0 Request (Active Low)
$\overline{\text{CPU\_IREQ1}}$	O	G20	CPU Interrupt 1 Request (Active Low)

Table 7 - CPU Interface Package Ball Definition (continued)

3.4 System Function Interface

All System Function Interface signals are 5 V tolerant.

The core of the chip will be held in reset for 16383 SYSTEM_CLK cycles after SYSTEM_RST has gone HIGH to allow the PLL's to lock.

Signal	I/O	Package Balls	Description
SYSTEM_CLK	I	W13	System Clock Input. The system clock frequency is 100 MHz.
SYSTEM_RST	I	AA12	System Reset Input. Active low. The system reset is asynchronous, and causes all registers within the ZL30301 to be reset to their default state.
SYSTEM_DEBUG	I	AA11	System Debug Enable. This is an asynchronous signal that, when de-asserted, prevents the software assertion of the debug-freeze command, regardless of the internal state of registers, or any error conditions. Active high.

Table 8 - System Function Interface Package Ball Definition

3.5 Test Facilities

3.5.1 Administration, Control and Test Interface

All Administration, Control and Test Interface signals are 5 V tolerant.

Signal	I/O	Package Balls	Description
GPIO[7:0]	ID/ OT	[7] AA15 [6] AB13 [5] AB12 [4] AB11 [3] AB10 [2] AA14 [1] AA13 [0] AB9	General Purpose I/O pins. Connected to an internal register, so customer can set user-defined parameters.
TEST_MODE[2:0]	I D	[2] AB17 [1] Y17 [0] AA17	Test Mode input - ensure these pins are tied to ground for normal operation. 000 SYS_NORMAL_MODE 001-010 RESERVED 011 SYS_TRISTATE_MODE 100-111 RESERVED

Table 9 - Administration/Control Interface Package Ball Definition

3.5.2 JTAG Interface

All JTAG Interface signals are 5 V tolerant, and conform to the requirements of IEEE1149.1 (2001).

Signal	I/O	Package Balls	Description
$\overline{\text{JTAG\_TRST}}$	I U	Y18	JTAG Reset. Asynchronous reset. In normal operation this pin should be pulled low.
JTAG_TCK	I	V20	JTAG Clock - maximum frequency is 25 MHz, typically run at 10 MHz. In normal operation this pin should be pulled either high or low.
JTAG_TMS	I U	U20	JTAG test mode select. Synchronous to JTAG_TCK rising edge. Used by the Test Access Port controller to set certain test modes.
JTAG_TDI	I U	AA18	JTAG test data input. Synchronous to JTAG_TCK.
JTAG_TDO	O	W20	JTAG test data output. Synchronous to JTAG_TCK.

Table 10 - JTAG Interface Package Ball Definition

3.6 Miscellaneous Inputs

The following unused inputs must be tied low or high as appropriate.

Signal	Package Balls	Description
IC_GND	W11, Y11, Y19, AA19, AB18	Internally connected. Tie to GND.
IC_VDD_IO	L22	Internally connected. Tie to VDD_IO.

Table 11 - Miscellaneous Inputs Package Ball Definitions

3.7 Power and Ground Connections

Signal	Package Balls				Description
VDD_IO	A1	A22	AA2	AA21	3.3 V VDD Power Supply for IO Ring
	AA4	AA5	AB1	AB22	
	B2	B21	C14	C15	
	C20	C3	D16	D19	
	D4	D7	G19	G4	
	K4	M4	N19	P3	
	T19	T20	T4	U2	
	W16	W19	W4	W5	
	W7	W8	Y20	Y3	
GND	A13	A15	AA20	AA3	0 V Ground Supply
	AA7	AB5	B11	B20	
	B3	C2	C21	H2	
	J10	J11	J12	J13	
	J14	J9	K10	K11	
	K12	K13	K14	K19	
	K9	L1	L10	L11	
	L12	L13	L14	L20	
	L9	M10	M11	M12	
	M13	M14	M19	M9	
	N10	N11	N12	N13	
	N14	N9	P10	P11	
	P12	P13	P14	P2	
	P9	R19	U3	W12	
	Y13	Y14	Y2	Y21	
VDD_CORE	D14	D15	D18	D9	1.8 V VDD Power Supply for Core Region
	F19	F4	H4	J19	
	J4	L4	N4	P19	
	P4	U19	W14	W6	
	W9	Y6			
A1VDD	AA8				1.8 V PLL Power Supply

Table 12 - Power and Ground Package Ball Definition

3.8 Internal Connections

The following pins are connected internally, and must be left open circuit.

Signal	Package Balls				Description
IC	AA1	AA10	AA16	AA6	Internally connected. Leave open circuit
	AA9	AB14	AB15	AB16	
	AB2	AB3	AB4	AB6	
	AB7	AB8	H22	K21	
	M2	M3	N1	N3	
	R2	R4	T3	U1	
	U4	V1	V3	W1	
	W17	W2	W3	W15	
	Y1	Y9	Y10	Y12	
	Y15	Y16	Y4	Y5	
	Y7	Y8			

Table 13 - Internal Connections Package Ball Definitions

The following pins must be connected together.

Signal	Package Balls	Description
CON_L3	L2	Connect to ball L3. Balls L2 and L3 perform a loopback, and should be connected only to each other
CON_L2	L3	Connect to ball L2. See L2.

Table 14 - Internal Connections Package Ball Definitions

3.9 No Connections

The following pins are not connected internally, and should be left open circuit.

Signal	Package Balls				Description
NC	F1	H3	J1	J2	No connection. Leave open circuit.
	J3	K1	K2	K3	

Table 15 - Miscellaneous Inputs Package Ball Definitions

3.10 Device ID

Signal	I/O	Package Balls	Description
DEVICE_ID[4:0]	O	[4] W18 [3] V19 [2] A10 [1] F3 [0] G2	Device ID. ZL30300 = 00100 ZL30301 = 10001 ZL30302 = 00110

Table 16 - Device ID Ball Definition

4.0 Typical Applications

Many carriers are now beginning the process of moving their networks over to a packet-based structure. This breaks the circuit-switched nature of the telecommunications network, and divorces the delivery of data from the delivery of timing and synchronization. However, there are many applications which still require accurate timing and synchronization, including:

- Circuit Emulation Service over packets, TDM over IP
- GSM, UMTS air interface synchronization over a packet network
- IP-PBX
- VoIP Gateways
- Video Conferencing
- Broadband Video Distribution

4.1 Edge of the PSN

There are a wide variety of applications and equipment that require synchronization, whether for voice, video or data. Figure 3 is a representation of a few different situations where synchronization from a PRS (primary reference source) is required to be carried across a packet network to its outer edges. At the PRS a ZL30301 is used to encode timing information. This timing is routed through the packet network to the boundaries at the outer edges of the PSN (packet-switched network). At the edge of the PSN another ZL30301 is used to regenerate or recover the timing.

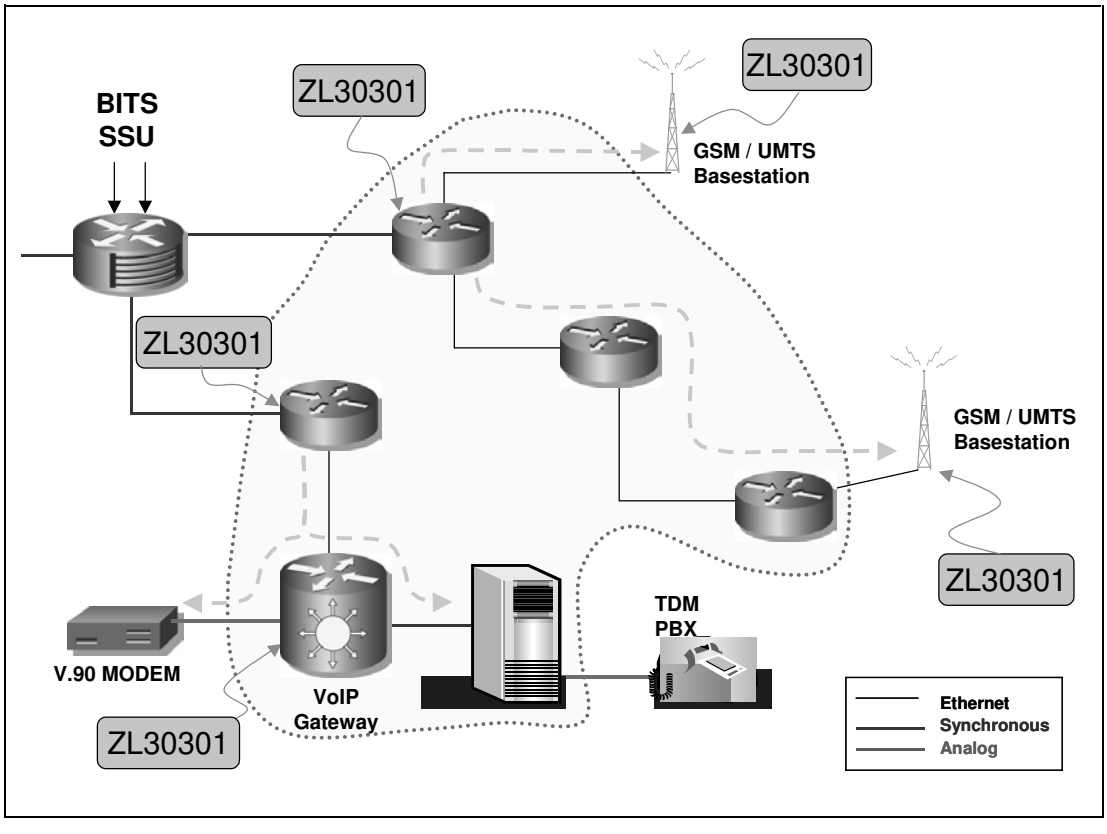

Figure 3 - Edge of the PSN

Unlike VoIP, fax and modem connections are not tolerant of buffer slips or a large number of data errors. A ZL30301 is used to synchronize the fax/modem inter-working functions to ensure no buffer slips.

A second application is legacy PBX support. Using TDM pseudo-wires or Circuit Emulation Services over Packet (CESoP) the T1/E1 interface trunk to the PBX may be carried across a PSN. A ZL30301 may be used in this case to synchronize both ends of the CESoP connection to ensure the T1/E1 line meets the required ITU-T and ANSI timing and synchronization specifications.

A third application is for VoIP. Traditionally VoIP did not put much emphasis on timing and synchronization in the gateway. It is becoming more important, for good voice quality, to reduce buffer slips by synchronizing the VoIP gateway. A ZL30301 is a perfect fit here, as well.

4.2 Wireless Access Applications

Traditionally within the UMTS Terrestrial Radio Access Network the Node B (basestation) is connected to the Radio Network Controller (RNC) through a T1/E1 link. The remote base stations must remain synchronized to the network, and synchronization is also derived from the T1/E1 link. When this link is replaced by a packet network, an alternative means of synchronization must be provided. Current generation wireless base stations often meet synchronization requirements through GPS clocks when PRS traceable network references are not available.

The ZL30301 can replace expensive parts such as GPS, distributing the clock over the packet network from the RNC. The transmit frequency must be maintained at a highly reliable frequency, within +/- 15 ppb from the master clock. This is because the clock is used to generate the radio signals for the air interface, and frequency deviations will cause interference with adjacent cell sites. The master clock can be distributed to the wireless network to maintain all nodes in complete synchronicity. Figure 2 depicts an example of such Wireless Infrastructure.

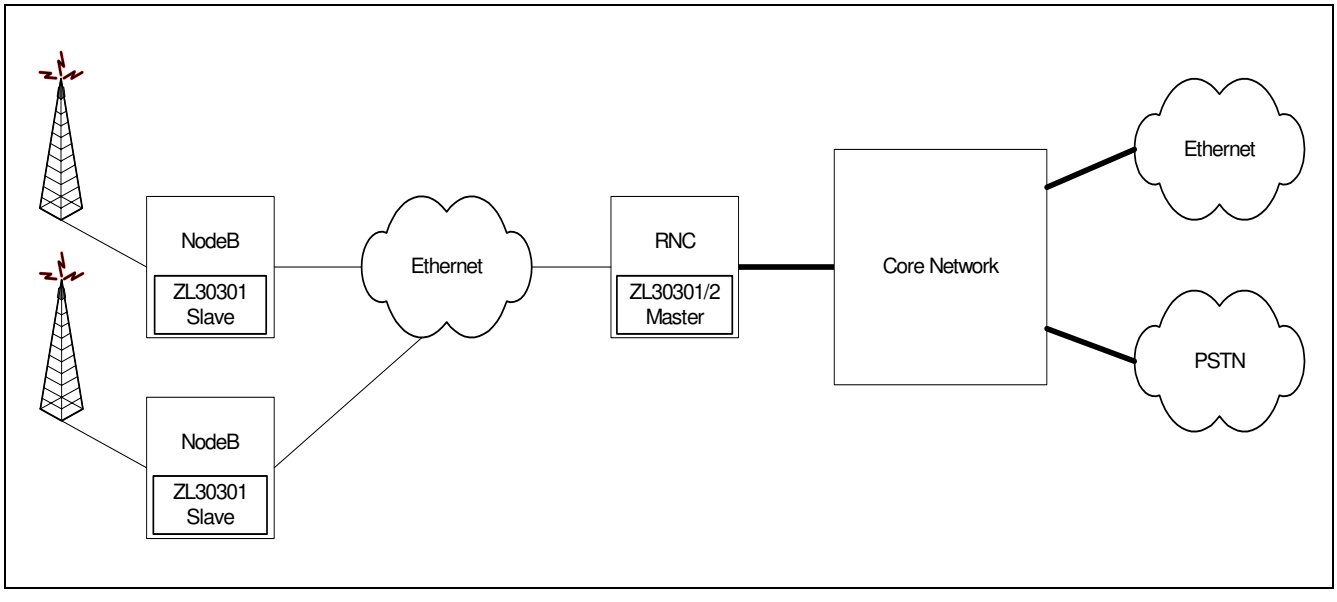

Figure 4 - Example of Wireless Infrastructure