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Switching Power Manager with USB On-the-Go + Triple Step-Down DC/DCs

FEATURES

- **Bidirectional Switching Regulator with Bat-Track™ Adaptive Output Control Provides Efficient Charging and a 5V Output for USB On-The-Go**
- **Bat-Track Control of External High Voltage Step-Down Switching Regulator**
- **Overvoltage Protection Guards Against Damage**
- **Instant-On Operation with Discharged Battery**
- Triple Step-Down Switching Regulators with I^2C Adjustable Outputs (1A/400mA/400mA I_{OUT})
- 180mΩ Internal Ideal Diode + External Ideal Diode Controller Powers the Load in Battery Mode
- Li-Ion/Polymer Battery Charger (1.5A Max I_{CHG})
- Battery Float Voltage: 4.2V (LTC3576), 4.1V (LTC3576-1)
- Compact (4mm × 6mm × 0.75mm) 38-Pin QFN Package

APPLICATIONS

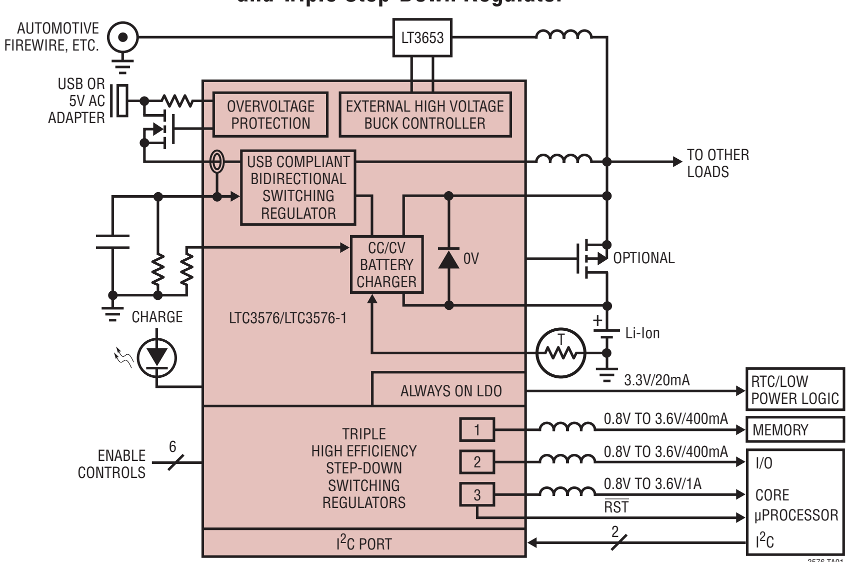
- HDD-Based Media Players
- GPS, PDAs, Digital Cameras, Smart Phones
- Automotive Compatible Portable Electronics

DESCRIPTION

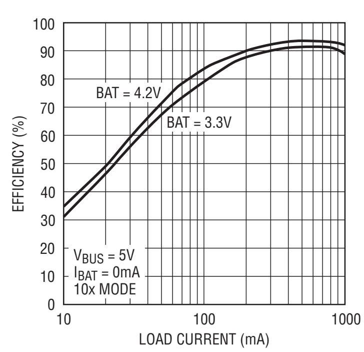
The LTC®3576/LTC3576-1 are highly integrated power management and battery charger ICs for Li-Ion/Polymer battery applications. They each include a high efficiency, bidirectional switching PowerPath™ manager with automatic load prioritization, a battery charger, an ideal diode, a controller for an external high voltage switching regulator and three general purpose step-down switching regulators with I^2C adjustable output voltages. The internal switching regulators automatically limit input current for USB compatibility and can also generate 5V at 500mA for USB on-the-go applications when powered from the battery. Both the USB and external switching regulator power paths feature Bat-Track optimized charging to provide maximum power to the application from supplies as high as 38V. An overvoltage circuit protects the LTC3576/LTC3576-1 from damage due to high voltage on the V_{BUS} or WALL pins with just two external components. The LTC3576/LTC3576-1 are available in a low profile 38-pin (4mm × 6mm × 0.75mm) QFN package.

TYPICAL APPLICATION

High Efficiency PowerPath Manager with Overvoltage Protection and Triple Step-Down Regulator



PowerPath Switching Regulator Efficiency to System Load (P_{VOUT}/P_{VBUS})

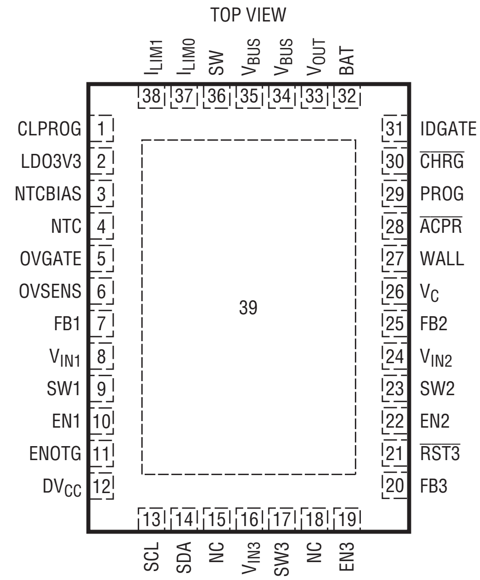


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS}, WALL (Transient) t < 1ms,
Duty Cycle < 1% .... –0.3V to 7V
V_{BUS}, WALL (Static), BAT, V_{IN1}, V_{IN2}, V_{IN3},
V_{OUT}, ENOTG, NTC, SDA, SCL, DV_{CC},
$\overline{RST3}$, $\overline{CHRG}$ .... –0.3V to 6V
I_{LIM0}, I_{ILIM1} .... –0.3V to Max(V_{BUS}, V_{OUT}, BAT) + 0.3V
EN1, EN2, EN3 .... –0.3V to V_{OUT} + 0.3V
FBx (x = 1, 2, 3) ....–0.3V to V_{INx} + 0.3V
I_{OVSENS}...10mA
I_{CLPROG} 3mA
$I_{\overline{CHRG}}$, $I_{\overline{RST3}}$...50mA
I_{PROG}..2mA
I_{LDO3V3}..30mA
I_{SW1}, I_{SW2} (Continuous).....................................600mA
I_{SW}, I_{SW3}, I_{BAT}, I_{VOUT} (Continuous)..............................2A
Maximum Junction Temperature.......................... 125°C
Operating Temperature Range..................–40°C to 85°C
Storage Temperature Range...................–65°C to 125°C

PIN CONFIGURATION



UFE PACKAGE
38-LEAD (4mm × 6mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3576EUFE#PBF	LTC3576EUFE#TRPBF	3576	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 85°C
LTC3576EUFE-1#PBF	LTC3576EUFE-1#TRPBF	35761	38-Lead (4mm × 6mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PowerPath Switching Regulator—Step-Down Mode							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
$I_{VBUS(LIM)}$	Total Input Current	1× Mode 5× Mode 10× Mode Low Power Suspend Mode High Power Suspend Mode	● ● ● ● ●	82 440 800 0.32 1.6	90 472 880 0.39 2.05	100 500 1000 0.5 2.5	mA mA mA mA mA
I_{VBUSQ} (Note 4)	Input Quiescent Current	1× Mode 5×, 10× Modes Low/High Power Suspend Modes			7 17 0.045		mA mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1× Mode 5× Mode 10× Mode Low Power Suspend Mode High Power Suspend Mode			210 1160 2200 9.6 56		mA/mA mA/mA mA/mA mA/mA mA/mA
$I_{VOUT(POWERPATH)}$	V_{OUT} Current Available Before Discharging Battery	1× Mode, BAT = 3.3V 5× Mode, BAT = 3.3V 10× Mode, BAT = 3.3V Low Power Suspend Mode High Power Suspend Mode		 0.26 1.6	121 667 1217 0.31 2	 0.41 2.4	mA mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	Switching Modes Suspend Modes			1.18 100		V mV
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35	V V
V_{DUVLO}	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	1×, 5×, 10× Modes, 0V < BAT < 4.2V, I_{VOUT} = 0mA, Battery Charger Off USB Suspend Modes, I_{VOUT} = 250µA		3.4 4.5	BAT + 0.3 4.6	4.7 4.7	V V
f_{OSC}	Switching Frequency			1.8	2.25	2.7	MHz
$R_{PMOS\_POWERPATH}$	PMOS On-Resistance				0.18		Ω
$R_{NMOS\_POWERPATH}$	NMOS On-Resistance				0.30		Ω
$I_{PEAK\_POWERPATH}$	Peak Inductor Current Limit	1× Mode (Note 5) 5× Mode (Note 5) 10× Mode (Note 5)			1 2 3		A A A
R_{SUSP}	Suspend LDO Output Resistance	Closed Loop			10		Ω
PowerPath Switching Regulator—Step-Up Mode (USB On-the-Go)							
V_{BUS}	Output Voltage	0mA ≤ I_{VBUS} ≤ 500mA, V_{OUT} > 3.2V		4.75		5.25	V
V_{OUT}	Input Voltage			2.9		5.5	V
I_{VBUS}	Output Current Limit		●	550	680		mA
I_{PEAK}	Peak Inductor Current Limit	(Note 5)			1.8		A
I_{OTGQ}	V_{OUT} Quiescent Current	V_{OUT} = 3.8V, I_{VBUS} = 0mA (Note 6)			1.38		mA
V_{CLPROG}	Output Current Limit Servo Voltage				1.15		V
$V_{OUT(UVLO)}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising			2.5	2.6 2.8	 2.9	V V
$t_{SCFAULT}$	Short-Circuit Fault Delay	V_{BUS} < 4V and PMOS Switch Off			7.2		ms
Bat-Track Switching Regulator Control							
V_{WALL}	Absolute WALL Input Threshold	Rising Threshold Hysteresis		4.2	4.3 1.1	4.4	V V
ΔV_{WALL}	Differential WALL Input Threshold	WALL-BAT Falling Hysteresis		0	30 60	45	mV mV
V_{OUT}	Regulation Target Under V_C Control			3.55	BAT + 0.3		V
I_{WALLQ}	WALL Quiescent Current				400		µA
$R_{\overline{ACPR}}$	$\overline{ACPR}$ Pull-Down Strength				150		Ω
$V_{H\overline{ACPR}}$	$\overline{ACPR}$ High Voltage				V_{OUT}		V
$V_{L\overline{ACPR}}$	$\overline{ACPR}$ Low Voltage				0		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overvoltage Protection							
$V_{OVCUTOFF}$	Overvoltage Protection Threshold	With 6.2k Series Resistor		6.1	6.35	6.7	V
V_{OVGATE}	OVGATE Output Voltage	$V_{OVSENS} < V_{OVCUTOFF}$ $V_{OVSENS} > V_{OVCUTOFF}$			1.88•V_{OVSENS} 0	12	V V
t_{RISE}	OVGATE Time to Reach Regulation	OVGATE C_{LOAD} = 1nF			2.2		ms
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	LTC3576	 ●	4.179 4.165	4.200 4.200	4.221 4.235	V V
		LTC3576-1	 ●	4.079 4.065	4.100 4.100	4.121 4.135	V V
I_{CHG}	Constant Current Mode Charger Current	R_{PROG} = 1k R_{PROG} = 5k		980 185	1030 206	1065 223	mA mA
I_{BAT}	Battery Drain Current	$V_{BUS} > V_{UVLO}$, Suspend Mode, I_{VOUT} = 0µA			3.6	6	µA
		V_{BUS} = 0V, I_{VOUT} = 0µA (Ideal Diode Mode)			28	45	µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
V_{PROG_TRKL}	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
$V_{C/10}$	C/10 Threshold Voltage at PROG				100		mV
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1030		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}, R_{PROG} = 1k			100		mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3.0	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				135		mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts When $V_{BAT} = V_{FLOAT}$		3.3	4	5	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End of Charge Current Ratio	(Note 7)		0.085	0.1	0.112	mA/mA
$V_{\overline{CHRG}}$	$\overline{\text{CHRG}}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{\text{CHRG}}$ Pin Leakage Current	$V_{\overline{CHRG}}$ = 5V				1	µA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		75	76.5 1.6	78	%NTCBIAS %NTCBIAS
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		33.4	34.9 1.5	36.4	%NTCBIAS %NTCBIAS
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.7	1.7 50	2.7	%NTCBIAS mV
I_{NTC}	NTC Leakage Current	NTC = NTCBIAS = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage	I_{VOUT} = 10mA			15		mV
$R_{DROPOUT}$	Internal Diode On-Resistance Dropout	I_{VOUT} = 200mA			0.18		Ω
I_{MAX_DIODE}	Diode Current Limit			2			A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Always On 3.3V LDO Supply						
V_{LDO3V3}	Regulated Output Voltage	0mA < I_{LDO3V3} < 20mA	3.1	3.3	3.5	V
R_{CL_LDO3V3}	Closed-Loop Output Resistance			2.7		Ω
R_{OL_LDO3V3}	Dropout Output Resistance			23		Ω
Logic (I_{LIM0}, I_{LIM1}, EN1, EN2, EN3, ENOTG, and SCL, SDA when DV_{CC} = 0V)						
V_{IL}	Logic Low Input Voltage				0.4	V
V_{IH}	Logic High Input Voltage		1.2			V
I_{PD1}	I_{LIM0}, I_{LIM1}, EN1, EN2, EN3, ENOTG, SCL, SDA Pull-Down Current			2		µA
I^2C Port						
DV_{CC}	Input Supply		1.6		5.5	V
I_{DVCC}	DV_{CC} Current	SCL/SDA = 0kHz, DV_{CC} = 3.3V		0.5		µA
$V_{DVCC(UVLO)}$	DV_{CC} UVLO			1.0		V
ADDRESS	I^2C Address			0001001[0]		
V_{IH}, SDA, SCL	Input High Threshold		70			$\%DV_{CC}$
V_{IL}, SDA, SCL	Input Low Threshold				30	$\%DV_{CC}$
I_{PD2}, SDA, SCL	Pull-Down Current			2		µA
V_{OL}	Digital Output Low (SDA)	I_{SDA} = 3mA			0.4	V
f_{SCL}	Clock Operating Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
t_{HD_STA}	Hold Time After (Repeated) Start Condition		0.6			µs
t_{SU_STA}	Repeated Start Condition Setup Time		0.6			µs
t_{SU_STO}	Stop Condition Setup Time		0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output		0		900	ns
$t_{HD\_DAT(I)}$	Data Hold Time Input		0			ns
t_{SU_DAT}	Data Setup Time		100			ns
t_{LOW}	SCL Low Period		1.3			µs
t_{HIGH}	SCL High Period		0.6			µs
t_f	SDA/SCL Fall Time		20		300	ns
t_r	SDA/SCL Rise Time		20		300	ns
t_{SP}	Input Spike Suppression Pulse Width				50	ns
General Purpose Switching Regulators 1, 2 and 3						
$V_{IN1,2,3}$	Input Supply Voltage	(Note 8)	2.7		5.5	V
$V_{OUT(UVLO)}$	V_{OUT} UVLO—V_{OUT} Falling V_{OUT} UVLO—V_{OUT} Rising	$V_{IN1,2,3}$ Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled in UVLO	2.5	2.6 2.8	 2.9	V V
f_{OSC}	Switching Frequency		1.8	2.25	2.7	MHz
$I_{FB1,2,3}$	FBx Input Current	$V_{FB1,2,3}$ = 0.85V	–50		50	nA
D1,2,3	Maximum Duty Cycle		100			%
$R_{SW1,2,3\_PD}$	SWx Pull-Down in Shutdown			10		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{VIN1,2,3}$	Pulse-Skipping Mode Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			90		µA
	Burst Mode® Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			20	35	µA
	LDO Mode Input Current	$I_{OUT1,2,3}$ = 0µA (Note 9)			15	25	µA
	Shutdown Input Current Limit	$I_{OUT1,2,3}$ = 0µA, FB1,2,3 = 0V				1	µA
$V_{FBHIGH1,2,3}$	Maximum Servo Voltage	Full Scale (1,1,1,1) (Note 10)	●	0.78	0.80	0.82	V
$V_{FBLOW1,2,3}$	Minimum Servo Voltage	Zero Scale (0,0,0,0) (Note 10)		0.405	0.425	0.445	V
$V_{LSB1,2,3}$	$V_{FB1,2}$ Servo Voltage Step Size				25		mV
$R_{LDO\_CL1,2,3}$	LDO Mode Closed-Loop R_{OUT}	$V_{FB1,2,3}$ = $V_{OUT1,2\ 3}$ = 0.8V			0.25		Ω
$R_{LDO\_OL1,2,3}$	LDO Mode Open-Loop R_{OUT}	(Note 11)			2.5		Ω
General Purpose Switching Regulator 1 and 2							
$I_{LIM1,2}$	PMOS Switch Current Limit	Pulse-Skipping/Burst Mode Operation (Note 5)		600	900	1300	mA
$I_{OUT1,2}$	Available Output Current	LDO Mode		50			mA
$R_{P1,2}$	PMOS $R_{DS(ON)}$				0.6		Ω
$R_{N1,2}$	NMOS $R_{DS(ON)}$				0.7		Ω
General Purpose Switching Regulator 3							
I_{LIM3}	PMOS Switch Current Limit	Pulse-Skipping/Burst Mode Operation (Note 5)		1300	1800	2800	mA
I_{OUT3}	Available Output Current	LDO Mode		50			mA
R_{P3}	PMOS $R_{DS(ON)}$				0.18		Ω
R_{N3}	NMOS $R_{DS(ON)}$				0.3		Ω
$t_{\overline{RST3}}$	Power-On Reset Time for Switching Regulator	V_{FB3} Within 92% of Final Value to $\overline{RST3}$ Hi-Z			230		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3576E/LTC3576E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3576E/LTC3576E-1 include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Total input current is the sum of quiescent current, I_{VBUSQ}, and measured current given by V_{CLPROG}/R_{CLPROG} • (h_{CLPROG} + 1).

Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

Note 6: The bidirectional switcher's supply current is bootstrapped to V_{BUS} and in the application will reflect back to V_{OUT} by (V_{BUS}/V_{OUT}) • 1/efficiency. Total quiescent current is the sum of the current into the V_{OUT} pin plus the reflected current.

Note 7: $h_{C/10}$ is expressed as a fraction of the measured full charge current with indicated PROG resistor.

Note 8: V_{OUT} not in UVLO.

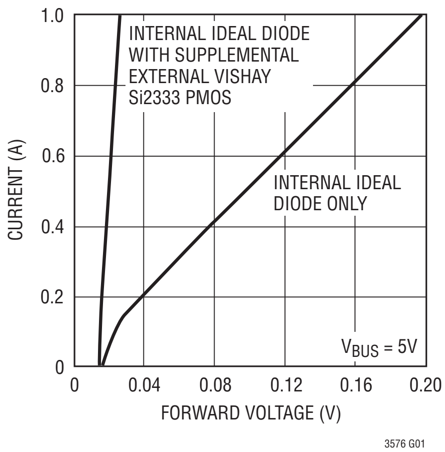
Note 9: FBx above regulation such that regulator is in sleep. Specification does not include resistive divider current reflected back to V_{INx}.

Note 10: Applies to pulse-skipping and Burst Mode operation only.

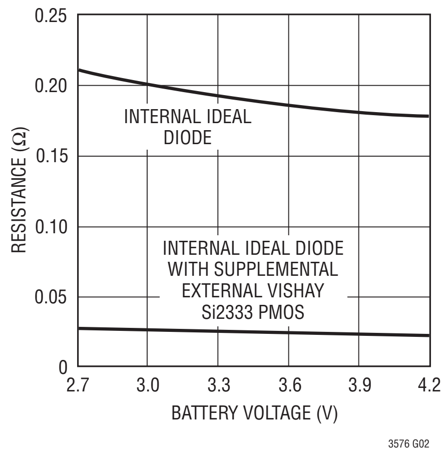
Note 11: Inductor series resistance adds to open-loop R_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

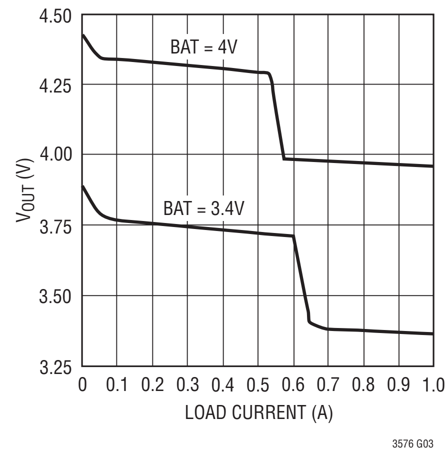
Ideal Diode V-I Characteristics



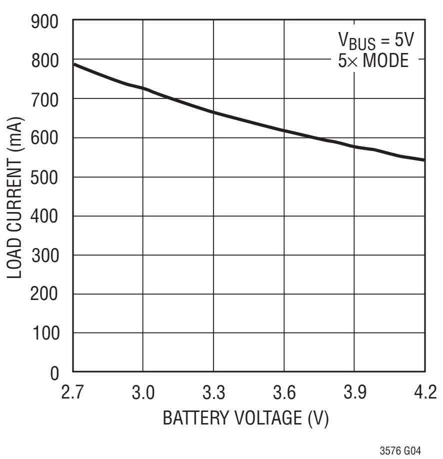
Ideal Diode Resistance vs Battery Voltage



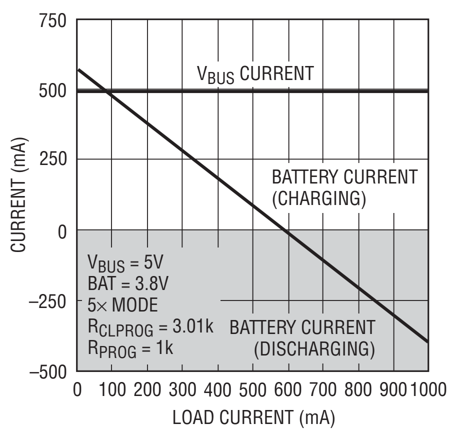
V_{OUT} Voltage vs Load Current (Battery Charger Disabled)



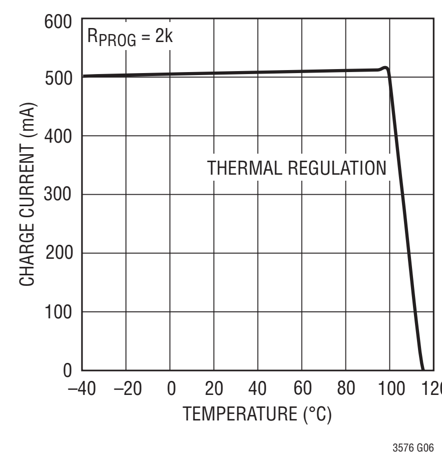
USB Limited Load Current vs Battery Voltage (Battery Charger Disabled)



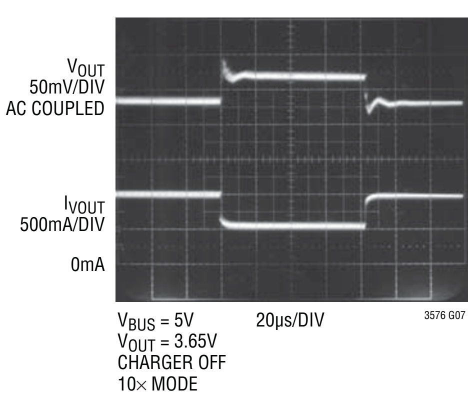
Battery and V_{BUS} Currents vs Load Current



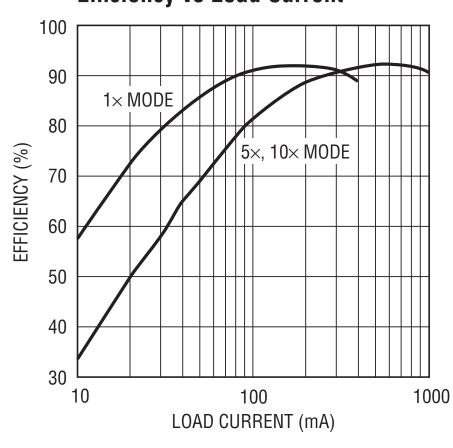
Battery Charge Current vs Temperature



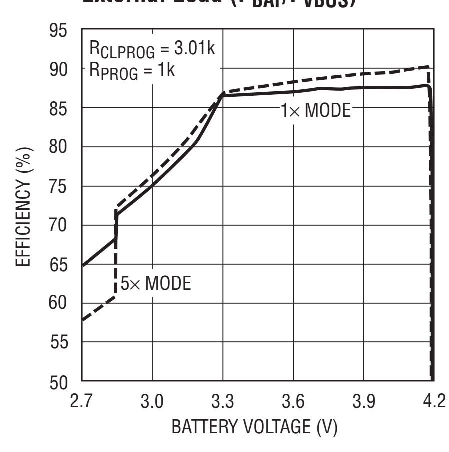
PowerPath Switching Regulator Transient Response



PowerPath Switching Regulator Efficiency vs Load Current

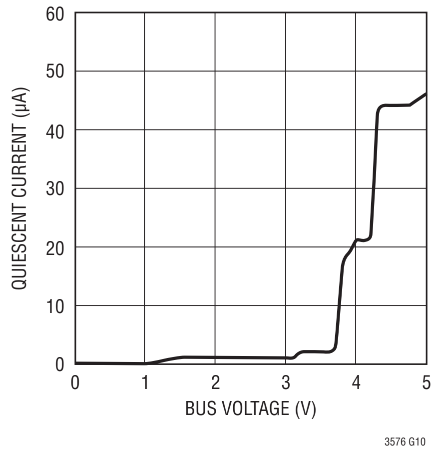


Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{VBUS})

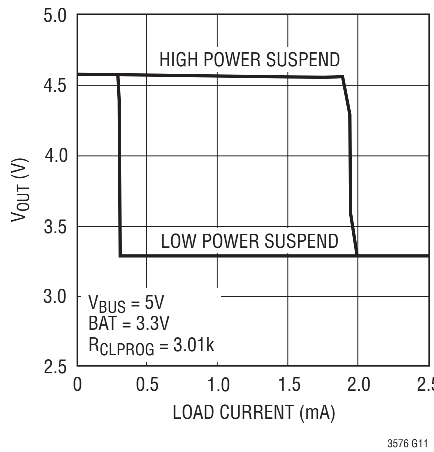


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

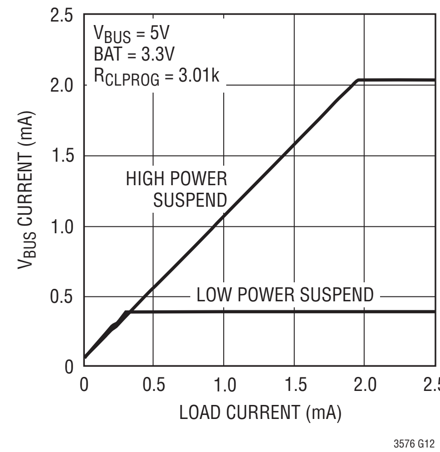
V_{BUS} Quiescent Current vs V_{BUS} Voltage (Suspend)



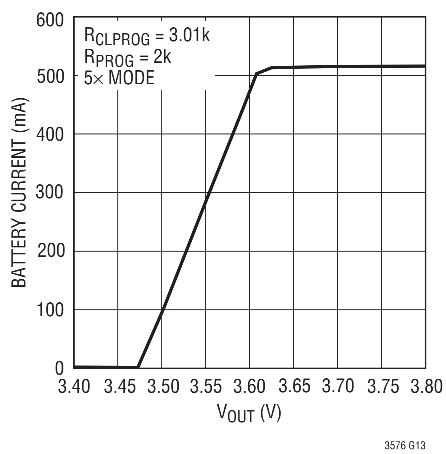
V_{OUT} Voltage vs Load Current in Suspend



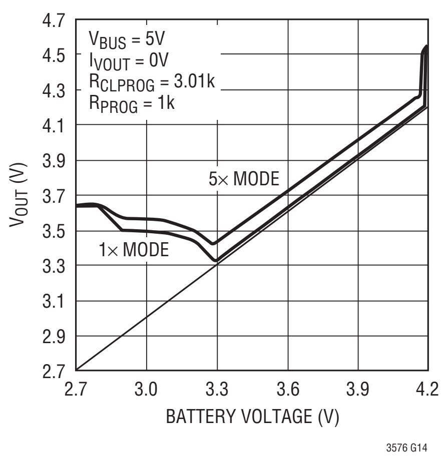
V_{BUS} Current vs Load Current in Suspend



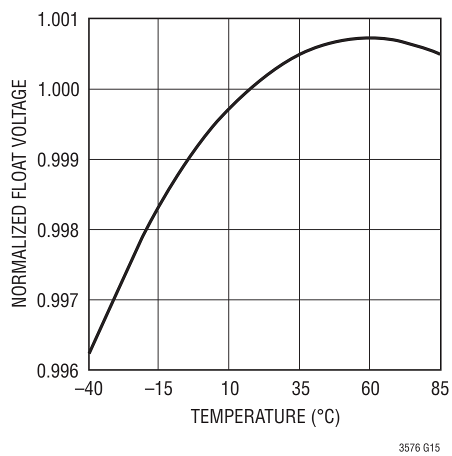
Battery Charge Current vs V_{OUT} Voltage



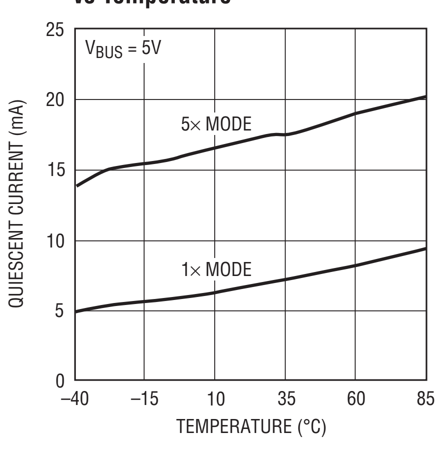
V_{OUT} Voltage vs Battery Voltage (Charger Overprogrammed)



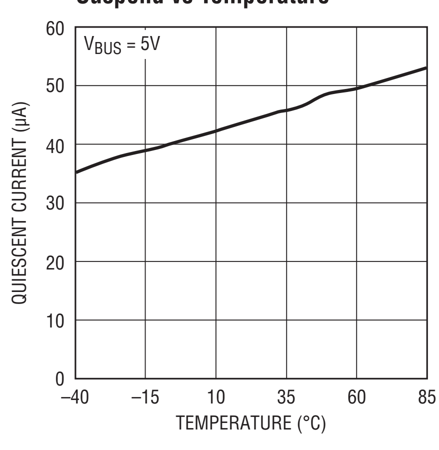
Normalized Battery Charger Float Voltage vs Temperature



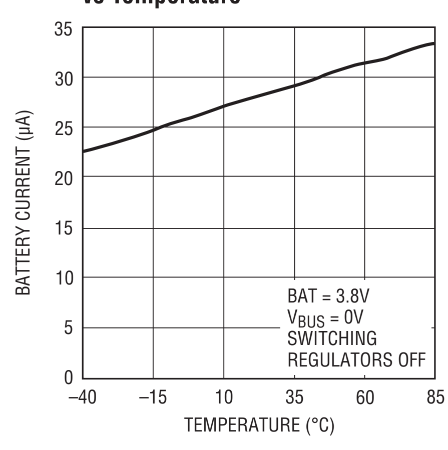
V_{BUS} Quiescent Current vs Temperature



V_{BUS} Quiescent Current in Suspend vs Temperature

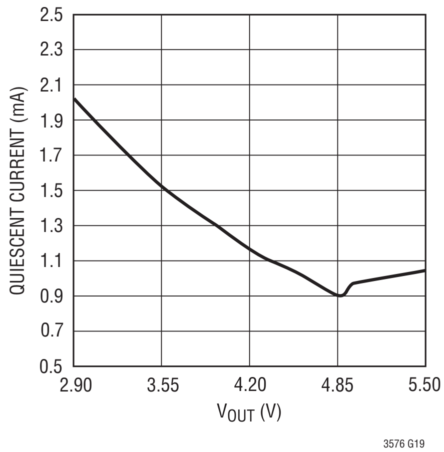


Battery Drain Current vs Temperature

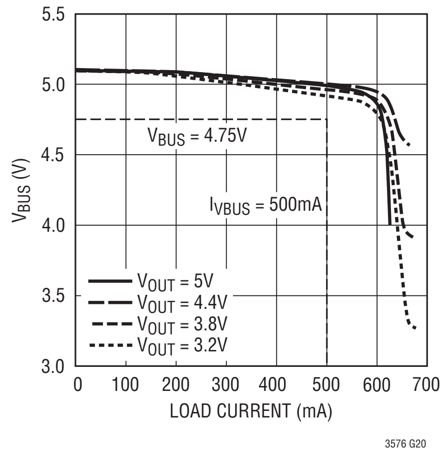


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

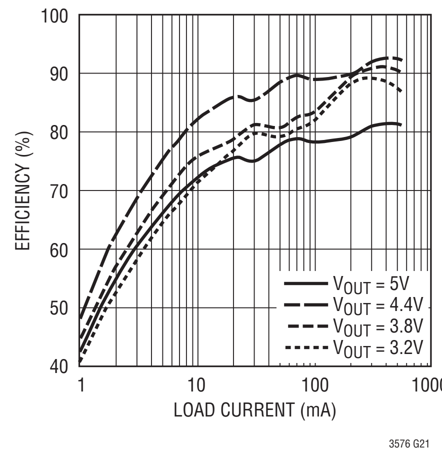
OTG Boost Quiescent Current vs V_{OUT} Voltage



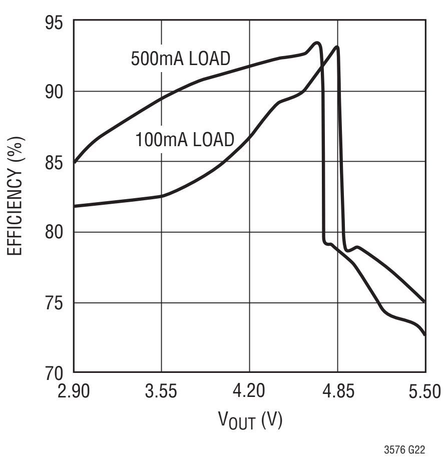
OTG Boost V_{BUS} Voltage vs Load Current



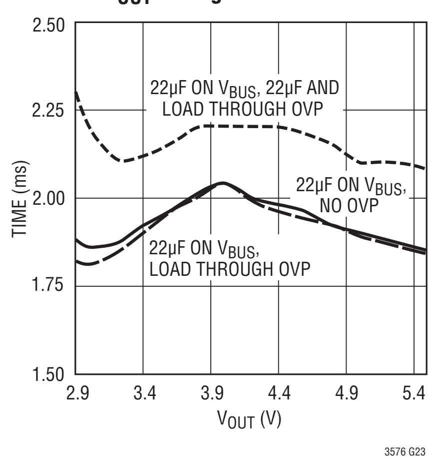
OTG Boost Efficiency vs Load Current



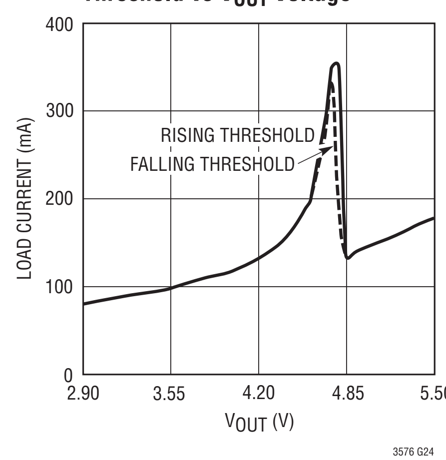
OTG Boost Efficiency vs V_{OUT} Voltage



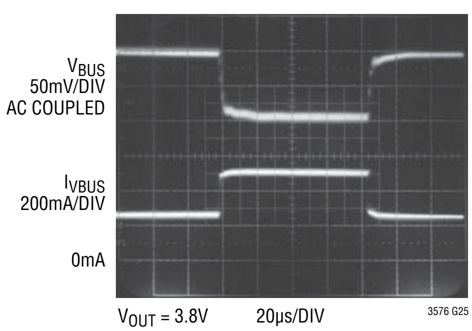
OTG Boost Start-Up Time into Current Source Load vs V_{OUT} Voltage



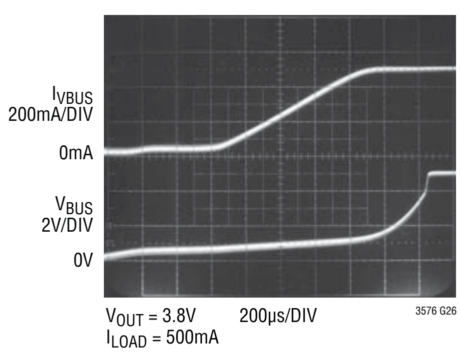
OTG Boost Burst Mode Current Threshold vs V_{OUT} Voltage



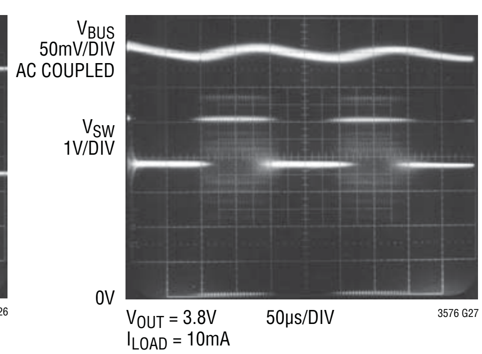
OTG Boost Transient Response



OTG Boost Start-Up into Current Source Load

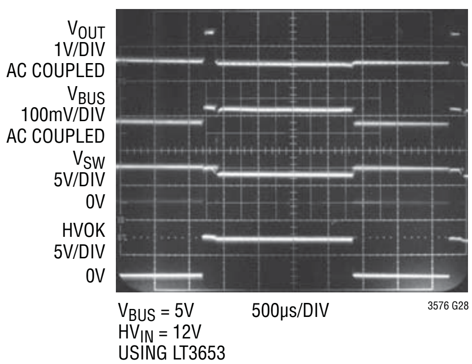


OTG Boost Burst Mode Operation

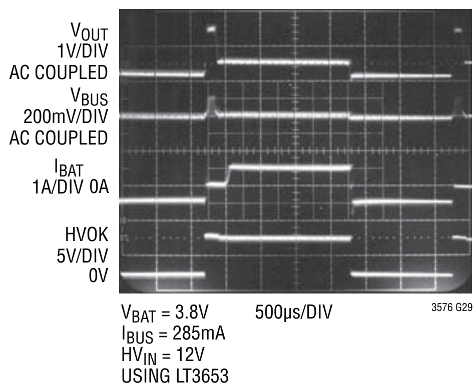


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

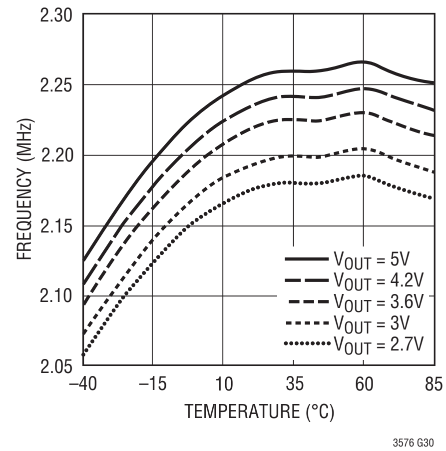
Battery Charging from USB-HV BUCK-USB



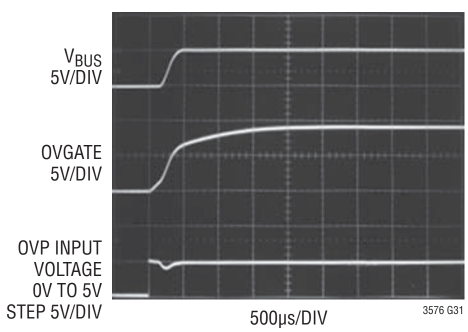
USB OTG from BAT-HV BUCK-BAT



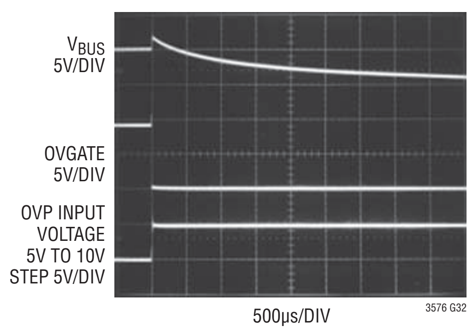
Oscillator Frequency vs Temperature



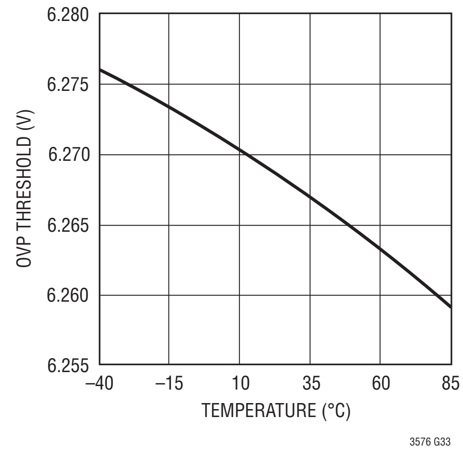
OVP Connect Waveform



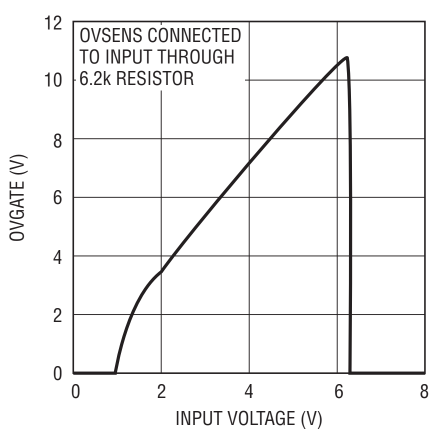
OVP Disconnect Waveform



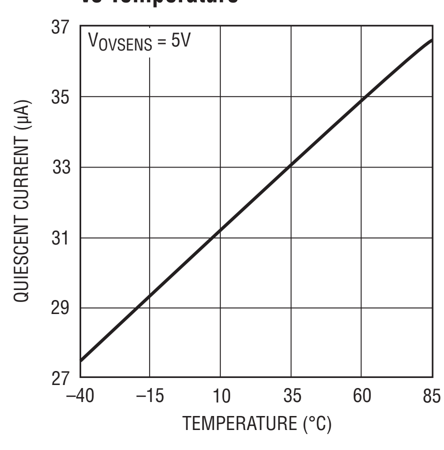
Rising OVP Threshold vs Temperature



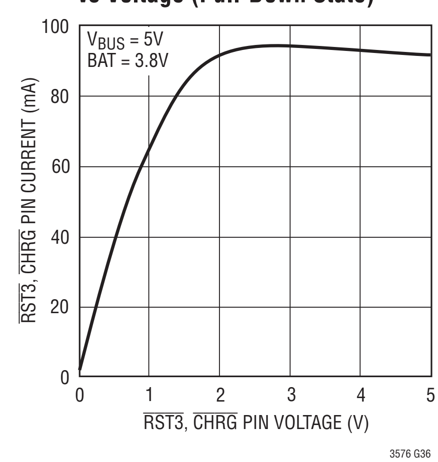
OVGATE vs OVSENS



OVGATE Quiescent Current vs Temperature

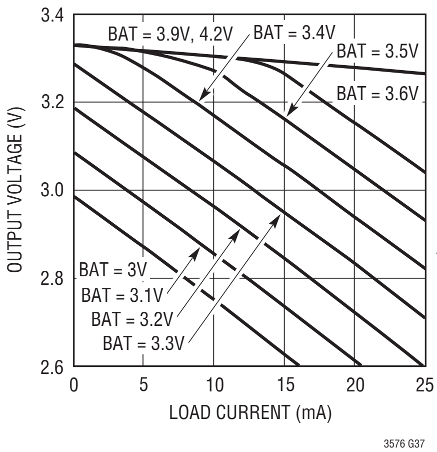


$\overline{RST3}$, $\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)

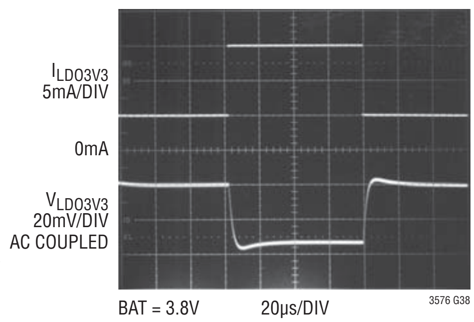


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

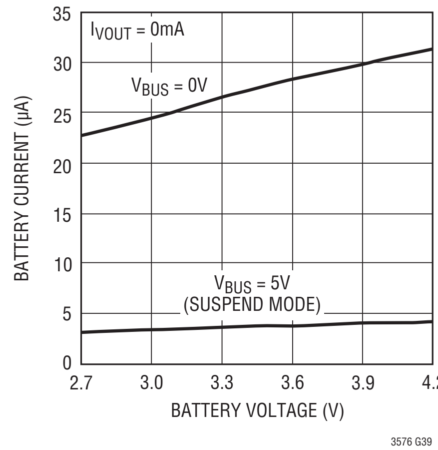
3.3V LDO Output Voltage vs Load Current, V_{BUS} = 0V



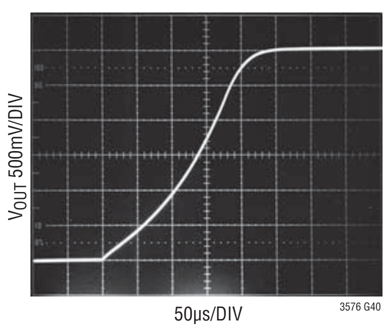
3.3V LDO Step Response (5mA to 15mA)



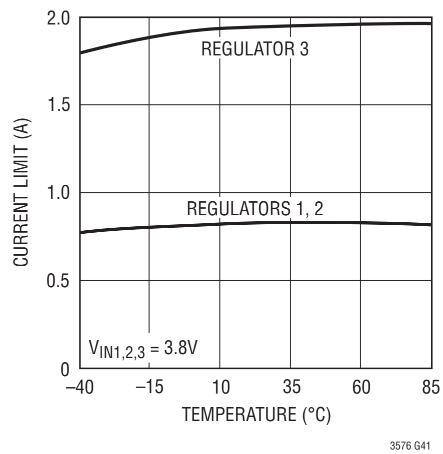
Battery Drain Current vs Battery Voltage



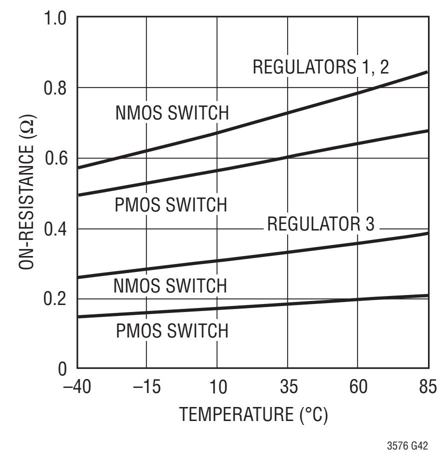
Switching Regulator Soft-Start Waveform



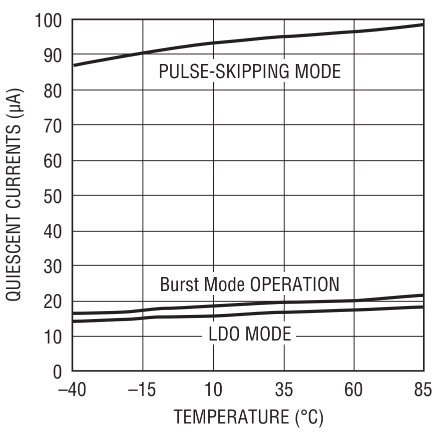
Switching Regulator Current Limit vs Temperature



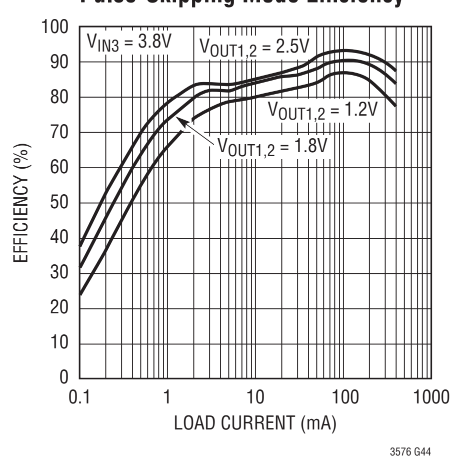
$R_{DS(ON)}$ for Switching Regulator Power Switches vs Temperature



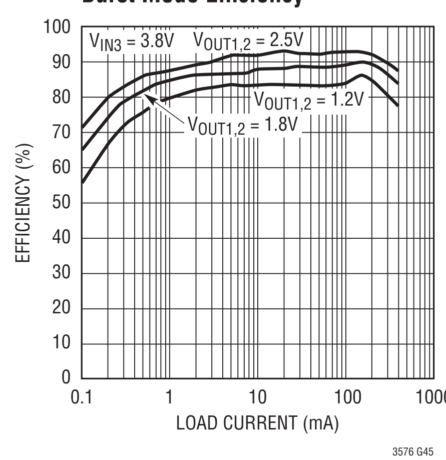
Switching Regulator Low Power Quiescent Currents vs Temperature



Switching Regulators 1, 2 Pulse-Skipping Mode Efficiency

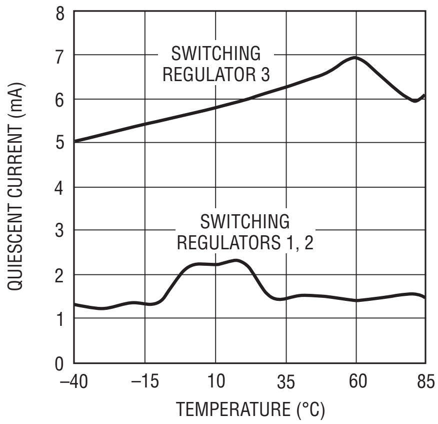


Switching Regulators 1, 2 Burst Mode Efficiency



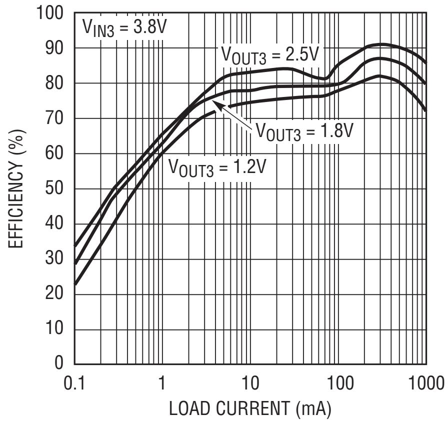
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

Switching Regulator Constant Frequency Quiescent Currents



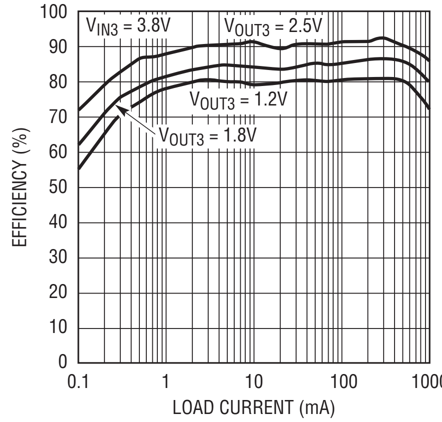
3576 G46

Switching Regulator 3 Pulse-Skipping Mode Efficiency



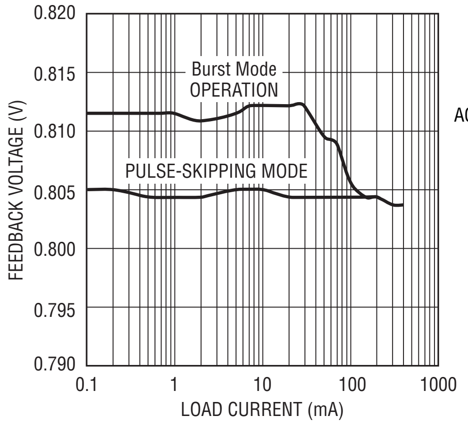
3576 G47

Switching Regulator 3 Burst Mode Efficiency



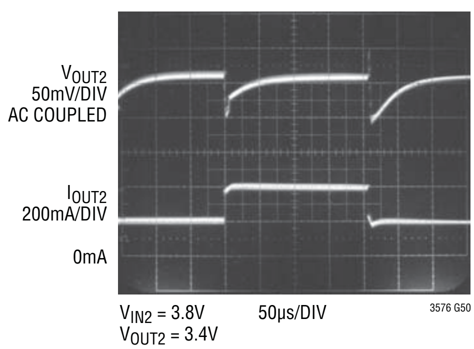
3576 G48

Switching Regulators 1, 2 Feedback Voltage vs Load Current



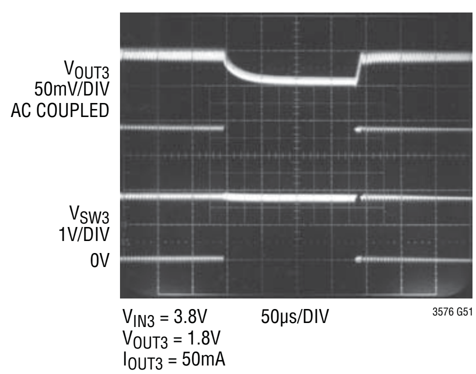
3576 G49

Switching Regulators 1, 2 Transient Response



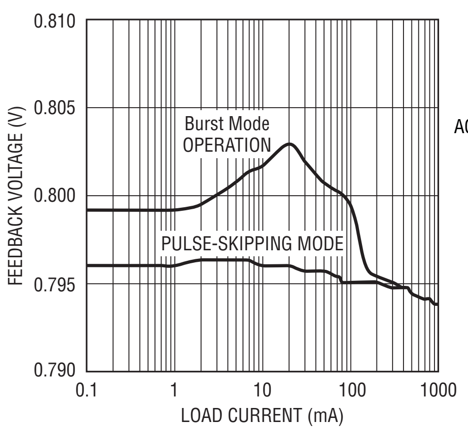
3576 G50

Switching Regulator Mode Transition, Pulse-Skipping-LDO-Pulse-Skipping



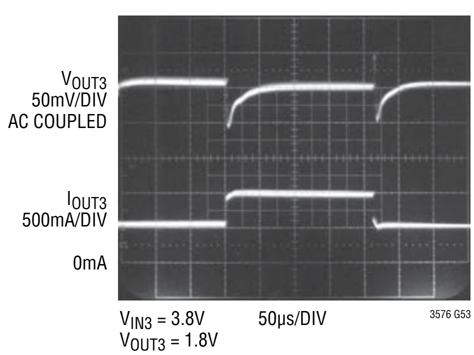
3576 G51

Switching Regulator 3 Feedback Voltage vs Load Current



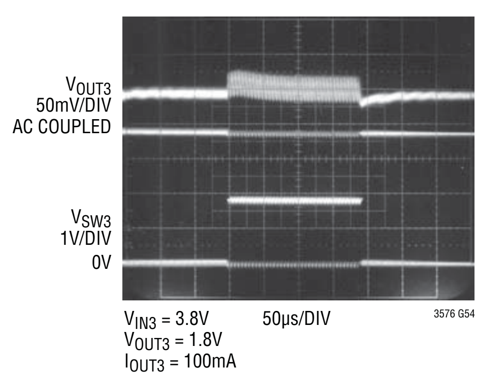
3576 G52

Switching Regulator 3 Transient Response



3576 G53

Switching Regulator Mode Transition, Pulse-Skipping–Burst Mode Operation–Pulse-Skipping



3576 G54

PIN FUNCTIONS

CLPROG (Pin 1): USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn or sourced from the V_{BUS} pins. A precise fraction, h_{CLPROG}, of the V_{BUS} current is sent to the CLPROG pin when the PMOS switch of the PowerPath switching regulator is on. The switching regulator delivers power until the CLPROG pin reaches 1.18V in step-down mode and 1.15V in step-up mode. When the switching regulator is in step-down mode, CLPROG is used to regulate the average input current. Several V_{BUS} current limit settings are available via user input which will typically correspond to the 500mA and 100mA USB specifications. When the switching regulator is in step-up mode (USB on-the-go), CLPROG is used to limit the average output current to 680mA. A multilayer ceramic averaging capacitor or R-C network is required at CLPROG for filtering.

LDO3V3 (Pin 2): 3.3V LDO Output Pin. This pin provides a regulated always-on 3.3V supply voltage. LDO3V3 gets its power from V_{OUT}. It may be used for light loads such as a watchdog microprocessor or real time clock. A 1µF capacitor is required from LDO3V3 to ground. If the LDO3V3 output is not used it should be disabled by connecting it to V_{OUT}.

NTCBIAS (Pin 3): NTC Thermistor Bias Output. If NTC operation is desired, connect a bias resistor between NTCBIAS and NTC, and an NTC thermistor between NTC and GND. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

NTC (Pin 4): Input to the Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor, which is typically co-packaged with the battery, to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

OVGATE (Pin 5): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOS pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage to the LTC3576/LTC3576-1. OVGATE works in conjunction with OVSENS to provide this protection.

OVSENS (Pin 6): Overvoltage Protection Sense Input. OVSENS should be connected through a 6.2k resistor to the input power connector and the drain of an external N-channel MOS pass transistor. When the voltage on this pin exceeds $V_{OVCUTOFF}$, the OVGATE pin will be pulled to GND to disable the pass transistor and protect the LTC3576/LTC3576-1. The OVSENS pin shunts current during an overvoltage transient in order to keep the pin voltage at 6V.

FB1 (Pin 7): Feedback Input for Switching Regulator 1. When regulator 1's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

V_{IN1} (Pin 8): Power Input for Switching Regulator 1. This pin will generally be connected to V_{OUT}. A 1µF MLCC capacitor is recommended on this pin.

SW1 (Pin 9): Power Transmission Pin for Switching Regulator 1.

EN1 (Pin 10): Logic Input. This logic input pin independently enables switching regulator 1. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

ENOTG (Pin 11): Logic Input. This logic input pin independently enables the bidirectional switching regulator to step up the voltage on V_{OUT} and provide a 5V output on V_{BUS} for USB on-the-go applications. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2µA internal pull-down current source.

PIN FUNCTIONS

DV_{CC} (Pin 12): Logic Supply for the I^2C Serial Port. If the serial port is not needed, it can be disabled by grounding DV_{CC}. When DV_{CC} is grounded, the I^2C bits are set to their default values. See Table 3.

SCL (Pin 13): Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SCL pin is equivalent to the C2, C4 and C6 bits in the I^2C serial port. SCL in conjunction with SDA determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 3 and 5. Has a 2μA internal pull-down current source.

SDA (Pin 14): Data Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{CC}. If DV_{CC} is grounded, the SDA pin is equivalent to the C3, C5 and C7 bits in the I^2C serial port. SDA in conjunction with SCL determine the operating modes of switching regulators 1, 2 and 3 when DV_{CC} is grounded. See Tables 3 and 5. Has a 2μA internal pull-down current source.

NC (Pin 15): Unconnected Pin. This pin is not connected internally to the part. It is permissible to tie this pin to V_{IN3} in order to make the V_{IN3} PCB trace wider.

V_{IN3} (Pin 16): Power Input for Switching Regulator 3. This pin will generally be connected to V_{OUT}. A 1μF MLCC capacitor is recommended on this pin.

SW3 (Pin 17): Power Transmission Pin for Switching Regulator 3.

NC (Pin 18): Unconnected Pin. This pin is not connected internally to the part. It is permissible to tie this pin to SW3 in order to make the SW3 PCB trace wider.

EN3 (Pin 19): Logic Input. This logic input pin independently enables switching regulator 3. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2μA internal pull-down current source.

FB3 (Pin 20): Feedback Input for Switching Regulator 3. When regulator 3's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

$\overline{RST3}$ (Pin 21): Logic Output. This in an open-drain output which indicates that switching regulator 3 has settled to its final value. It can be used as a power-on reset for the primary microprocessor or to enable the other switching regulators for supply sequencing.

EN2 (Pin 22): Logic Input. This logic input pin independently enables switching regulator 2. Active high. This pin is logically ORed with its corresponding bit in the I^2C serial port. See Table 3. Has a 2μA internal pull-down current source.

SW2 (Pin 23): Power Transmission Pin for Switching Regulator 2.

V_{IN2} (Pin 24): Power Input for Switching Regulator 2. This pin will generally be connected to V_{OUT}. A 1μF MLCC capacitor is recommended on this pin.

FB2 (Pin 25): Feedback Input for Switching Regulator 2. When regulator 2's control loop is complete, this pin servos to 1 of 16 possible set points based on the commanded value from the I^2C serial port. See Table 4.

V_C (Pin 26): Bat-Track External Switching Regulator Control Output. This pin drives the V_C pin of an external Linear Technology step-down switching regulator. An external P-channel MOSFET is sometimes required to provide power to V_{OUT} with its gate tied to the $\overline{ACPR}$ pin (see the Applications Information section). In concert with WALL and $\overline{ACPR}$, it will regulate V_{OUT} to maximize battery charger efficiency

WALL (Pin 27): External Power Source Sense Input. WALL should be connected to the output of the external high voltage switching regulator and to the drain of an external P-channel MOSFET if used. It is used to determine when power is applied to the external regulator. When power is detected, $\overline{ACPR}$ is driven low and the USB input is automatically disabled. Pulling this pin above 4.3V enables the V_C pin.

PIN FUNCTIONS

$\overline{ACPR}$ (Pin 28): External Power Source Present Output (Active Low). $\overline{ACPR}$ indicates that the output of the external high voltage step-down switching regulator is suitable for use by the LTC3576/LTC3576-1. It should be connected to the gate of an external P-channel MOSFET whose source is connected to V_{OUT} and whose drain is connected to WALL. $\overline{ACPR}$ has a high level of V_{OUT} and a low level of GND. The USB bidirectional switcher is disabled when $\overline{ACPR}$ is low.

PROG (Pin 29): Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

$\overline{CHRG}$ (Pin 30): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible charger states are represented by $\overline{CHRG}$: charging, not charging, unresponsive battery and battery temperature out of range. In addition, $\overline{CHRG}$ is used to indicate whether there is a short-circuit condition on V_{BUS} when the bidirectional switching regulator is in step-up mode (on-the-go). $\overline{CHRG}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. See Table 1. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

IDGATE (Pin 31): Ideal Diode Amplifier Output. This pin controls the gate of an optional external P-channel MOSFET used as an ideal diode between V_{OUT} and BAT. The external ideal diode operates in parallel with the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. If the external ideal diode MOSFET is not used, IDGATE should be left floating.

BAT (Pin 32): Single Cell Li-Ion Battery Pin. Depending on available V_{BUS} power, a Li-Ion battery on BAT will either deliver power to V_{OUT} through the ideal diode or be charged from V_{OUT} via the battery charger.

V_{OUT} (Pin 33): Output Voltage of the Bidirectional PowerPath Switching Regulator in step-down mode and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3576/LTC3576-1 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. In on-the-go mode, this pin delivers power to V_{BUS} via the SW pin. V_{OUT} should be bypassed with a low impedance ceramic capacitor.

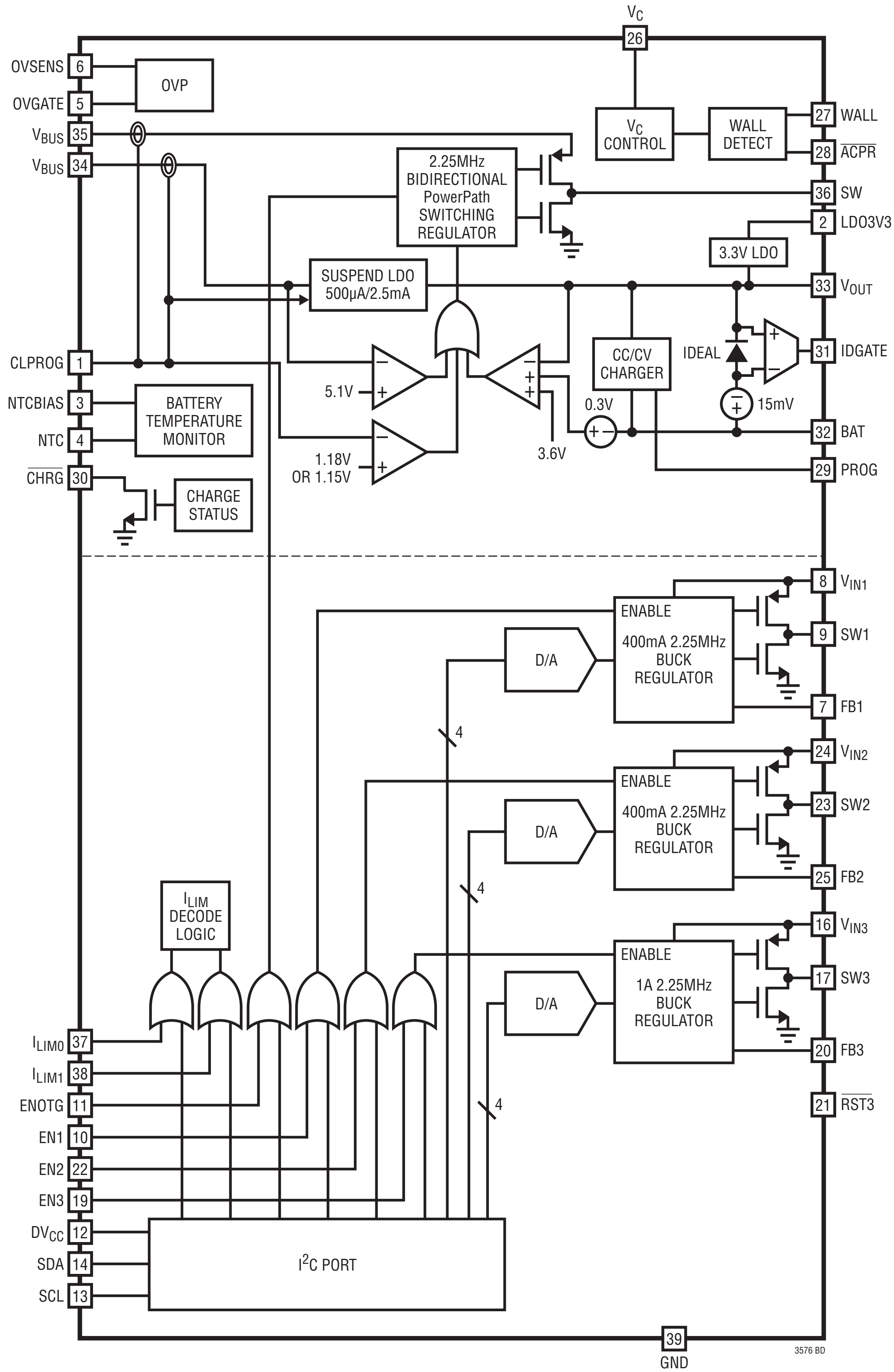
V_{BUS} (Pins 34, 35): Power Pins. These pins deliver power to V_{OUT} via the SW pin by drawing controlled current from a DC source such as a USB port or DC output wall adapter. In on-the-go mode these pins provide power to external loads. Tie the two V_{BUS} pins together at the part and bypass with a low impedance multilayer ceramic capacitor.

SW (Pin 36): The SW pin transfers power between V_{BUS} and V_{OUT} via the bidirectional switching regulator. See the Applications Information section for a discussion of inductance value and current rating.

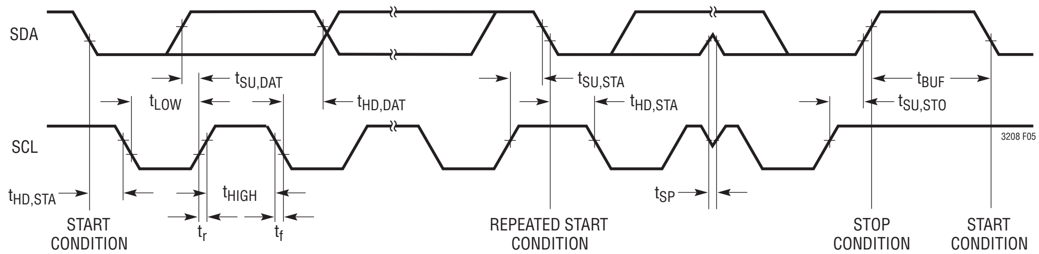
I_{LIM0}, I_{LIM1} (Pins 37, 38): I_{LIM0} and I_{LIM1} control the current limit of the PowerPath switching regulator. See Table 1. Both the I_{LIM0} and I_{LIM1} pins are logically ORed with their corresponding bits in the I^2C serial port. See Tables 3 and 6. Each has a 2μA internal pull-down current source.

Exposed Pad (Pin 39): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3576/LTC3576-1.

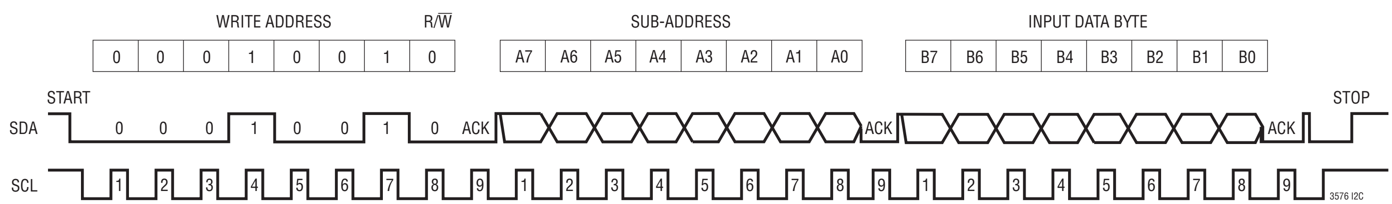
BLOCK DIAGRAM



TIMING DIAGRAM



I²C WRITE PROTOCOL



OPERATION

Introduction

The LTC3576/LTC3576-1 are highly integrated power management ICs designed to make optimal use of the power available from a variety of sources, while minimizing power dissipation and easing thermal budgeting constraints. They include a high efficiency bidirectional PowerPath switching regulator, a controller for an external high voltage step-down switching regulator, a battery charger, an ideal diode, an always-on LDO, an overvoltage protection circuit and three general purpose step-down switching regulators. The entire chip is controlled by either direct digital control or by an I^2C serial port or both.

The innovative PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application.

When acting as a step-down converter, the LTC3576/LTC3576-1's bidirectional switching regulator takes power from USB, wall adapters, or other 5V sources and provides power to the application and efficiently charges the battery using Bat-Track. Because power is conserved the LTC3576/LTC3576-1 allow the load current on V_{OUT} to exceed the current drawn by the USB port making maximum use of the allowable USB power for battery charging. For USB compatibility the switching regulator includes a precision average input current limit. The PowerPath switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

Additionally, the bidirectional switching regulator can also operate as a 5V synchronous step-up converter taking power from V_{OUT} and delivering up to 500mA to V_{BUS} without the need for any additional external components. This enables systems with USB dual-role transceivers to function as USB on-the-go dual-role devices. True output disconnect and average output current limit features are included for short-circuit protection.

For automotive, firewire, and other high voltage applications, the LTC3576/LTC3576-1 provide Bat-Track control of an external LTC step-down switching regulator to maximize battery charger efficiency and minimize heat production. When power is available from both the USB and an auxiliary input, the auxiliary input is given priority.

The LTC3576/LTC3576-1 contain both an internal 180mΩ ideal diode as well as an ideal diode controller for use with an optional external P-channel MOSFET. The ideal diode(s) from BAT to V_{OUT} guarantee that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS} or WALL.

An always-on LDO provides a regulated 3.3V from available power at V_{OUT}. Drawing very little quiescent current, this LDO will be on at all times and can be used to supply 20mA.

The LTC3576/LTC3576-1 feature an overvoltage protection circuit which is designed to work with an external N-channel MOSFET to prevent damage to their inputs caused by accidental application of high voltage.

To prevent battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides either low power or high power USB suspend current to the application.

The three general purpose switching regulators can be independently enabled either by direct digital control or by operating the I^2C serial port. Under I^2C control, all three switching regulators have adjustable set points so that voltages can be reduced when high processor performance is not needed. Along with constant frequency PWM mode, all three switching regulators have automatic Burst Mode operation and LDO modes for significantly reduced quiescent current under light load conditions.

OPERATION

Bidirectional PowerPath Switching Regulator—Step-Down Mode

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant frequency bidirectional switching regulator operating in step-down mode. V_{OUT} drives the combination of the external load (step-down switching regulators 1, 2 and 3) and the battery charger. To meet the maximum USB load specification, the switching regulator contains a measurement and control system that ensures that the average input current remains below the level programmed at CLPROG.

If the combined load does not cause the switching regulator to reach the programmed input current limit, V_{OUT} will track approximately 0.3V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power flow in step-down mode.

If the combined external load plus battery charge current is large enough to cause the switching regulator to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB current, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at V_{OUT} exceeds the programmed power from V_{BUS}, load current will be drawn from the battery via the ideal diode(s) even when the battery charger is enabled.

The current out of CLPROG is a precise fraction of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches the programmed limit, CLPROG reaches 1.18V and power delivered by the switching regulator is held constant.

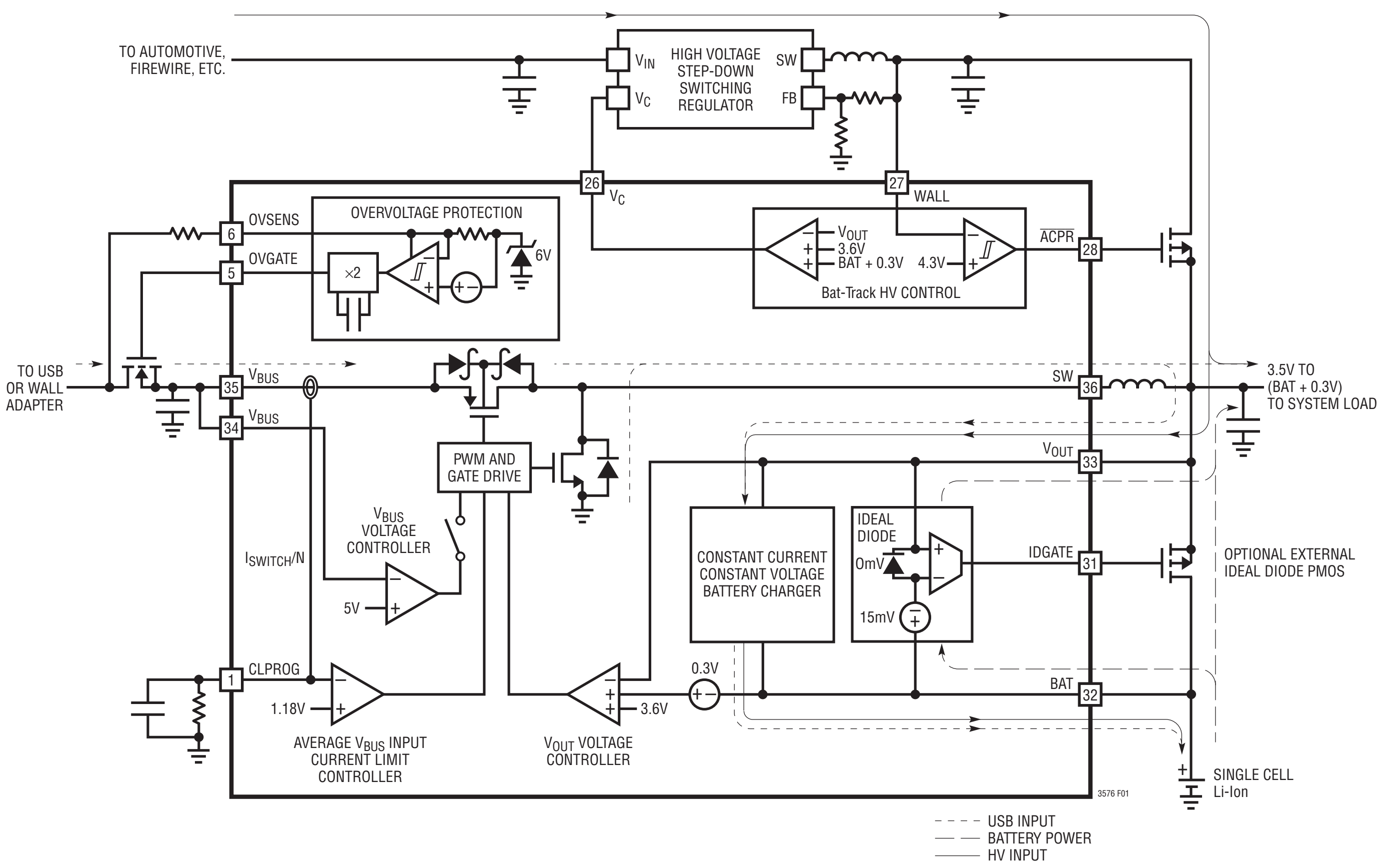


Figure 1. PowerPath Block Diagram—Power Available from USB/Wall Adapter

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The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins or by the I^2C serial port. The input current limit has five possible settings ranging from the USB suspend limit of 500µA up to 1A for wall adapter applications. Two of these settings are specifically intended for use in the 100mA and 500mA USB applications. Refer to Table 1 for current limit settings using the I_{LIM0} and I_{LIM1} pins and Table 6 for current limit settings using the I^2C port.

Table 1. USB Current Limit Settings Using I_{LIM0} and I_{LIM1}

I_{LIM1}	I_{LIM0}	USB SETTING
0	0	1× Mode (USB 100mA Limit)
0	1	10× Mode (Wall 1A Limit)
1	0	Low Power Suspend (USB 500µA Limit)
1	1	5× Mode (USB 500mA Limit)

When the switching regulator is activated, the average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet (h_{CLPROG} + 1)$$

where I_{VBUSQ} is the quiescent current of the LTC3576/LTC3576-1, V_{CLPROG} is the CLPROG servo voltage in current limit, R_{CLPROG} is the value of the programming resistor and h_{CLPROG} is the ratio of the measured current at V_{BUS} to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of h_{CLPROG}, V_{CLPROG} and I_{VBUSQ}. Given worst-case circuit tolerances, the USB specification for the average input current in 100mA or 500mA mode will not be violated, provided that R_{CLPROG} is 3.01k or greater.

While not in current limit, the switching regulator's Bat-Track feature will set V_{OUT} to approximately 300mV above the voltage at BAT. However, if the voltage at BAT is below 3.3V, and the load requirement does not cause the switching regulator to exceed its current limit, V_{OUT} will regulate at a fixed 3.6V as shown in Figure 2. This instant-on operation will allow a portable product to run immediately when power is applied without waiting for the battery to charge. If the load does exceed the current limit at V_{BUS}, V_{OUT} will range between the no-load voltage and slightly below the battery voltage, indicated by the shaded region of Figure 2.

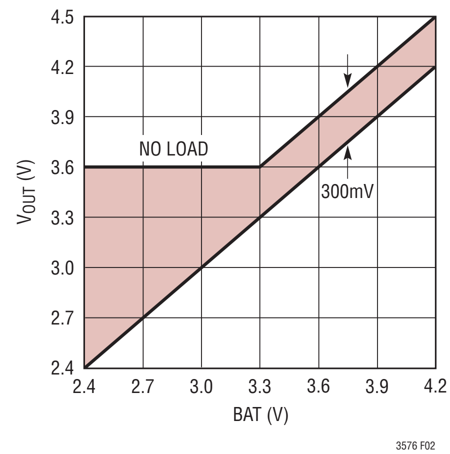

Figure 2. V_{OUT} vs BAT

For very low-battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull V_{OUT} below the 3.6V instant-on voltage. To prevent V_{OUT} from falling below this level, an undervoltage circuit automatically detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized while allowing as much battery charge current as possible. See Battery Charger Over Programming in the Applications Information section.

The voltage regulation loop is compensated by the capacitance on V_{OUT}. A 10µF MLCC capacitor is required for loop stability. Additional capacitance beyond this value will improve transient response.

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the switching regulator off until V_{BUS} rises above 4.30V and is about 200mV above the battery voltage. Hysteresis on the UVLO turns off the regulator if V_{BUS} falls below 4V or to within 50mV of the battery voltage. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode(s).

Bidirectional PowerPath Switching Regulator—Step-Up Mode

For USB on-the-go applications, the bidirectional PowerPath switching regulator acts as a step-up converter to deliver power from V_{OUT} to V_{BUS}. The power from V_{OUT} can come from the battery or the output of the external

OPERATION

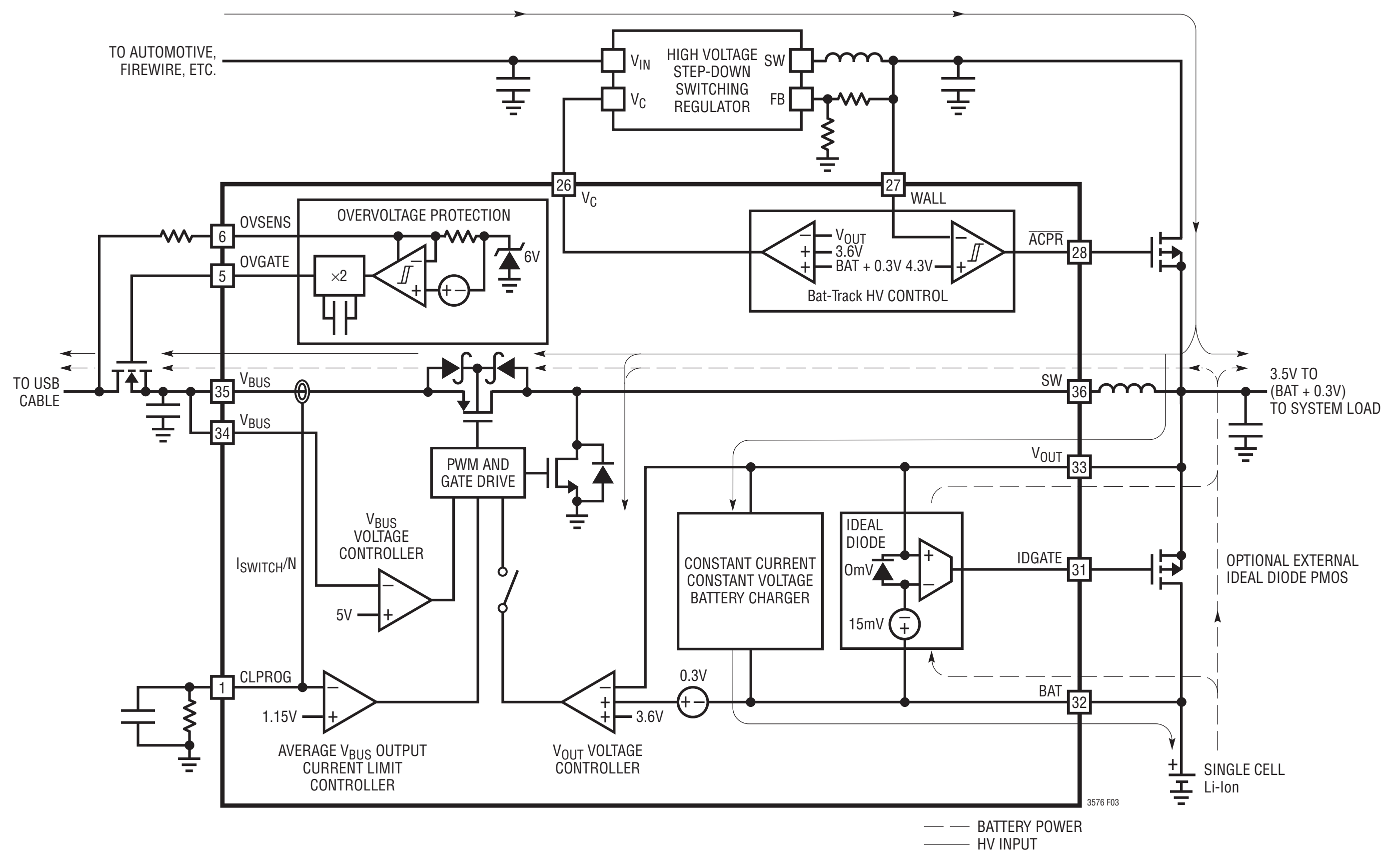

Figure 3. PowerPath Block Diagram—USB On-the-Go

high voltage switching regulator. As a step-up converter, the bidirectional switching regulator produces 5V on V_{BUS} and is capable of delivering at least 500mA. USB on-the-go can be enabled by either the external control pin, ENOTG, or via I^2C. Figure 3 shows the power flow in step-up mode.

An undervoltage lockout circuit monitors V_{OUT} and prevents step-up conversion until V_{OUT} rises above 2.8V. To prevent backdriving of V_{BUS} when input power is available, the V_{BUS} undervoltage lockout circuit prevents step-up conversion if V_{BUS} is greater than 4.3V at the time step-up mode is enabled. The switching regulator is also designed to allow true output disconnect by eliminating body diode conduction of the internal PMOS switch. This allows V_{BUS} to go to zero volts during a short-circuit condition or while shut down, drawing zero current from V_{OUT}.

The voltage regulation loop is compensated by the capacitance on V_{BUS}. A 4.7µF MLCC is required for loop stability. Additional capacitance beyond this value will improve transient response. The V_{BUS} voltage has approximately 3% load regulation up to an output current of 500mA. At light loads, the switching regulator goes into Burst Mode operation. The regulator will deliver power to V_{BUS} until it reaches 5.1V after which the NMOS and PMOS switches shut off. The regulator delivers power again to V_{BUS} once it falls below 5.1V.

The switching regulator features both peak inductor and average output current limit. The peak current mode architecture limits peak inductor current on a cycle-by-cycle basis. The peak current limit is equal to $V_{BUS}/2\Omega$ to a maximum of 1.8A so that in the event of a sudden short circuit, the current limit will fold back to a lower value. In step-up mode, the voltage on CLPROG represents the average output current of the switching regulator when a programming resistor and an averaging capacitor are connected from CLPROG to GND. With a 3.01k resistor on CLPROG, the bidirectional switching regulator has an output current limit of 680mA. As the output current ap-

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proaches this limit CLPROG servos to 1.15V and V_{BUS} falls rapidly to V_{OUT}. When V_{BUS} is close to V_{OUT} there may not be sufficient negative slope on the inductor current when the PMOS switch is on to balance the rise in the inductor current when the NMOS switch is on. This will cause the inductor current to run away and the voltage on CLPROG to rise. When CLPROG reaches 1.2V the switching of the synchronous PMOS is terminated and V_{OUT} is applied statically to its gate. This ensures that the inductor current will have sufficient negative slope during the time current is flowing to the output. The PMOS will resume switching when CLPROG drops down to 1.15V.

The LTC3576/LTC3576-1 maintain voltage regulation even if V_{OUT} is above V_{BUS}. This is achieved by disabling the PMOS switch. The PMOS switch is enabled when V_{BUS} rises above V_{OUT} + 180mV and is disabled when it falls below V_{OUT} + 70mV to prevent the inductor current from running away when not in current limit. Since the PMOS no longer acts as a low impedance switch in this mode, there will be more power dissipation within the IC. This will cause a sharp drop in efficiency.

If V_{BUS} is less than 4V and the PMOS switch is disabled for more than 7.2ms a short-circuit fault will be declared and the part will shut off. The $\overline{CHRG}$ pin will blink at 35kHz with a duty cycle that varies between 12% and 88% at a 4Hz rate. See Table 2. To re-enable step-up mode, the ENOTG pin or, with ENOTG grounded, the B0 bit in the I^2C port must be cycled low and then high.

Bat-Track Auxiliary High Voltage Switching Regulator Control

The WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage step-down switching regulator such as the LT®3480 or the LT3653 to minimize heat production when operating from higher voltage sources, as shown in Figures 1 and 3. Bat-Track control circuitry regulates the external switching regulator's output voltage to the larger of (BAT + 300mV) or 3.6V. This maximizes battery charger efficiency while still allowing instant-on operation when the battery is deeply discharged.

The feedback network of the high voltage regulator should be set to generate an output voltage between 4.5V and 5.5V. When high voltage is applied to the external regulator, WALL will rise toward this programmed output voltage. When WALL exceeds approximately 4.3V, $\overline{ACPR}$ is brought low and the Bat-Track control of the LTC3576/LTC3576-1 overdrives the local V_C control of the external high voltage step-down switching regulator. Therefore, once the Bat-Track control is enabled, the output voltage is set independent of the switching regulator feedback network.

Bat-Track control provides a significant efficiency advantage over the simple use of a 5V switching regulator output to drive the battery charger. With a 5V output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage switching regulator and 5V is the output voltage of the switching regulator. With a typical switching regulator efficiency of 87% and a typical battery voltage of 3.8V, the total battery charger efficiency is approximately 66%. Assuming a 1A charge current, 1.7W of power is dissipated just to charge the battery!

With Bat-Track, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{V_{BAT} + 0.3V}$$

With the same assumptions as above, the total battery charger efficiency is approximately 81%. This example works out to less than 1W of power dissipation, or almost 60% less heat.

See the Typical Applications section for complete circuits using the LT3480 and the LT3653 with Bat-Track control.

Ideal Diode(s) from BAT to V_{OUT}

The LTC3576/LTC3576-1 each have an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diode(s). Furthermore, if power to V_{BUS} (USB or wall adapter) is removed,

OPERATION

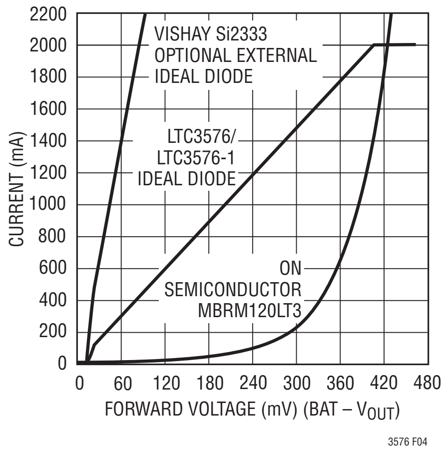

Figure 4. Ideal Diode V-I Characteristics

then all of the application power will be provided by the battery via the ideal diodes. The ideal diode(s) will be fast enough to keep V_{OUT} from drooping with only the storage capacitance required for the switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction.

To supplement the internal ideal diode, an external P-channel MOSFET may be added from BAT to V_{OUT}. The IDGATE pin of the LTC3576/LTC3576-1 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET transistor having an on-resistance of 30mΩ or lower.

Suspend LDO

If the LTC3576/LTC3576-1 are configured for USB suspend mode, the bidirectional switching regulator is disabled and the suspend LDO provides power to the V_{OUT} pin (presuming there is power available to V_{BUS}). This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the switching converter is disabled (suspended). The suspend LDO sends a scaled copy of the V_{BUS} current to the CLPROG pin, which will servo to approximately 100mV in this mode. To remain compliant with the USB specification, the input to the LDO is current limited so that it will not exceed the low power or high power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diode(s).

3.3V Always-On LDO Supply

The LTC3576/LTC3576-1 include a low quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller, standby microcontroller or real time clock. Designed to deliver up to 20mA, the always-on LDO requires at least a 1µF low impedance ceramic bypass capacitor for compensation. The LDO is powered from V_{OUT}, and therefore will enter dropout at loads less than 20mA as V_{OUT} falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to V_{OUT}.

Battery Charger

The LTC3576/LTC3576-1 include a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out-of-temperature charge pausing.

Battery Preconditioning

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{\text{CHRG}}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.85V, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1030/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current.

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Likewise, the USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the voltage on the battery reaches the pre-programmed float voltage, the battery charger will regulate the battery voltage and the charge current will decrease naturally. Once the battery charger detects that the battery has reached the float voltage, the four hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below the recharge threshold which is typically 100mV less than the charger's float voltage. In the event that the safety timer is running when the battery voltage falls below the recharge threshold, it will reset back to zero. To prevent brief excursions below the recharge threshold from resetting the safety timer, the battery voltage must be below the recharge threshold for more than 1ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced), or if the battery charger is cycled on and off by the I^2C port.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1030th of the battery charge current is sent to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1030 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equation:

$$I_{CHG} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input power available and prioritization with the system load drawn from V_{OUT}.

The Battery Charger Flow Chart illustrates the battery charger's algorithm.

Charge Status Indication

The $\overline{\text{CHRG}}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{\text{CHRG}}$ which include charging, not charging, unresponsive battery and battery temperature out of range.

The signal at the $\overline{\text{CHRG}}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{\text{CHRG}}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{\text{CHRG}}$ pin easily recognized by both humans and microprocessors, the pin is either low for charging, high for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults, unresponsive battery and battery temperature out of range.

When charging begins, $\overline{\text{CHRG}}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the BAT pin reaches the float voltage and the charge current has dropped to one-tenth of the programmed value, the $\overline{\text{CHRG}}$ pin is released (Hi-Z). If a fault occurs, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking".

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Battery Charger Flow Chart