



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



FDS5692Z

N-Channel UltraFET Trench® MOSFET

50V, 5.8A, 24mΩ

General Description

This N-Channel UltraFET device has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

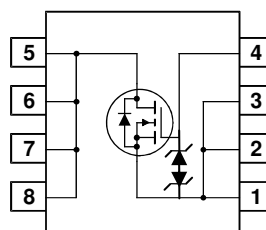
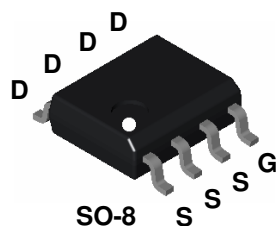
Applications

- DC/DC converter



Features

- Max $r_{DS(on)}$ = 24mΩ at $V_{GS} = 10V$, $I_D = 5.8A$
- Max $r_{DS(on)}$ = 33mΩ at $V_{GS} = 4.5V$, $I_D = 5.6A$
- ESD protection diode (note 3)
- Low Qgd
- Fast switching speed



MOSFET Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	50	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	5.8	A
	– Pulsed	40	
E_{AS}	Single Pulse Avalanche Energy	72	mJ
P_D	UltraFET Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDS5692Z	FDS5692Z	SO-8	13"	12mm	2500units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Drain-Source Avalanche Ratings

E_{AS}	Drain-Source Avalanche Energy (Single Pulse)	$V_{DD} = 50\text{ V}$, $I_D = 12\text{ A}$, $L = 1\text{ mH}$			72	mJ
I_{AS}	Drain-Source Avalanche Current			12		A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		48		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics (Note 4)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.8\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 5.6\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 5.8\text{ A}$, $T_J = 125^\circ\text{C}$		20 26 32	24 33 41	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		1025		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			50		pF
R_G	Gate Resistance	$f = 1.0\text{ MHz}$		0.79		Ω
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 10\text{ V}$	$V_{DS} = 25\text{ V}$, $I_D = 5.8\text{ A}$		18	25	nC
$Q_{g(TOT)}$	Total Gate Charge, $V_{GS} = 5\text{ V}$			10	14	nC
Q_{gs}	Gate-Source Gate Charge			2.8		nC
Q_{gd}	Gate-Drain Gate Charge			3.0		nC

Switching Characteristics (Note 4)

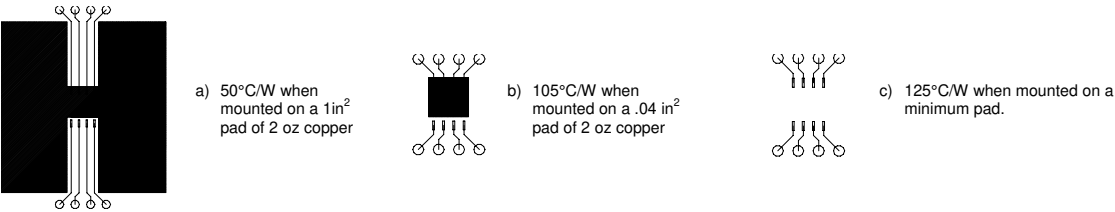
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 25\text{ V}$, $I_D = 5.8\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		9	18	ns
t_r	Rise Time			5	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns
t_f	Fall Time			6	12	ns

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics						
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V,	I _S = 5.8 A	0.79	1.25	V
			I _S = 2.9 A	0.75	1.0	V
t _{rr}	Reverse Recovery Time	I _F = 6A, dI _F /dt = 100A/μs		24		ns
Q _{rr}	Reverse Recovery Charge			16		nC

Notes:
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



- Scale 1 : 1 on letter size paper
2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

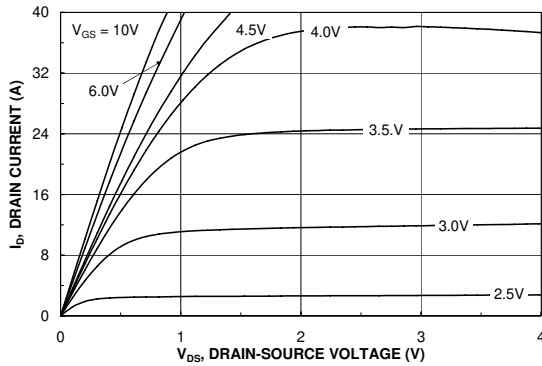


Figure 1. On-Region Characteristics.

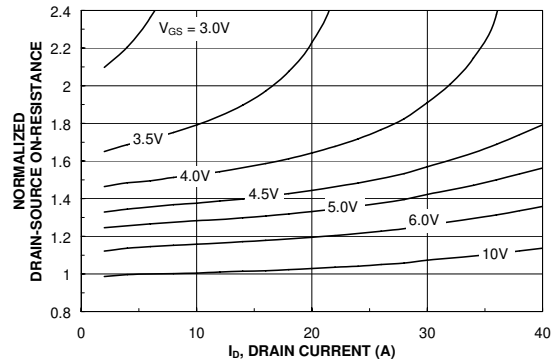


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

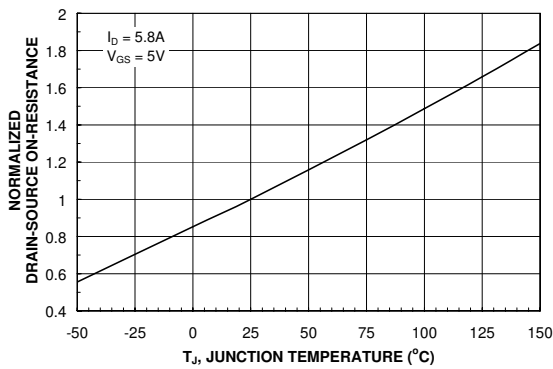


Figure 3. On-Resistance Variation with Temperature.

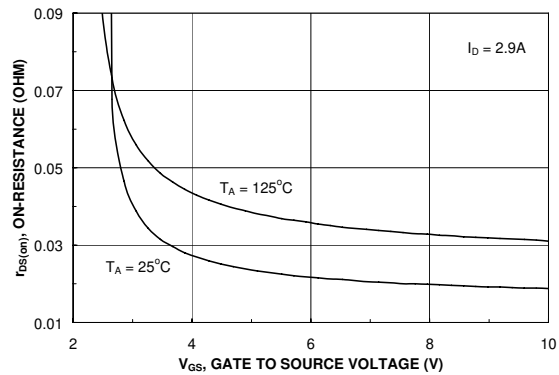


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

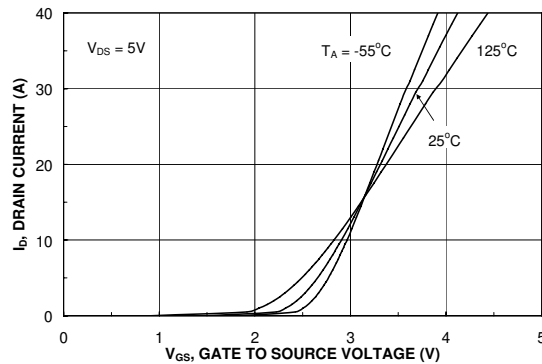


Figure 5. Transfer Characteristics.

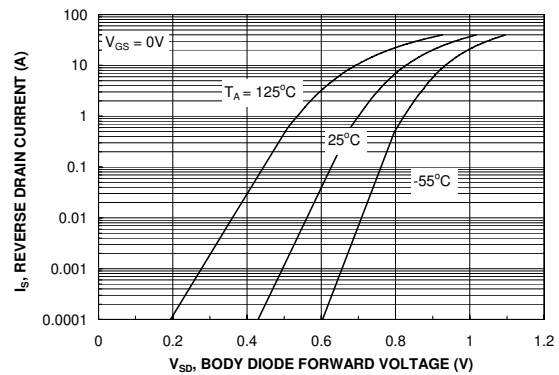


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

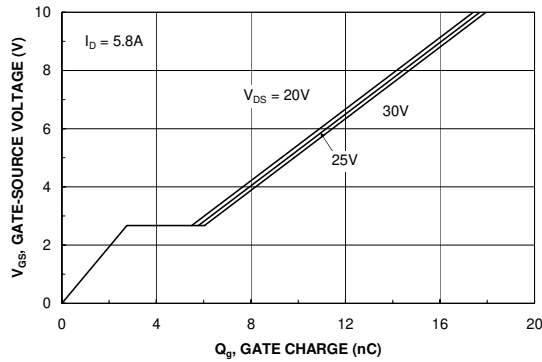


Figure 7. Gate Charge Characteristics.

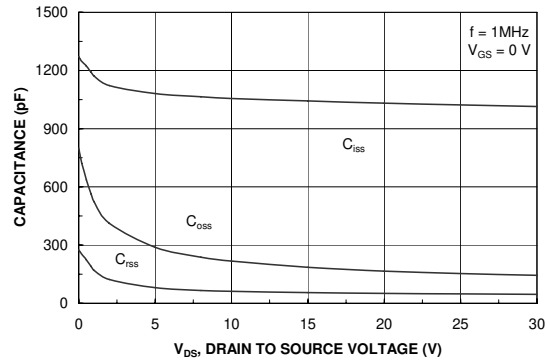


Figure 8. Capacitance Characteristics.

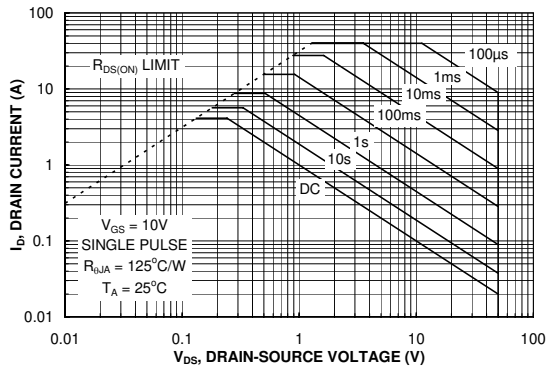


Figure 9. Maximum Safe Operating Area.

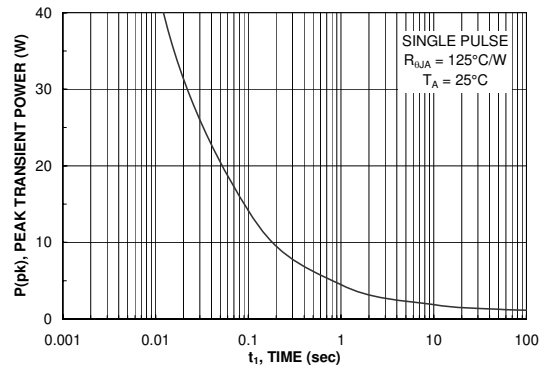


Figure 10. Single Pulse Maximum UltraFET Dissipation.

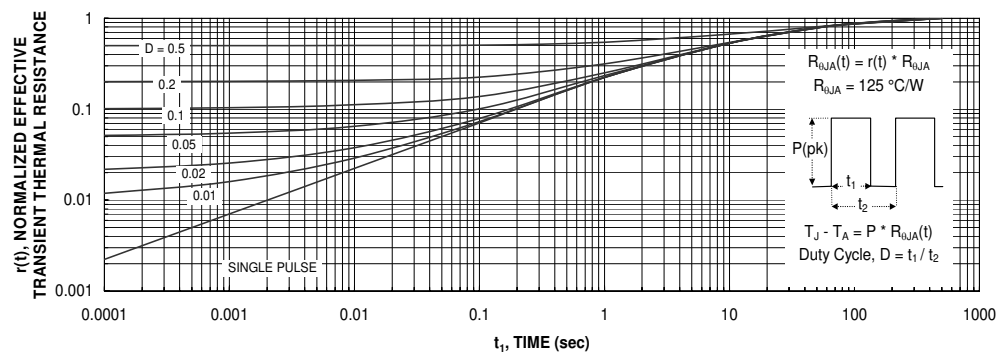


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-6
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SuperSOT™-8
Bottomless™	FPS™	MICROCOUPLER™	QFET®	SyncFET™
Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOME™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I²C™	MSXPro™	RapidConnect™	UHC™
E²CMOS™	i-Lo™	OCX™	µSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.