N24C64

EEPROM Serial 64-Kb I^{2}C

Description

The N24C64 is a EEPROM Serial 64−Kb I^{2}C device, organized internally as 256 pages of 32 bytes each. This device supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I^{2}C protocol.

Data is written by providing a starting address, then loading 1 to 32 contiguous bytes into a Page Write Buffer, and then writing all data to non−volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight N24C64 devices on the same bus.

Features

- Supports Standard, Fast and Fast−Plus I^{2}C Protocol
- 1.7 V / 1.6 V to 5.5 V Supply Voltage Range
- 32−Byte Page Write Buffer
- Fast Write Time (4 ms max)
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^{2}C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Automotive Grade 1 Temperature Range
- US 8−lead and 4−ball WLCSP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free, and RoHS Compliant
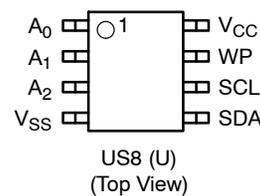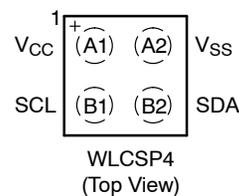
ON Semiconductor®

US8
U SUFFIX
CASE 493

WLCSP4
A4 SUFFIX
CASE 567NH

PIN CONFIGURATIONS

A$_0$		V$_{CC}$
A$_1$		WP
A$_2$		SCL
V$_{SS}$		SDA

US8 (U)
(Top View)

V$_{CC}$	(A1) (A2)	V$_{SS}$
SCL	(B1) (B2)	SDA

WLCSP4
(Top View)

MARKING DIAGRAMS

8

XX M■
●

1

+
T
YW
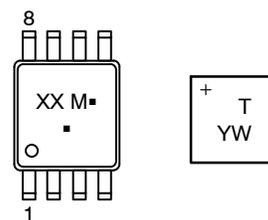
XX or T = Specific Device Code*
M   = Date Code
Y   = Year
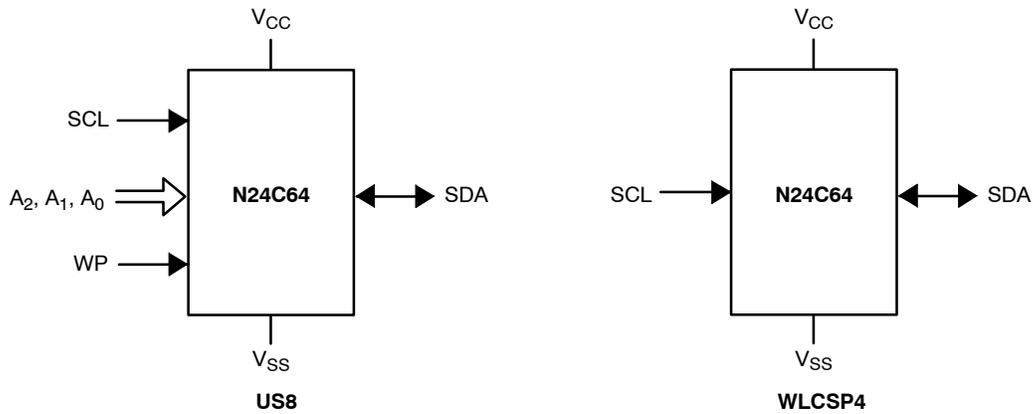W   = Work Week
■   = Pb−Free Package

(Note: Microdot may be in either location)

* See Ordering Information section for the Specific Device Marking Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

May, 2018 − Rev. 2

N24C64

US8

WLCSP4

PIN FUNCTION

Pin Name	Function
A_0, A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

Figure 1. Functional Symbols

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Max	Units
N_{END} (Note 2)	Endurance	1,000,000	Write Cycles (Note 3)
T_{DR} (Note 2)	Data Retention	100	Years

2. T_A = 25°C
3. A Write Cycle refers to writing a Byte or a Page.

Table 3. D.C. OPERATING CHARACTERISTICS
$(V_{CC}$ = 1.7 V / 1.6 V* to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 1 MHz		1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 1 MHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		2	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage	SCL, SDA	−0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage	SCL, SDA	V_{CC} x 0.7	V_{CC} + 0.5	V
V_{ILA}	Input Low Voltage	A2, A1, A0 and WP	−0.5	V_{CC} x 0.3	V
V_{IHA}	Input High Voltage	A2, A1, A0 and WP	V_{CC} x 0.8	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	$V_{CC} <$ 2.5 V, I_{OL} = 1.0 mA		0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PIN IMPEDANCE CHARACTERISTICS
$(V_{CC}$ = 1.7 V / 1.6 V* to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V		8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	V_{IN} = 0 V		6	pF
R_{PD} (Note 5)	WP, A0, A1 or A2 On−Chip Pull−Down Resistor	$V_{IN} < V_{IHA}$	50		kΩ
I_{PD} (Note 5)	WP, A0, A1 or A2 On−Chip Pull−Down Current	$V_{IN} > V_{IHA}$		2	μA

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. For improved noise immunity (and to allow for floating input pins), the WP, A0, A1 & A2 inputs are pulled−down to GND by relatively strong on−chip resistors. When attempting to drive these inputs High, the external drivers must be able to supply sufficient current, until the input level at the pin exceeds V_{IHA}. Once the input level at the pin exceeds V_{IHA}, the resistive pull−down (R_{PD}) converts to a constant current pull−down (I_{PD}).

Table 5. A.C. CHARACTERISTICS

(V_{CC} = 1.7 V / 1.6 V* to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C unless otherwise noted.) (Note 6)

Symbol	Parameter	Standard		Fast		Fast−Plus		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	μs
t_{DH} (Note 7)	Data Out Hold Time	100		100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		4		4		4	ms
t_{PU} (Notes 7, 8)	Power-up to Ready Mode		0.35		0.35		0.35	ms

*$V_{CC(min)}$ = 1.6 V for Read operations, T_A = −20°C to +85°C
6. Test conditions according to "A.C. Test Conditions" table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC} for $V_{CC} \geq$ 2.2 V; 0.15 x V_{CC} to 0.85 x V_{CC} for V_{CC} < 2.2 V
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Load	Current Source: I_{OL} = 6 mA ($V_{CC} \geq$ 2.5 V); I_{OL} = 2 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power-On Reset (POR)

Each N24C64 incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the clock signal generated by the Master.

SDA: The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address inputs set the device address that must be matched by the corresponding Slave address bits. The Address inputs are hard-wired HIGH or LOW allowing for up to eight devices to be used (cascaded) on the same bus. When left floating, these inputs are pulled LOW internally.

WP: When pulled HIGH, the Write Protect input pin inhibits all write operations. When left floating, this pin is pulled LOW internally.

Functional Description

The N24C64 supports the Inter-Integrated Circuit (I^2C) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The N24C64 operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

I^2C Bus Protocol

The 2-wire I^2C bus consists of two lines, SCL and SDA, connected to the V_{CC} supply via pull-up resistors. The Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A '0' is transmitted by pulling a line LOW and a '1' by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8-bit Slave address. For the N24C64, the first four bits of the Slave address are set to 1010 (Ah); the next three bits, A_2, A_1 and A_0, must match the logic state of the similarly named input pins. The $R/\overline{W}$ bit tells the Slave whether the Master intends to read (1) or write (0) data (Figure 3). The device in WLCSP with 4 bumps responds only to address combination A2A1A0 = 000.

Acknowledge

During the 9th clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.
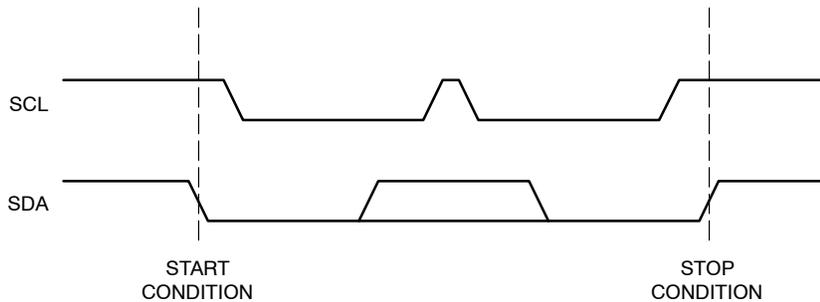

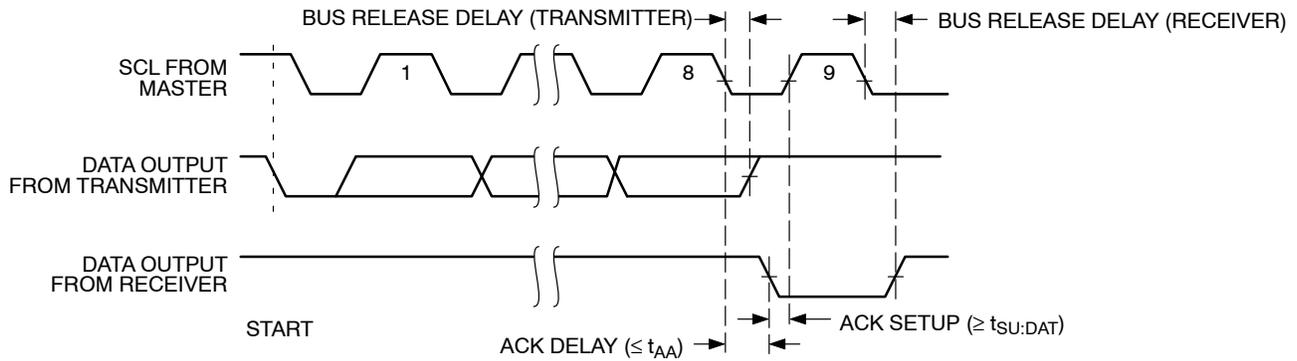**Figure 2. Start/Stop Timing**

Figure 3. Slave Address Bits
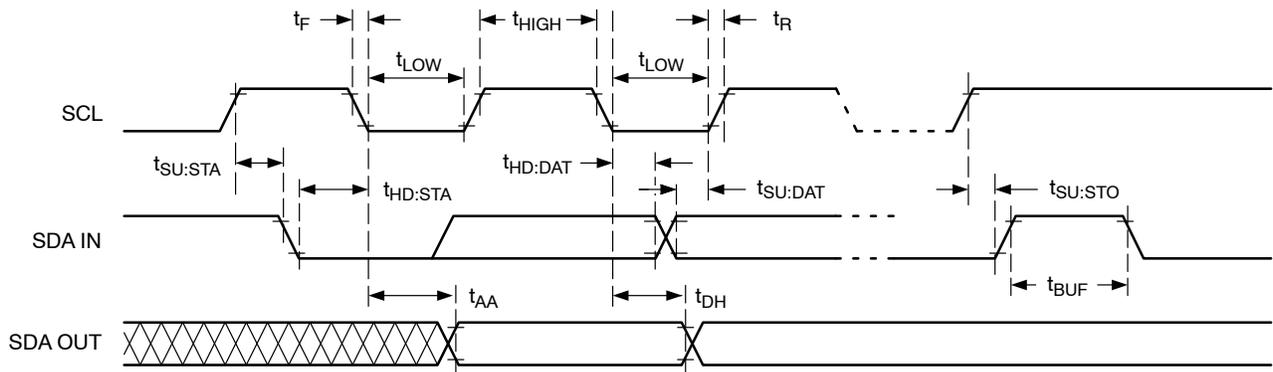
Figure 4. Acknowledge Timing

Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{\text{W}}$ bit set to '0'. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 6). The STOP starts the internal Write cycle, and while this operation is in progress (t_{WR}), the SDA output is tri-stated and the Slave does not acknowledge the Master (Figure 7).

Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 8). Up to 32 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle (t_{WR}).

Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow-up with a new Read or Write request, rather than wait for the maximum specified Write time (t_{WR}) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the Write operation. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the 1st data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the Slave will not acknowledge the data byte and the Write request will be rejected.

Delivery State

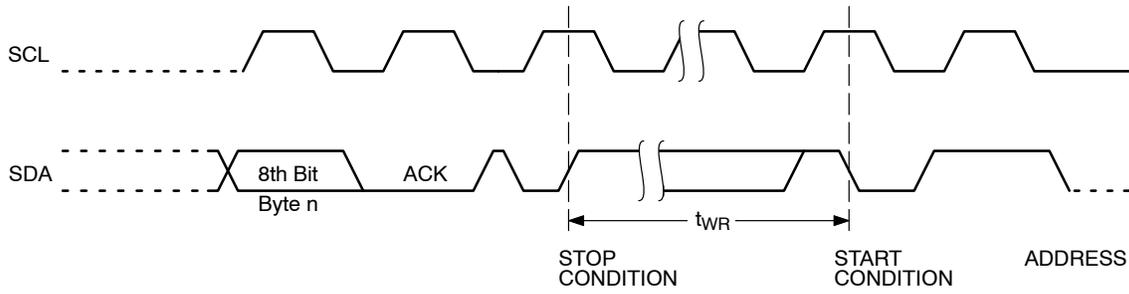The N24C64 is shipped erased, i.e., all bytes are FFh.

N24C64

*$a_{15} - a_{13}$ are don't care bits.
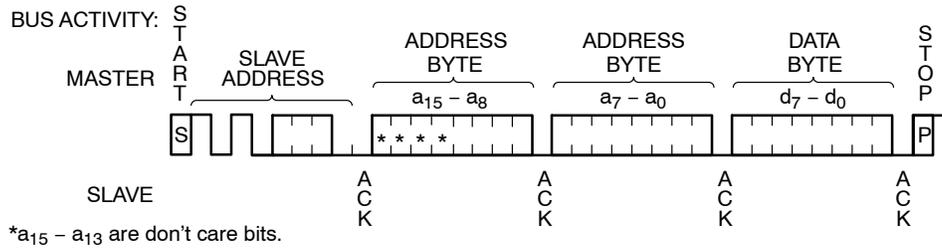
Figure 6. Byte Write Sequence

Figure 7. Write Cycle Timing
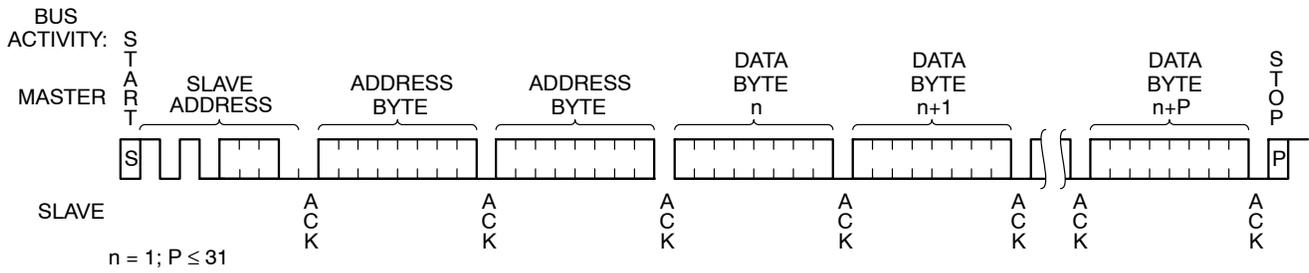

n = 1; P ≤ 31

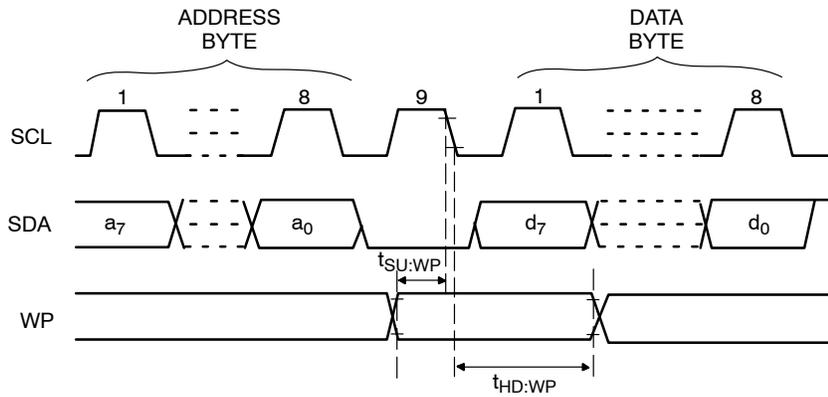**Figure 8. Page Write Sequence**

Figure 9. WP Timing

READ OPERATIONS

Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 10). The Slave then returns to Standby mode.

Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte

Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 11).

Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 12). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.
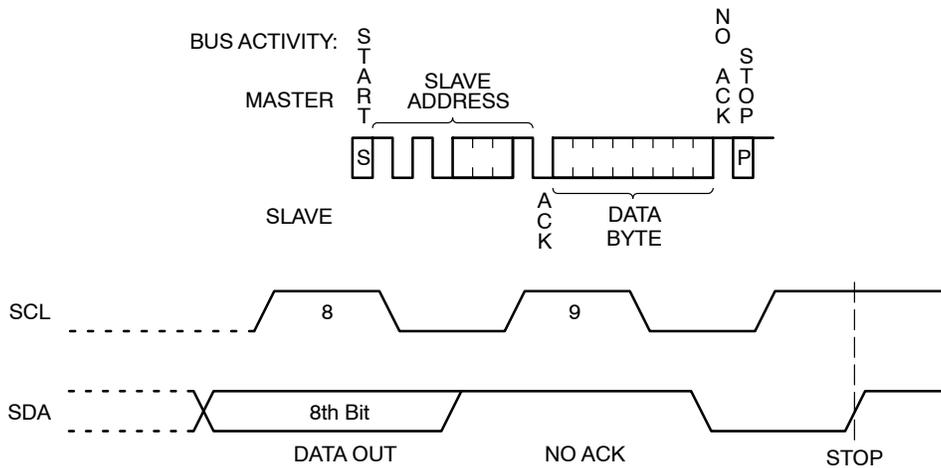
Figure 10. Immediate Read Sequence and Timing
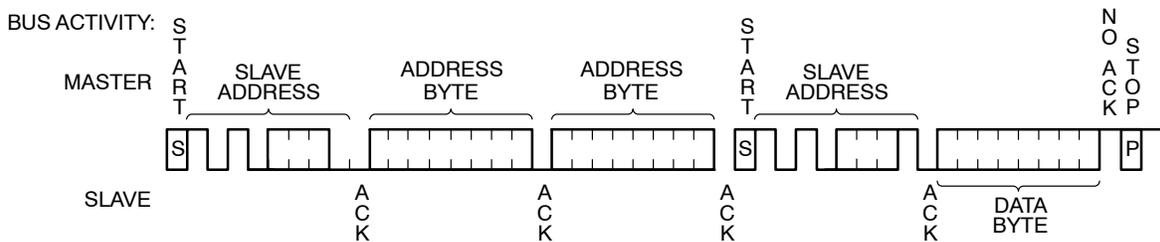
Figure 11. Selective Read Sequence
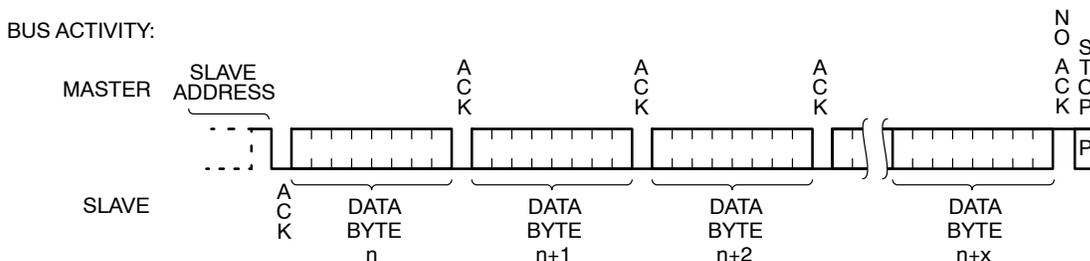
Figure 12. Sequential Read Sequence

N24C64

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Shipping†
N24C64UDTG	AT	U = US–8	D = Industrial (−40°C to +85°C)	T = Tape & Reel, 3,000 Units / Reel
N24C64UVTG	A6	U = US–8	V = Automotive Grade 1 (−40°C to +125°C)	T = Tape & Reel, 3,000 Units / Reel
N24C64A4DXTG	T	A = WLCSP	D = Industrial (−40°C to +85°C)	T = Tape & Reel, 5,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
9. All packages are RoHS-compliant (Lead-free, Halogen-free).
10. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

ON Semiconductor is licensed by the Philips Corporation to carry the I2C bus protocol.

US8
CASE 493
ISSUE D

SCALE 4 :1

DATE 15 JUL 2015
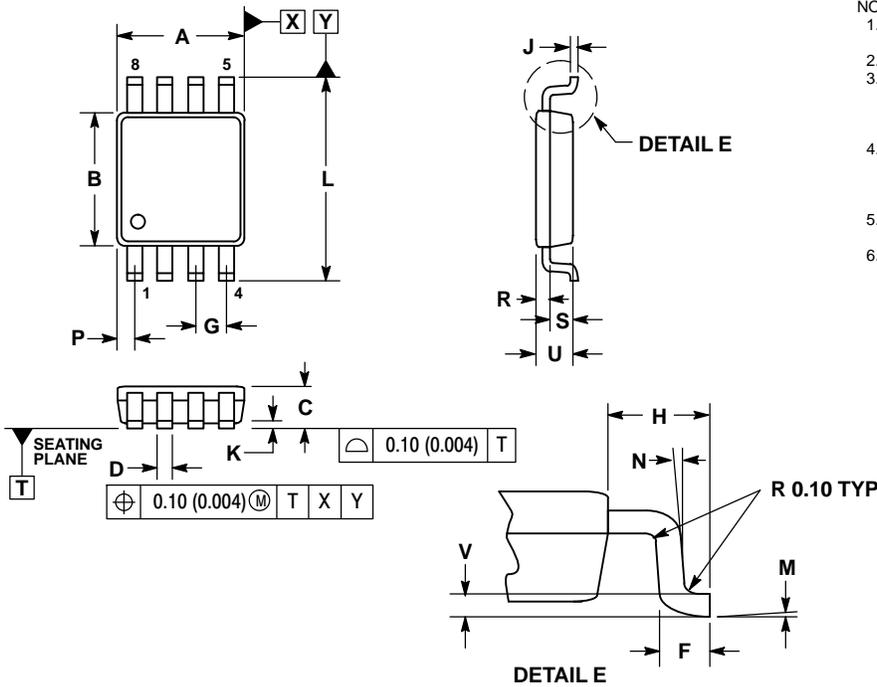
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0.0203MM (0.003–0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508MM (0.0002").

DETAIL E

$\square$ 0.10 (0.004) T

$\oplus$ 0.10 (0.004) Ⓜ T X Y

SEATING PLANE

R 0.10 TYP

DETAIL E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0 °	6 °	0 °	6 °
N	0 °	10 °	0 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

8X
0.30

8X
0.68

3.40

1

0.50
PITCH
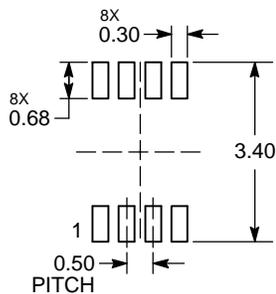
DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

8

XX M■

1
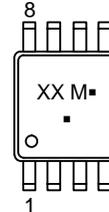
XX = Specific Device Code
M = Date Code
■ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ BY R. FORNESS	19 MAR 2001
A	CHANGED DIM "P" TO 0.23 MM MIN, 0.34 MM MAX AND 0.010 IN MIN, 0.013 IN MAX. REQ BY J. MILLER	25 JUN 2003
B	ADDED SOLDERING FOOTPRINT. REQ. BY D. TRUHITTE.	13 APR 2006
C	MODIFIED SOLDERING FOOTPRINT. REQ. BY B. BECKER.	23 MAR 2015
D	MODIFIED DIMENSION A MIN VALUE AND DIMENSION C MAX VALUE FOR MM. REQ. BY R. AVILA.	15 JUL 2015

WLCSP4 0.77x0.77, 0.35P
CASE 567NH
ISSUE A

DATE 23 AUG 2016

SCALE 4:1

PIN A1
REFERENCE

TOP VIEW

DETAIL A

0.05 C

NOTE 4   A1   **SIDE VIEW**

NOTE 3

C   SEATING
PLANE

BACKSIDE
COATING
NOTE 6

A3
A2
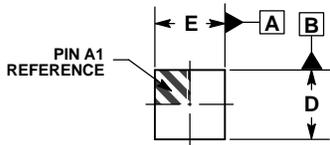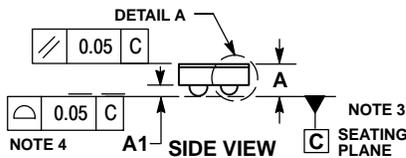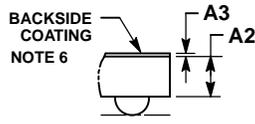
DETAIL A
OPTIONAL CONSTRUCTION

4X ⌀ **b**

0.05 C A B
0.03 C

NOTE 5
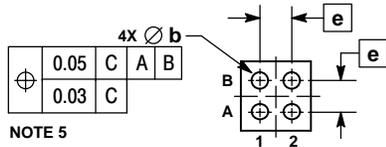
BOTTOM VIEW

RECOMMENDED
SOLDERING FOOTPRINT*

A1

PACKAGE
OUTLINE

0.35
PITCH

4X
⌀ 0.18

0.35
PITCH
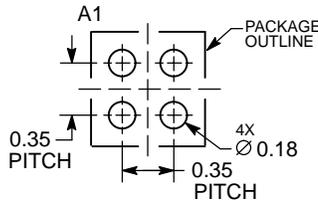
DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING IS OPTIONAL.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	–––	–––	0.38
A1	0.08	0.10	0.12
A2	0.23 REF		
A3	0.025 REF		
b	0.16	0.18	0.20
D	0.75	0.77	0.79
E	0.75	0.77	0.79
e	0.35 BSC		

GENERIC
MARKING DIAGRAM*

X
Y W

X = Specific Device Code
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY A. SARWARI.	27 JAN 2016
A	CORRECTED DETAIL A, ADDED NOMINAL VALUES, UPDATED TOLERANCES. REQ. BY V. CRACIUNOIU.	23 AUG 2016

PUBLICATION ORDERING INFORMATION

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