

Parallel NOR Flash Automotive Memory

**MT28FW512ABA1xPC-0AAT, MT28FW512ABA1xJS-0AAT,
MT28FW512ABA1xPN-0AAT**

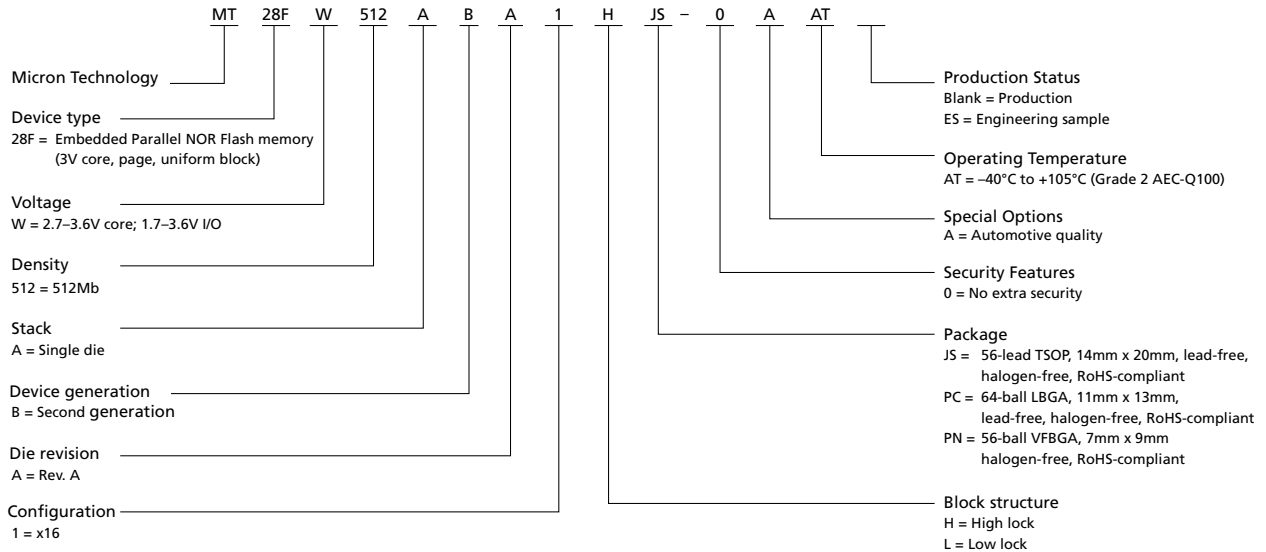
Features

- Single-level cell (SLC) process technology
- Supply voltage
 - $V_{CC} = 2.7\text{--}3.6\text{V}$ (program, erase, read)
 - $V_{CCQ} = 1.65 - V_{CC}$ (I/O buffers)
- Asynchronous random/page read
 - Page size: 16 words
 - Page access: 20ns ($V_{CC} = V_{CCQ} = 2.7\text{--}3.6\text{V}$)
 - Random access: 105ns ($V_{CC} = V_{CCQ} = 2.7\text{--}3.6\text{V}$)
 - Random access: 110ns ($V_{CCQ} = 1.65\text{--}V_{CC}$)
- Buffer program (512-word program buffer)
 - 2.0 MB/s (TYP) when using full buffer program
 - 2.5 MB/s (TYP) when using accelerated buffer program (V_{HH})
- Word program: 25us per word (TYP)
- Block erase (128KB): 0.2s (TYP)
- Memory organization
 - Uniform blocks: 128KB or 64KW each
 - x16 data bus
- Program/erase suspend and resume capability
 - Read from another block during a PROGRAM SUSPEND operation
 - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, and write to buffer capability
- BLANK CHECK operation to verify an erased block
- CYCLIC REDUNDANCY CHECK (CRC) operation to verify a program pattern
- $V_{PP}/WP\#$ protection
 - Protects first or last block regardless of block protection settings
- Software protection
 - Volatile protection
 - Nonvolatile protection
 - Password protection
- Extended memory block
 - 512-word block for permanent, secure identification
 - Programmed or locked at the factory or by the customer
- JESD47-compliant
 - 100,000 (minimum) ERASE cycles per block
 - Data retention: 20 years (TYP)
- Package
 - 56-pin TSOP, 14mm x 20mm (JS)
 - 64-ball LBGGA, 13mm x 11mm (PC)
 - 56-ball VFBGA, 7mm x 9mm (PN)
- RoHS-compliant, halogen-free packaging
- Automotive operating temperature
 - Ambient: -40°C to 105°C

Part Numbering Information

For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart





Contents

General Description	7
Automatic Power Savings Feature	7
Signal Assignments	9
Signal Descriptions	12
Memory Organization	14
Memory Configuration	14
Memory Map	14
Bus Operations	15
Read	15
Write	15
Standby	15
Output Disable	16
Reset	16
Registers	17
Data Polling Register	17
Read Status Register	22
Clear Status Register	23
Lock Register	24
Standard Command Definitions – Address-Data Cycles	26
READ and AUTO SELECT Operations	28
READ/RESET Command	28
READ CFI Command	28
AUTO SELECT Command	28
Read Electronic Signature	29
Cyclic Redundancy Check Operation	30
CYCLIC REDUNDANCY CHECK Command	30
Cyclic Redundancy Check Operation Command Sequence	30
Bypass Operations	33
UNLOCK BYPASS Command	33
UNLOCK BYPASS RESET Command	33
Program Operations	34
PROGRAM Command	34
UNLOCK BYPASS PROGRAM Command	34
WRITE TO BUFFER PROGRAM Command	34
UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command	37
WRITE TO BUFFER PROGRAM CONFIRM Command	37
BUFFERED PROGRAM ABORT AND RESET Command	37
PROGRAM SUSPEND Command	37
PROGRAM RESUME Command	38
ACCELERATED BUFFERED PROGRAM Operations	38
Erase Operations	39
CHIP ERASE Command	39
UNLOCK BYPASS CHIP ERASE Command	39
BLOCK ERASE Command	39
UNLOCK BYPASS BLOCK ERASE Command	40
ERASE SUSPEND Command	40
ERASE RESUME Command	41
ACCELERATED CHIP ERASE Operations	41
BLANK CHECK Operation	41
Device Protection	43



Hardware Protection	43
Software Protection	43
Volatile Protection Mode	44
Nonvolatile Protection Mode	44
Password Protection Mode	44
Block Protection Command Definitions – Address-Data Cycles	47
Protection Operations	50
LOCK REGISTER Commands	50
PASSWORD PROTECTION Commands	50
NONVOLATILE PROTECTION Commands	50
NONVOLATILE PROTECTION BIT LOCK BIT Commands	51
VOLATILE PROTECTION Commands	52
EXTENDED MEMORY BLOCK Commands	52
EXIT PROTECTION Command	53
Common Flash Interface	54
Power-Up and Reset Characteristics	59
Absolute Ratings and Operating Conditions	61
DC Characteristics	63
Read AC Characteristics	65
Write AC Characteristics	67
Data Polling/Toggle AC Characteristics	72
Program/Erase Characteristics	74
Package Dimensions	75
Revision History	78
Rev. F – 11/16	78
Rev. E – 9/15	78
Rev. D – 01/15	78
Rev. C – 12/14	78
Rev. B – 07/14	78
Rev. A – 05/14	78

List of Figures

Figure 1: Part Number Chart	2
Figure 2: Logic Diagram	8
Figure 3: 56-Pin TSOP (Top View)	9
Figure 4: 64-Ball LBGA (Top View – Balls Down)	10
Figure 5: 56-Ball VFBGA (Top View – Balls Down)	11
Figure 6: Data Polling Flowchart	19
Figure 7: Toggle Bit Flowchart	20
Figure 8: Data Polling/Toggle Bit Flowchart	21
Figure 9: Lock Register Program Flowchart	25
Figure 10: Boundary Condition of Program Buffer Size	35
Figure 11: WRITE TO BUFFER PROGRAM Flowchart	36
Figure 12: Software Protection Scheme	45
Figure 13: Set/Clear Nonvolatile Protection Bit Algorithm Flowchart	51
Figure 14: Power-Up Timing	59
Figure 15: Reset AC Timing – No PROGRAM/ERASE Operation in Progress	60
Figure 16: Reset AC Timing During PROGRAM/ERASE Operation	60
Figure 17: AC Measurement Load Circuit	62
Figure 18: AC Measurement I/O Waveform	62
Figure 19: Random Read AC Timing	66
Figure 20: Page Read AC Timing	66
Figure 21: WE#-Controlled Program AC Timing	68
Figure 22: CE#-Controlled Program AC Timing	70
Figure 23: Chip/Block Erase AC Timing	71
Figure 24: Accelerated Program AC Timing	71
Figure 25: Data Polling AC Timing	72
Figure 26: Toggle/Alternative Toggle Bit Polling AC Timing	73
Figure 27: 56-Pin TSOP – 14mm x 20mm (Package Code: JS)	75
Figure 28: 64-Ball LBGA – 11mm x 13mm (Package Code: PC)	76
Figure 29: 56-Ball VFBGA 7mm x 9mm (Package Code: PN)	77



List of Tables

Table 1: Signal Descriptions	12
Table 2: Blocks[511:0]	14
Table 3: Bus Operations	15
Table 4: Data Polling Register Bit Definitions	17
Table 5: Operations and Corresponding Bit Settings	18
Table 6: Status Register Definitions	22
Table 7: Lock Register Bit Definitions	24
Table 8: Standard Command Definitions – Address-Data Cycles	26
Table 9: Block Protection	29
Table 10: Read Electronic Signature – 512Mb	29
Table 11: Command Sequence – Range of Blocks	30
Table 12: Command Sequence – Entire Chip	32
Table 13: ACCELERATED PROGRAM Requirements and Recommendations	38
Table 14: ACCELERATED CHIP ERASE Requirements and Recommendations	41
Table 15: V _{pp} /WP# Functions	43
Table 16: Block Protection Status	46
Table 17: Block Protection Command Definitions – Address-Data Cycles	47
Table 18: Extended Memory Block Address and Data	52
Table 19: Query Structure Overview	54
Table 20: CFI Query Identification String	54
Table 21: CFI Query System Interface Information	55
Table 22: Device Geometry Definition	55
Table 23: Primary Algorithm-Specific Extended Query Table	56
Table 24: Power-Up Specifications	59
Table 25: Reset AC Specifications	60
Table 26: Absolute Maximum/Minimum Ratings	61
Table 27: Operating Conditions	61
Table 28: Input/Output Capacitance	62
Table 29: DC Current Characteristics	63
Table 30: DC Voltage Characteristics	64
Table 31: Read AC Characteristics – V _{CC} = V _{CCQ} = 2.7–3.6V	65
Table 32: Read AC Characteristics – V _{CCQ} = 1.65V–V _{CC}	65
Table 33: WE#-Controlled Write AC Characteristics	67
Table 34: CE#-Controlled Write AC Characteristics	69
Table 35: Data Polling/Toggle AC Characteristics	72
Table 36: Program/Erase Characteristics	74

General Description

The device is an asynchronous, uniform block, parallel NOR Flash memory device. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The device supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 512 words via one command sequence. A 512-word extended memory block overlaps addresses with array block 0. Users can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Automatic Power Savings Feature

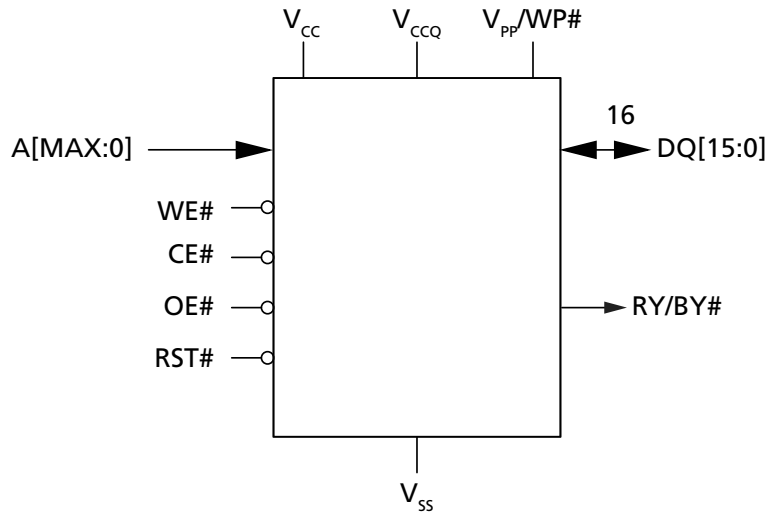
The automatic power savings feature provides low power operation during reads.

After data is read from the memory array and the address lines are quiescent, the automatic power savings feature reduces device current to a low value of I_{CCAPS} .

During automatic power savings mode, average current is measured over 5ms time interval 5 μ s after the following events happen:

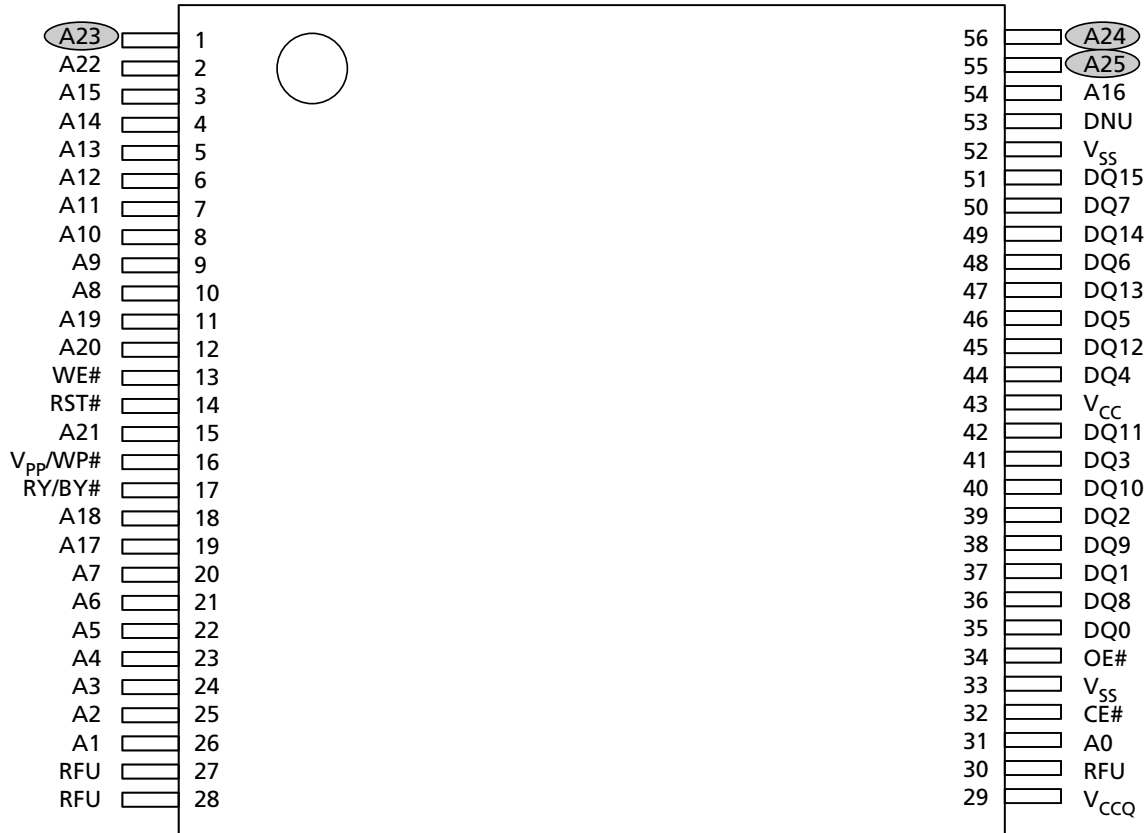
- No internal read, program or erase activity occurring
- RST# is deasserted and CE# is asserted
- All other signals are quiescent and at V_{SS} or V_{CCQ}

Figure 2: Logic Diagram



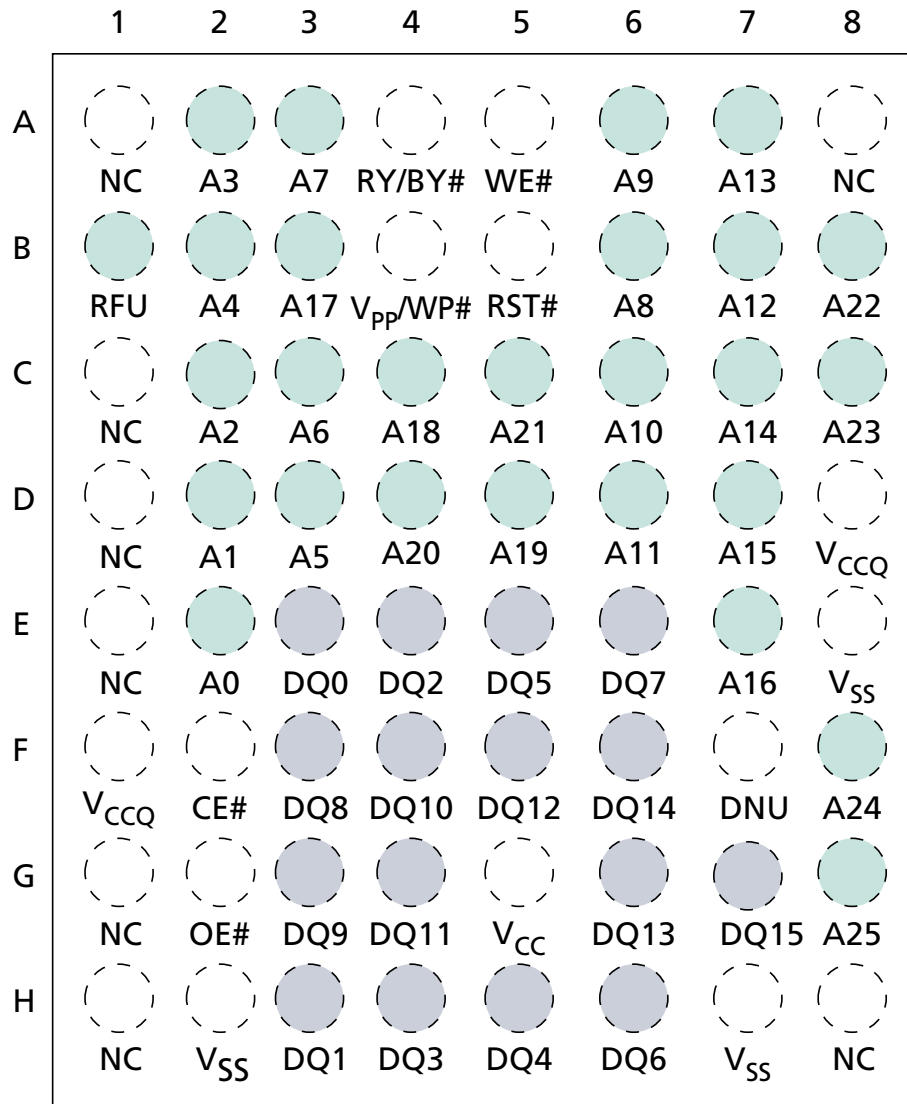
Signal Assignments

Figure 3: 56-Pin TSOP (Top View)



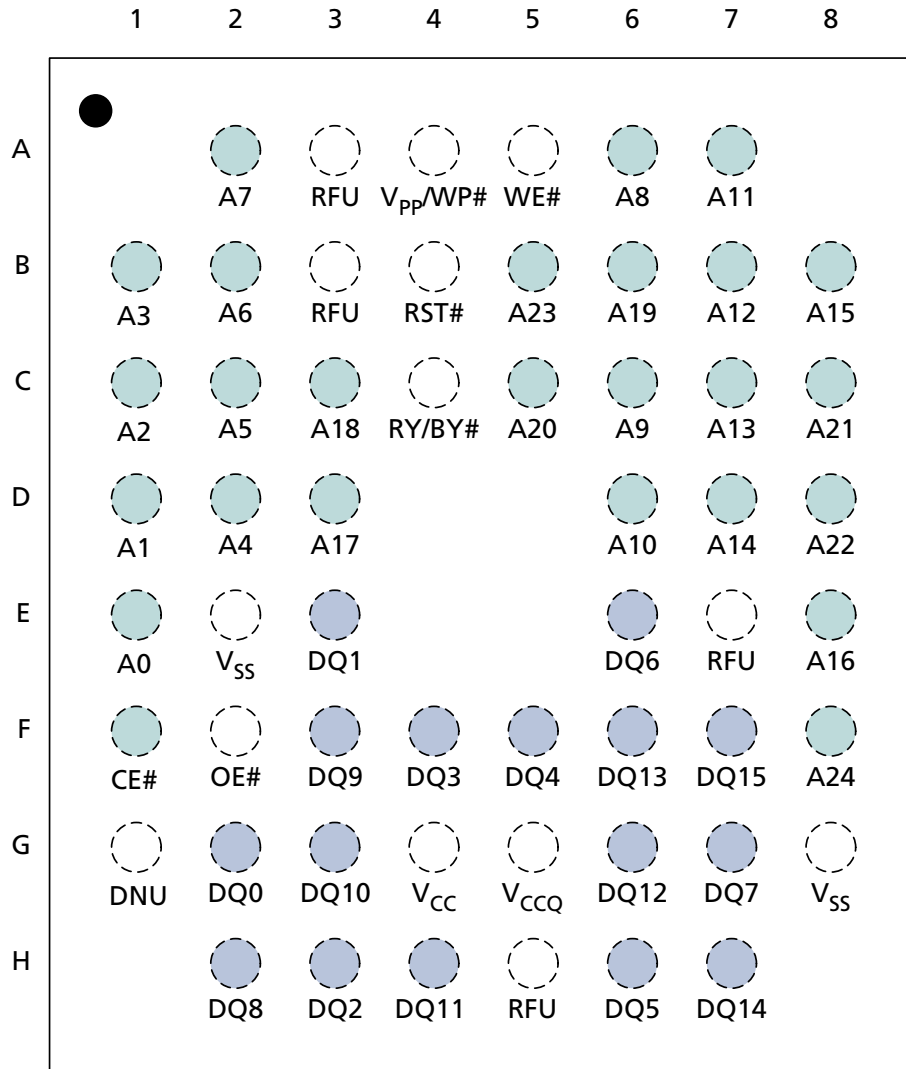
- Notes:
1. A23 is valid for 256Mb and above; otherwise, it is RFU.
 2. A24 is valid for 512Mb and above; otherwise, it is RFU.
 3. A25 is valid for 1Gb and above; otherwise, it is RFU.

Figure 4: 64-Ball LPGA (Top View – Balls Down)



- Notes:
1. A23 is valid for 256Mb and above; otherwise, it is RFU.
 2. A24 is valid for 512Mb and above; otherwise, it is RFU.
 3. A25 is valid for 1Gb and above; otherwise, it is RFU.

Figure 5: 56-Ball VFBGA (Top View – Balls Down)



- Notes: 1. A23 is valid for 256Mb and above; otherwise, it is RFU.
 2. A24 is valid for 512Mb and above; otherwise, it is RFU.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	Address: Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	Chip enable: Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are High-Z.
OE#	Input	Output enable: Active LOW input. OE# LOW enables the data output buffers during READ cycles. When OE# is HIGH, data outputs are High-Z.
WE#	Input	Write enable: Controls WRITE operations to the device. Address is latched on the falling edge of WE# and data is latched on the rising edge.
V _{pp} /WP#	Input	V_{pp}/Write Protect: Provides WRITE PROTECT function and V _{HH} function. These functions protect the lowest or highest block and enable the device to enter unlock bypass mode, respectively. (Refer to Hardware Protection and Bypass Operations for details.)
RST#	Input	Reset: Applies a hardware reset to the device control logic and places it in standby, which is achieved by holding RST# LOW for at least ^t PLPH. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^t PHEL or ^t PHWL, whichever occurs last).
DQ[15:0]	I/O	Data I/O: Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
RY/BY#	Output	Ready busy: Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V _{CCQ} . A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V _{OL} .
V _{CC}	Supply	Supply voltage: Provides the power supply for READ, PROGRAM, and ERASE operations. The device is disabled when V _{CC} ≤ V _{LKO} . If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1μF and 0.01μF capacitor should be connected between V _{CC} and V _{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations (see DC Characteristics).
V _{CCQ}	Supply	I/O supply voltage: Provides the power supply to the I/O pins and enables all outputs to be powered independently from V _{CC} . A 0.1μF and 0.01μF capacitor should be connected between V _{CCQ} and V _{SS} to decouple the current surges from the power supply.
V _{SS}	Supply	Ground: All V _{SS} pins must be connected to the system ground.
RFU	—	Reserved for future use: Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a DNU signal.



Table 1: Signal Descriptions (Continued)

Name	Type	Description
DNU	—	Do not use: Do not connect to any other signal, or power supply; must be left floating.
NC	—	No connect: No internal connection; can be driven or floated.



Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map

Table 2: Blocks[511:0]

Block	Address Range	
	Start	End
511	1FF 0000h	1FF FFFFh
⋮	⋮	⋮
255	0FF 0000h	0FF FFFFh
⋮	⋮	⋮
127	07F 0000h	07F FFFFh
⋮	⋮	⋮
63	03F 0000h	03F FFFFh
⋮	⋮	⋮
0	000 0000h	000 FFFFh

Note: 1. 512Mb device = Blocks 0–511.

Bus Operations

Table 3: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V _{pp} /WP#	A[MAX:0]	DQ[15:0]
READ	L	L	H	H	X	Address	Data output
WRITE	L	H	L	H	H ³	Command address	Data input ⁴
STANDBY	H	X	X	H	X	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z
RESET	X	X	X	L	X	X	High-Z

- Notes:
1. Typical glitches of less than 3ns on CE#, OE#, and WE# are ignored by the device and do not affect bus operations.
 2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
 3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
 4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, extended memory block, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 16 words and is addressed by address inputs A[3:0]. The extended memory blocks and CFI area support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. If CE# goes HIGH and returns LOW for a subsequent access, a random read access is performed and ^tACC or ^tCE is required. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation (See AC Characteristics for timing requirement details).

Standby

Driving CE# HIGH in read mode causes the device to enter standby and data I/Os to be High-Z (See DC Characteristics).

During PROGRAM or ERASE operations, the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes. The device cannot be placed into standby mode during a PROGRAM/ERASE operation.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

When RST# is HIGH, a time of t_{PHEL} is required before a READ operation can access the device, and a delay of t_{PHWL} is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored, the device defaults to read array mode, and the data polling register is reset.

If RST# is driven LOW during a PROGRAM/ERASE operation or any other operation that requires writing to the device, the operation will abort within t_{PLRH} , and memory contents at the aborted block or address are no longer valid.

Registers

The device features two methods for monitoring internal status during modify operations: data polling status and read status register. Users must not mix the two methods. Only one method at a time must be used to monitor internal operations.

Data Polling Register

The device automatically enters data polling status mode upon command issuance. The data polling status information uses the following to indicate information: DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7; DQ[15:8] are reserved and will output 00h.

Table 4: Data Polling Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program, erase, or blank check controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE/BLANK CHECK operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK or CRC operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM, BLANK CHECK, or CRC operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	

- Notes:
1. The data polling register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
 2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon ERASE operation's successful completion, DQ7 outputs 1. During a BUFFER PROGRAM operation, the data polling bit is valid only for the last word being programmed in the write buffer.

3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.
5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.
6. When DQ5 is set to 1, a READ/RESET (F0h) command must be issued before any subsequent command.

Table 5: Operations and Corresponding Bit Settings

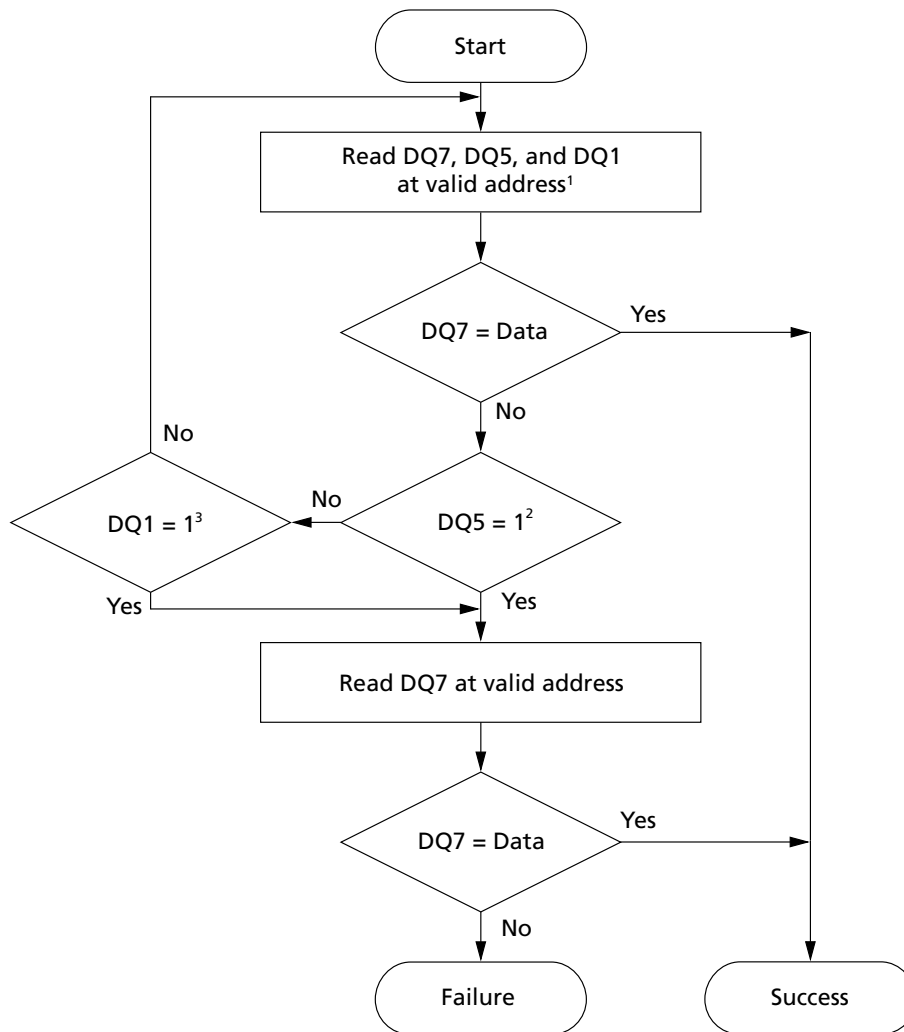
Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	2
CRC range of blocks	Any address	1	Toggle	0	–	–	0	0	
CRC chip	Any address	DQ7#	Toggle	0	–	–	0	0	4
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLANK CHECK	Blank-checking block	0	Toggle	0	1	Toggle	–	0	
	Non-blank-checking block	0	Toggle	0	1	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	–	High-Z	
	Non-erasing block	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	2
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	2
ERASE Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	
BLANK CHECK Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	
CRC range of blocks error	Any address	1	Toggle	1	–	–	–	High-Z	
CRC chip error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	4

- Notes:
1. Unspecified data bits should be ignored.
 2. DQ7# for buffer program is related to the last address location loaded.

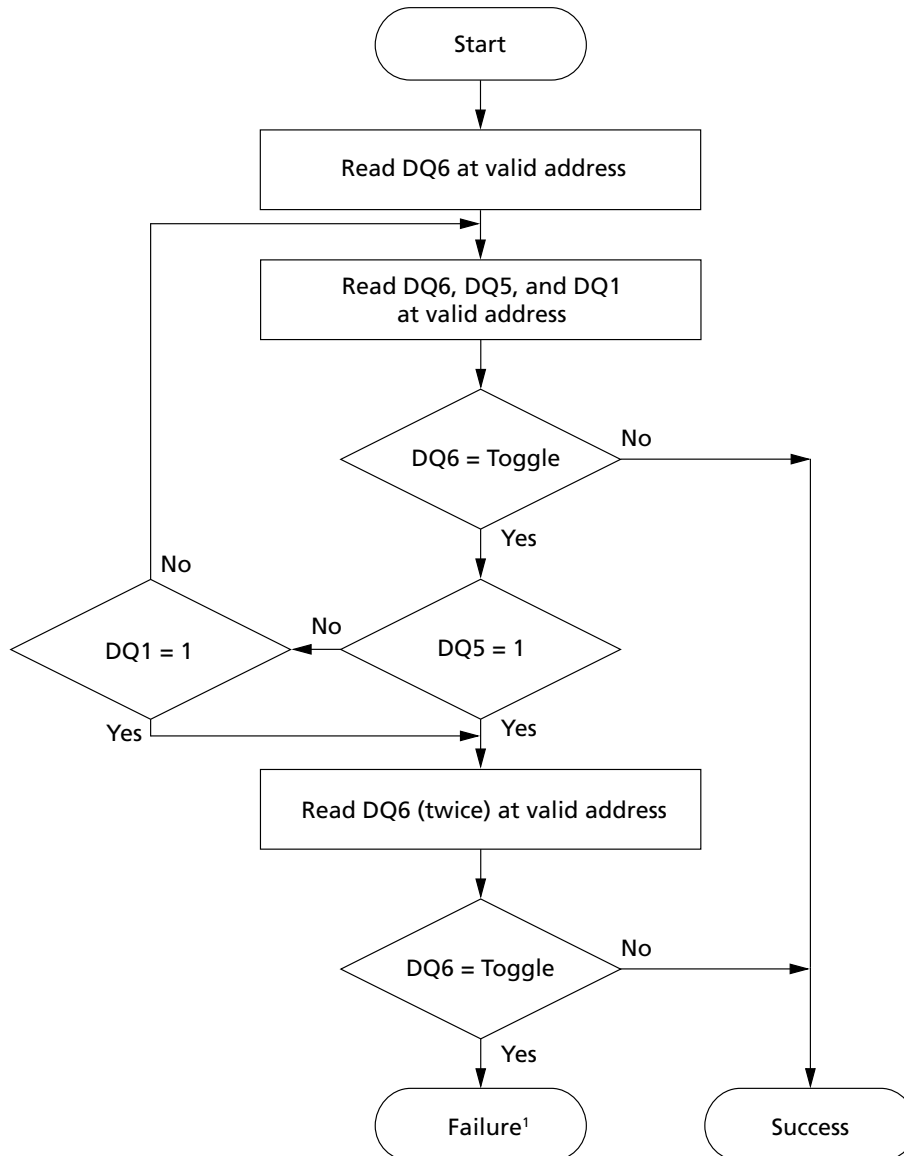
- DQ7# is the reverse DQ7 of the last word or byte loaded before CRC chip confirm command cycle.

Figure 6: Data Polling Flowchart



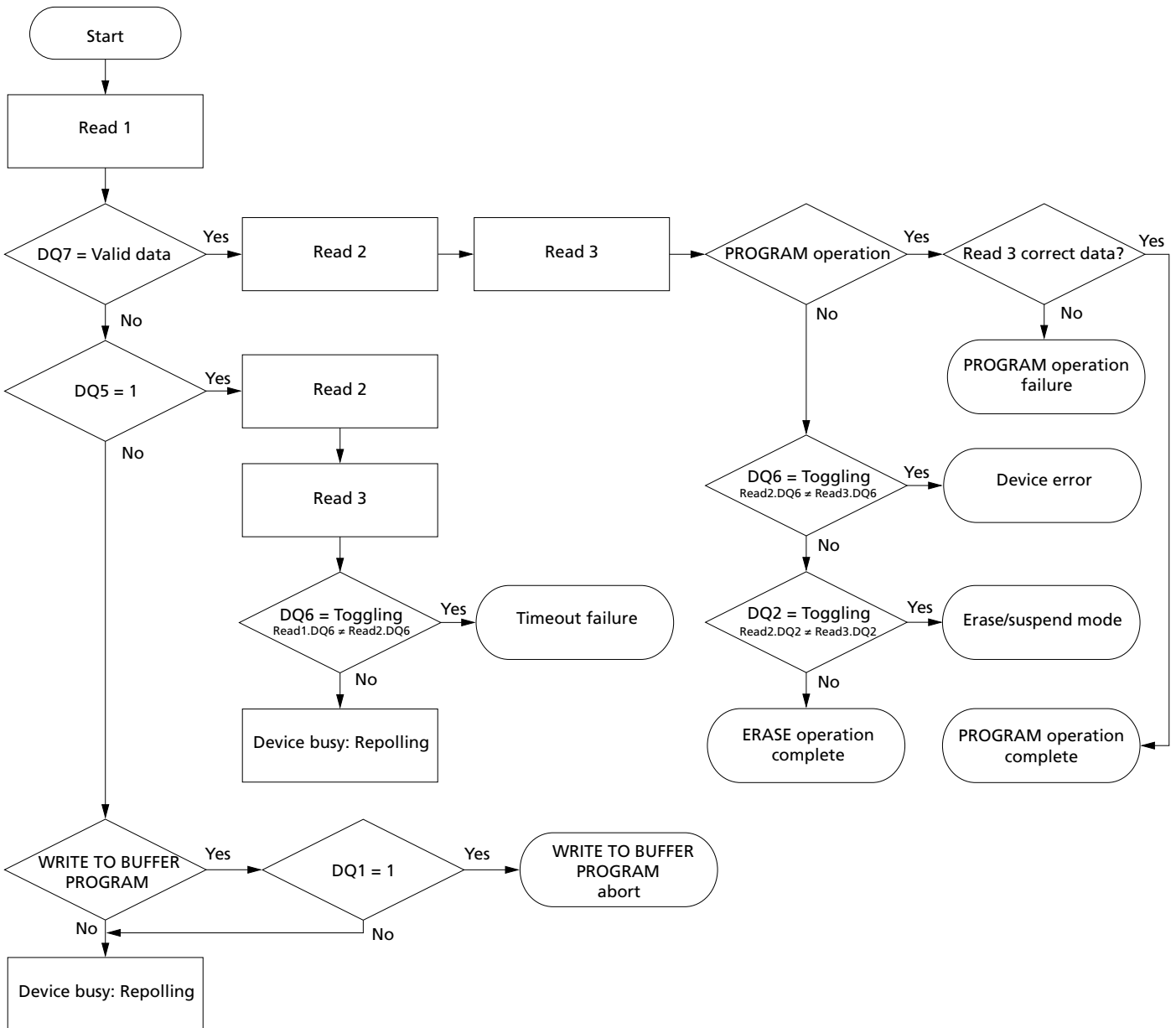
- Notes:
- Valid address is the last address being programmed or an address within the block being erased.
 - Failure results: DQ5 = 1 indicates an operation error. A READ/RESET (F0h) command must be issued before any subsequent command.
 - Failure results: DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation. A full three-cycle RESET (AAh/55h/F0h) command sequence must be used to reset the aborted device.

Figure 7: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 8: Data Polling/Toggle Bit Flowchart



Read Status Register

The device's status register displays PROGRAM, ERASE, and BLANK CHECK operations status. A device's status can be read after writing the READ STATUS REGISTER command (70h). When the READ STATUS REGISTER command is issued, the current status is captured by the register and the device is in read status register mode. The first read access in the status register mode exits the mode and returns to the output state when the READ STATUS REGISTER command was issued. No other command should be sent before reading the status register to exit the status register mode.

The status register bits are output on DQ[7:0], while DQ[15:8] outputs are 00h.

Table 6: Status Register Definitions

Bit	Name	Settings	Description
SR[15:8]	–	Reserved	Reserved for future use. Will always be set to 0.
SR7	Device program/erase/blank check status	0 = Busy 1 = Ready	Indicates erase, program, or blank check completion in the device. SR[6:1] are invalid; SR7 = 0.
SR6	Erase suspend status	0 = Erase in progress/complete 1 = Erase suspended	Indicates whether the device is erase suspended. After issuing an ERASE SUSPEND command, SR7 and SR6 are set to 1. SR6 remains set until the device receives an ERASE RESUME command.
SR5	Erase/blank check status	0 = Erase/blank check successful 1 = Erase/blank check error	Set to 1 if an attempted erase or blank check failed.
SR4	Program status	0 = Program success 1 = Program error	Indicates whether the program failed or the buffer program has aborted.
SR3	Writer buffer abort status	0 = Program not aborted 1 = Program aborted during buffer program	Indicates whether the buffer program has aborted.
SR2	Program suspend status	0 = Program in progress/complete 1 = Program suspended	Indicates whether the device is program suspended. After receiving a PROGRAM SUSPEND command, SR7 and SR2 are set to 1, and remain set at 1 until a RESUME command is received.
SR1	Device protect status	0 = Unlocked 1 = Aborted erase/program attempt on a locked block	Indicates whether program or erase was attempted on a locked block. If an ERASE or PROGRAM operation is attempted on a locked block, SR1 is set to 1 and the operation aborts.
SR0	–	Reserved	Reserved for future use. Will always be set to 0.

Clear Status Register

The status register content can be cleared by CLEAR STATUS REGISTER command (71h). The CLEAR STATUS REGISTER command clears the status register bits SR[6:1]. SR7 remains at 0, which indicates the device is busy.

However, for buffer program abort only, the CLEAR STATUS REGISTER command would change also SR7 to 1, which reverts the device to main array read mode. The status register can also be cleared by using RESET Command (F0h).

Lock Register

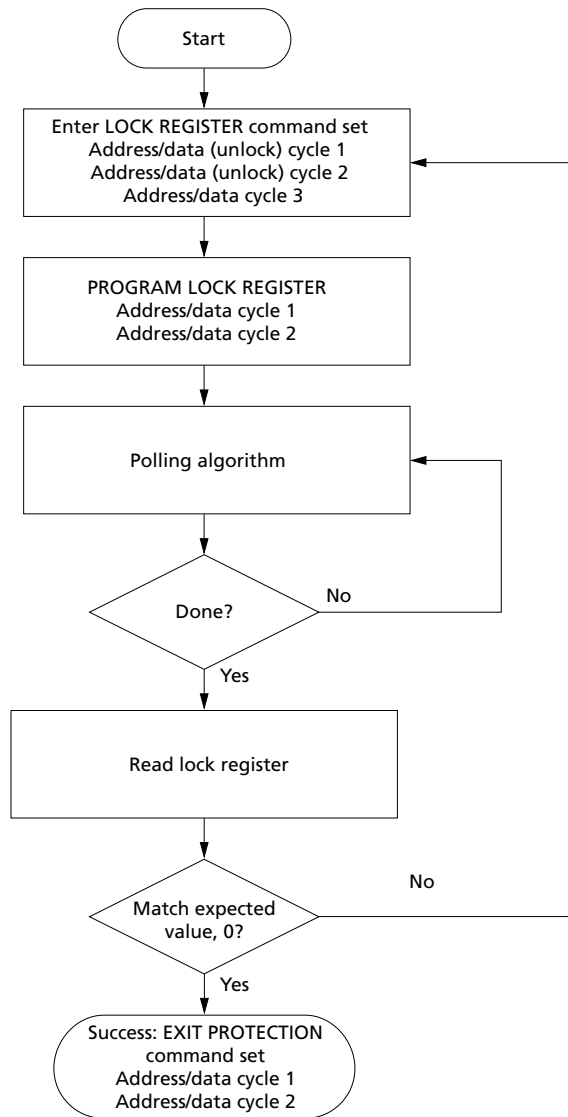
Table 7: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ[15:9]	–	Default value = 1	DQ[15:9] are reserved and are set to a default value of 1.	
DQ8	–	Default value = 0	DQ8 is reserved and is set to a default value of 0.	
DQ[7:3]	–	Default value =1	DQ[7:3] are reserved and are set to a default value of 1.	
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (default)	Places the device in nonvolatile protection mode, with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

- Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved.
 2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Figure 9: Lock Register Program Flowchart



- Notes:
1. Each lock register bit can be programmed only once.
 2. See the Block Protection Command Definitions table for address-data cycle details.
 3. DQ5 and DQ1 are ignored in this algorithm flow.



Standard Command Definitions – Address-Data Cycles

Table 8: Standard Command Definitions – Address-Data Cycles

Note 1 applies to entire table

Command and Code/Subcode	Address and Data Cycles												Notes	
	1st		2nd		3rd		4th		5th		6th			
	A	D	A	D	A	D	A	D	A	D	A	D		
READ and AUTO SELECT Operations														
READ/RESET (F0h)	555	AA	2AA	55	X	F0								2
READ CFI (98h)	555	98												
EXIT READ CFI (F0h)	X	F0												
AUTO SELECT (90h)	555	AA	2AA	55	555	90	Note 3	Note 3						4, 5
EXIT AUTO SELECT (F0h)	X	F0												
READ STATUS (70h)	555	70												
CLEAR STATUS (71h)	555	71												
BYPASS Operations														
UNLOCK BYPASS (20h)	555	AA	2AA	55	555	20								
UNLOCK BYPASS RESET (90h/00h)	X	90	X	00										
PROGRAM Operations														
PROGRAM (A0h)	555	AA	2AA	55	555	A0	PA	PD						
UNLOCK BYPASS PROGRAM (A0h)	X	A0	PA	PD										6
WRITE TO BUFFER PROGRAM (25h)	555	AA	2AA	55	BAd	25	BAd	N	PA	PD				7, 8, 9
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	BAd	25	BAd	N	PA	PD								6
WRITE TO BUFFER PROGRAM CONFIRM (29h)	BAd	29												7
BUFFERED PROGRAM ABORT and RESET (F0h)	555	AA	2AA	55	555	F0								
PROGRAM SUSPEND (B0h)	X	B0												
PROGRAM RESUME (30h)	X	30												
PROGRAM SUSPEND (51h)	X	51												
PROGRAM RESUME (50h)	X	50												
ERASE Operations														
CHIP ERASE (80/10h)	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
UNLOCK BYPASS CHIP ERASE (80/10h)	X	80	X	10										6



Table 8: Standard Command Definitions – Address-Data Cycles (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Address and Data Cycles												Notes
	1st		2nd		3rd		4th		5th		6th		
	A	D	A	D	A	D	A	D	A	D	A	D	
BLOCK ERASE (80/30h)	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30	
UNLOCK BYPASS BLOCK ERASE (80/30h)	X	80	BAd	30									6
ERASE SUSPEND (B0h)	X	B0											
ERASE RESUME (30h)	X	30											
BLANK CHECK Operations													
BLANK CHECK	555	33											

- Notes:
1. A = Address; D = Data; X = "Don't Care"; BAd = Any address in the block; N = Number of words to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
 2. A full three-cycle RESET command sequence must be used to reset the device in the event of a buffered program abort error (DQ1 = 1).
 3. These cells represent READ cycles (versus WRITE cycles for the others).
 4. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
 5. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
 6. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
 7. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
 8. WRITE TO BUFFER PROGRAM operation: maximum cycles = 517. UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 515. WRITE TO BUFFER PROGRAM operation: N + 1 = words to be programmed; maximum buffer size = 512 words.
 9. A[MAX:9] address pins should remain unchanged while A[8:0] pins are used to select a word within the N+1 word page.

READ and AUTO SELECT Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the data polling register. One or three bus WRITE operations can be used to issue the READ/RESET command. Note: A full three-cycle RESET command sequence must be used to reset the device in the event of a buffered program abort error (DQ1 = 1).

Once a PROGRAM, ERASE, or SUSPEND operation begins, RESET commands are ignored until the operation is complete. Read/reset serves primarily to return the device to read mode from a failed PROGRAM or ERASE operation. Read/reset may cause a return to read mode from undefined states that might result from invalid command sequences. A hardware reset may be required to return to normal operation from some undefined states.

To exit the unlock bypass mode, the system must issue a two-cycle UNLOCK BYPASS RESET command sequence. A READ/RESET command will not exit unlock bypass mode.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is only valid when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area (Refer to the Common Flash Interface for details).

Read CFI mode is exited by performing a READ/RESET command (F0h). The device returns to read mode unless it entered read CFI mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information as shown in the Electronic Signature table.
- Block protection, which includes the block protection status and extended memory block protection indicator, as shown in the Block Protection table.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set, as shown in the Read Electronic Signature table or the Block Protection table, respectively. In addition, this device information can be read or set by issuing an AUTO SELECT command.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.



512Mb: x16, 3V, MT28FW, Automotive Parallel NOR READ and AUTO SELECT Operations

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

Auto select mode is exited by performing a READ/RESET command (F0h). The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 9: Block Protection

Note 1 applies to entire table

READ Cycle	CE#	OE#	WE#	Address Input				Data Input/Output
				A[MAX:16]	A[15:2]	A1	A0	DQ[15:0]
128-bit (0x0-0x7) Factory-Programmable Extended Memory Protection Indicator (Bit DQ7)								
Low lock	L	L	H	L	L	H	H	0009h ² 0089h ³
High lock	L	L	H	L	L	H	H	0019h ² 0099h ³
Block protection status								
Protected	L	L	H	Block base address	L	H	L	0001h
Unprotected	L	L	H		L	H	L	0000h

- Notes: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. Customer-lockable (default).
3. Micron prelocked.

Read Electronic Signature

Table 10: Read Electronic Signature – 512Mb

Note 1 applies to entire table

READ Cycle	CE#	OE#	WE#	Address Input					Data Input/Output
				A[MAX:4]	A3	A2	A1	A0	DQ[15:0]
Manufacturer code	L	L	H	L	L	L	L	L	0089h
Device code 1	L	L	H	L	L	L	L	H	227Eh
Device code 2	L	L	H	L	H	H	H	L	2223h
Device code 3	L	L	H	L	H	H	H	H	2201h

- Note: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.

Cyclic Redundancy Check Operation

CYCLIC REDUNDANCY CHECK Command

The CYCLIC REDUNDANCY CHECK (CRC) command is a nonsecure hash function designed to detect accidental changes to raw data. Typically, it is used in digital networks and storage devices such as hard disk drives. A CRC-enabled device calculates a short, fixed-length binary sequence known as the CRC code (or CRC). The device CRC operation will generate the CRC result of the whole device or of an address range specified by the operation. Then the CRC result is compared with the expected CRC data provided in the sequence. Finally, the device indicates a pass or fail through the data polling register. If the CRC fails, corrective action is possible, such as re-verifying with a normal READ mode or rewriting the array data.

CRC is a higher performance alternative to reading data directly to verify recently programmed data, or as a way to periodically check the data integrity of a large block of data against a stored CRC reference over the life of the product.

CRC helps improve test efficiency for programmer or burn-in stress tests. No system hardware changes are required to enable CRC.

The CRC-64 operation follows the ECMA standard; the generating polynomial is:

$$G(x) = x^{64} + x^{62} + x^{57} + x^{55} + x^{54} + x^{53} + x^{52} + x^{47} + x^{46} + x^{45} + x^{40} + x^{39} + x^{38} + x^{37} + x^{35} + x^{33} + x^{32} + x^{31} + x^{29} + x^{27} + x^{24} + x^{23} + x^{22} + x^{21} + x^{19} + x^{17} + x^{13} + x^{12} + x^{10} + x^9 + x^7 + x^4 + x + 1$$

Note: The data stream sequence is from LSB to MSB and the default initial CRC value is all zeros.

The CRC command sequences are shown in the tables below, for an entire die or for a selected range, respectively.

Cyclic Redundancy Check Operation Command Sequence

Table 11: Command Sequence – Range of Blocks

Note 1 and 2 apply to entire table.

Address	DQ[15:0]	Description	Notes
0000555	00AAh	UI unlock cycle 1	
00002AA	0055h	UI unlock cycle 2	
0000000	00EBh	Extended function interface command	
0000000	0027h	CRC sub-op code	
0000000	000Ah	N-1 data count	
0000000	FFFEh	CRC operation option data	
0000001	Data	1st word of 64-bit expected CRC	
0000002	Data	2nd word of 64-bit expected CRC	
0000003	Data	3rd word of 64-bit expected CRC	
0000004	Data	4th word of 64-bit expected CRC	

Table 11: Command Sequence – Range of Blocks (Continued)

Note 1 and 2 apply to entire table.

Address	DQ[15:0]	Description	Notes
0000005	DQ15 = A14 DQ14 = A13 ... DQ2 = A1 DQ1 = A0 DQ0 = set to zero	Byte address to start	3
0000006	A ₃₀ -A ₁₅	Byte address to start	3
0000007	Reserved	Default as 0000h	
0000008	DQ15 = A14 DQ14 = A13 ... DQ2 = A1 DQ1 = A0 DQ0 = set to zero	Byte address to stop	3
0000009	A ₃₀ -A ₁₅	Byte address to stop	3
000000A	Reserved	Default as 0000h	
0000000	0029h	Confirm command	
0000000	Read	Continue data polling to wait for device to be ready	

- Notes:
1. If the CRC check fails, a check error is generated by setting DQ5 = 1.
 2. This is a byte-aligned operation.
 3. The stop address must be bigger than the start address; otherwise, the algorithm will take no action.

Table 12: Command Sequence – Entire Chip

Address	DQ[15:0]	Description
0000555	00AAh	UI unlock cycle 1
00002AA	0055h	UI unlock cycle 2
0000000	00EBh	Extended function interface command
0000000	0027h	CRC sub-op code
0000000	0004h	N-1 data count
0000000	FFFFh	CRC operation option data
0000001	Data	1st word of 64-bit expected CRC
0000002	Data	2nd word of 64-bit expected CRC
0000003	Data	3rd word of 64-bit expected CRC
0000004	Data	4th word of 64-bit expected CRC
0000000	0029h	Confirm command
0000000	Read	Continue data polling to wait for device to be ready

Note: 1. Applies to entire table: If the CRC check fails, a check error is generated by setting DQ5 = 1.

Bypass Operations

UNLOCK BYPASS Command

The UNLOCK BYPASS (20h) command is used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

The UNLOCK BYPASS command is used in conjunction with UNLOCK BYPASS PROGRAM or UNLOCK BYPASS ERASE commands to program or erase the device faster than with standard PROGRAM or ERASE commands. Using these commands can save considerable time when the cycle time to the device is long. When in unlock bypass mode, only the following commands are valid:

- The UNLOCK BYPASS PROGRAM command can be issued to program addresses within the device.
- The UNLOCK BYPASS BLOCK ERASE command can then be issued to erase one or more memory blocks.
- The UNLOCK BYPASS CHIP ERASE command can be issued to erase the whole memory array.
- The UNLOCK BYPASS WRITE TO BUFFER PROGRAM and UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM commands can be issued to speed up the programming operation.
- The UNLOCK BYPASS RESET command can be issued to return the device to read mode.

In unlock bypass mode, the device can be read as if in read mode.

In addition to the UNLOCK BYPASS command, when $V_{PP}/WP\#$ is raised to V_{HH} , the device automatically enters unlock bypass mode. When $V_{PP}/WP\#$ returns to V_{IH} or V_{IL} , the device is no longer in unlock bypass mode, and normal operation resumes. The transitions from V_{IH} to V_{HH} and from V_{HH} to V_{IH} must be slower than t_{VHVPP} . (See the Accelerated Program, Data Polling/Toggle AC Characteristics.)

Note: Micron recommends entering and exiting unlock bypass mode using the ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising $V_{PP}/WP\#$ to V_{HH} . $V_{PP}/WP\#$ should never be raised to V_{PPH} from any mode except read mode; otherwise, the device may be left in an indeterminate state. $V_{PP}/WP\#$ should not remain at V_{HH} for than 80 hours cumulative.

UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

Program Operations

PROGRAM Command

The PROGRAM (A0h) command can be used to program a value to one address in the memory array. The command requires four bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller. After programming has started, bus READ operations output the data polling register content.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESUME command, respectively.

If the address falls in a protected block, the PROGRAM command is ignored, and the data remains unchanged. The data polling register is not read, and no error condition is given.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred. When an error occurs, bus READ operations to the device continue to output the data polling register. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory block or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a hardware reset or by powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

UNLOCK BYPASS PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS PROGRAM (A0h) command can be used to program one address in the memory array. The command requires two bus WRITE operations instead of four required by a standard PROGRAM command; the final WRITE operation latches the address and data and starts the program/erase controller (The standard PROGRAM command requires four bus WRITE operations). The PROGRAM operation using the UNLOCK BYPASS PROGRAM command behaves identically to the PROGRAM operation using the PROGRAM command. The operation cannot be aborted. A bus READ operation to the memory outputs the data polling register.

WRITE TO BUFFER PROGRAM Command

The WRITE TO BUFFER PROGRAM (25h) command makes use of the program buffer to speed up programming and dramatically reduces system programming time compared to the standard non-buffered PROGRAM command. This product supports a 512-word maximum program buffer.

When issuing a WRITE TO BUFFER PROGRAM command, $V_{pp}/WP\#$ can be held HIGH or raised to V_{HH} . Also, it can be held LOW if the block is not the lowest or highest block, depending on the part number.

The following successive steps are required to issue the WRITE TO BUFFER PROGRAM command:

First, two UNLOCK cycles are issued. Next, a third bus WRITE cycle sets up the WRITE TO BUFFER PROGRAM command. The set-up code can be addressed to any location within the targeted block. Then, a fourth bus WRITE cycle sets up the number of words to be programmed. Value n is written to the same block address, where $n + 1$ is the number of words to be programmed. Value $n + 1$ must not exceed the size of the program buffer, or the operation will abort. A fifth cycle loads the first address and data to be programmed. Last, n bus WRITE cycles load the address and data for each word into the program buffer. Addresses must lie within the range from *the start address + 1* to *the start address + (n - 1)*.

Optimum programming performance and lower power usage are achieved by aligning the starting address at the beginning of a 512-word boundary ($A[8:0] = 0x000h$). Any buffer size smaller than 512 words is allowed within a 512-word boundary, while all addresses used in the operation must lie within the 512-word boundary. In addition, any crossing boundary buffer program will result in a program abort.

To program the content of the program buffer, this command must be followed by a WRITE TO BUFFER PROGRAM CONFIRM command.

If an address is written several times during a WRITE TO BUFFER PROGRAM operation, the address/data counter will be decremented at each data load operation, and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or the incorrect sequence of bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The data polling register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

The WRITE TO BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1, and an attempt to do so is masked during the operation. Rather than the WRITE TO BUFFER PROGRAM command, the ERASE command should be used to set memory bits from 0 to 1.

Figure 10: Boundary Condition of Program Buffer Size

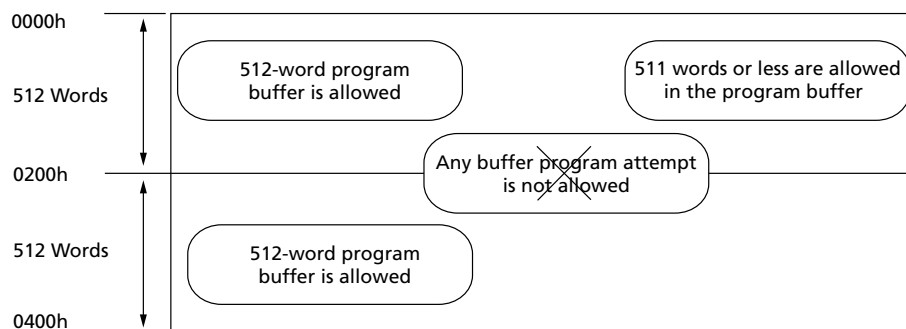
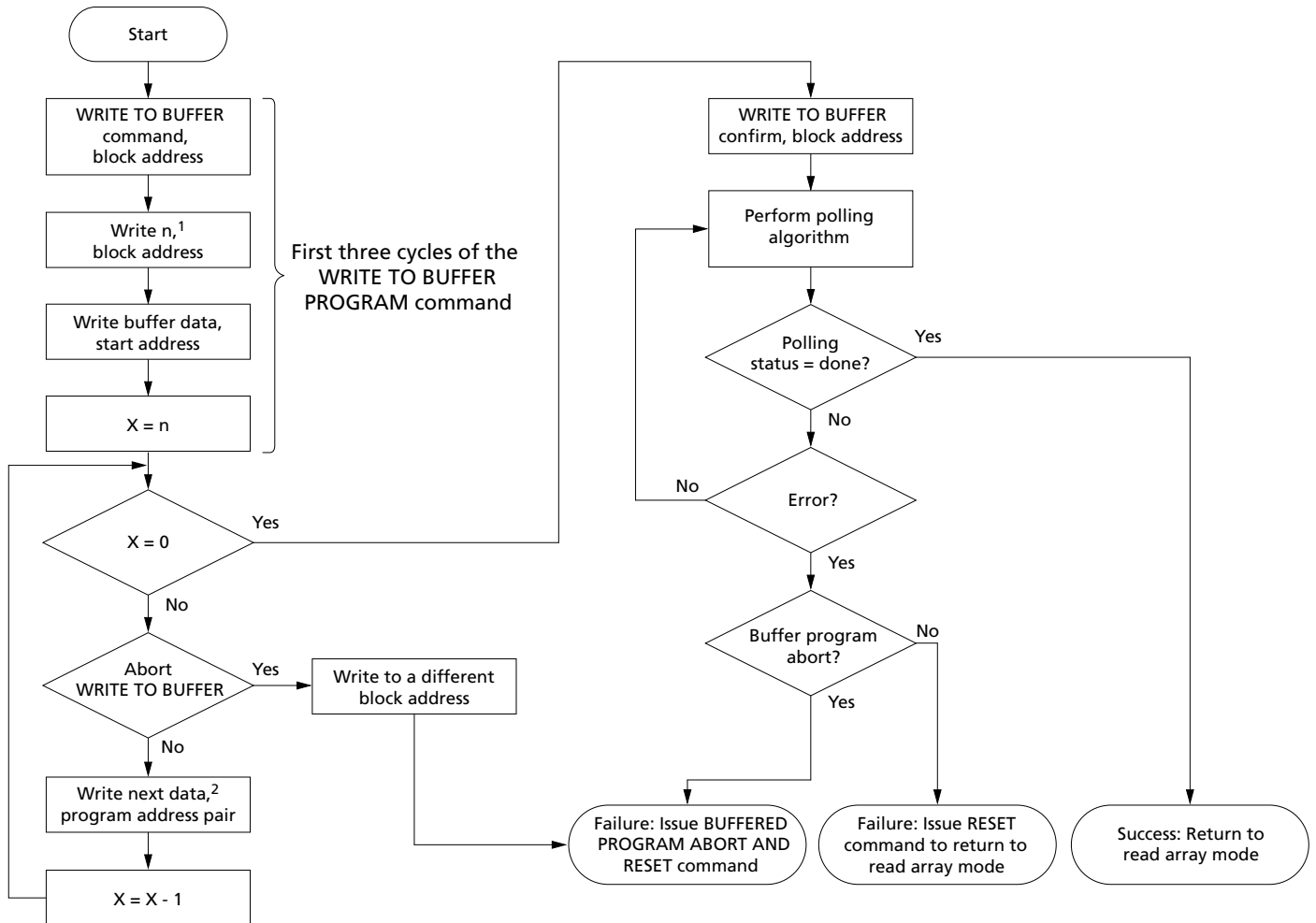


Figure 11: WRITE TO BUFFER PROGRAM Flowchart



- Notes:
1. $n + 1$ is the number of addresses to be programmed.
 2. The BUFFERED PROGRAM ABORT AND RESET command (3 cycles reset) must be issued to return the device to read mode.
 3. When the block address is specified, any address in the selected block address space is acceptable. However, when loading program buffer address with data, all addresses must fall within the selected program buffer page.

UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS WRITE TO BUFFER (25h) command can be used to program the device in fast program mode. The command requires two bus WRITE operations fewer than the standard WRITE TO BUFFER PROGRAM command.

The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command behaves the same way as the WRITE TO BUFFER PROGRAM command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register.

The WRITE TO BUFFER PROGRAM CONFIRM command is used to confirm an UNLOCK BYPASS WRITE TO BUFFER PROGRAM command and to program the $n + 1$ words loaded in the program buffer by this command.

WRITE TO BUFFER PROGRAM CONFIRM Command

The WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm a WRITE TO BUFFER PROGRAM command and to program the $n + 1$ words loaded in the program buffer by this command.

BUFFERED PROGRAM ABORT AND RESET Command

A BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to reset the device to read mode when the BUFFER PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program in the WRITE TO BUFFER PROGRAM command.
- Write to an address in a different block than the one specified during the WRITE BUFFER LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.

The abort condition is indicated by $DQ1 = 1$, $DQ7 = DQ7\#$ (for the last address location loaded), $DQ6 = \text{toggle}$, and $DQ5 = 0$ (all of which are data polling register bits). A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

PROGRAM SUSPEND Command

The PROGRAM SUSPEND command can be used to interrupt a program operation so that data can be read from another block. When the PROGRAM SUSPEND command is issued during a program operation, the device suspends the operation within the program suspend latency time and updates the data polling register bits.

After the PROGRAM operation has been suspended, data can be read from any address. However, data is invalid when read from an address where a program operation has been suspended.

The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any address not in erase suspend or program suspend mode. To read from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequences must be issued.

The system may also issue the AUTO SELECT command sequence when the device is in program suspend mode. The system can read as many auto select codes as required. When the device exits auto select mode, the device reverts to program suspend mode and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power-down. In this case, data integrity cannot be ensured, and it is recommended that the words that were aborted be reprogrammed. This device has two different command codes for program suspend, B0h and 51h. Code B0h is available for legacy compatibility. Code 51h is recommended for use.

PROGRAM RESUME Command

The PROGRAM RESUME command must be issued to exit a program suspend mode and resume a PROGRAM operation. The controller can use DQ7 or DQ6 data polling bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming. This device has two different command codes for Program Resume (30h or 50h). Code 30h is available for legacy compatibility. Code 50h is recommended to use.

ACCELERATED BUFFERED PROGRAM Operations

ACCELERATED BUFFER PROGRAM operations provides faster performance than standard program command sequences. Operations are enabled through $V_{PP}/WP\#$ under the V_{HH} voltage supply.

When the system asserts V_{HH} on input, the device automatically enters the UNLOCK BYPASS mode, which enables the system to use the UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h) command sequence.

Removing V_{HH} from the V_{PP} upon completion of the embedded program operation returns the device to normal operation.

Table 13: ACCELERATED PROGRAM Requirements and Recommendations

Device State	Requirements/Recommendations
Device blocks	Requirement: Must be unprotected prior to raising $V_{PP}/WP\#$ to V_{HH}
V_{HH} applied to $V_{PP}/WP\#$	Requirement: Maximum cumulative period of 80 hours.
$V_{PP}/WP\#$	<p>Requirement: Must not be at V_{HH} for operations except ACCELERATED BUFFERED PROGRAM and CHIP ERASE; otherwise device can be damaged</p> <p>Recommendation: Keep stable to V_{HH} during ACCELERATED BUFFERED PROGRAM operation</p>
Power-up	Recommendation: Apply V_{HH} on $V_{PP}/WP\#$ after V_{CC}/V_{CCQ} is stable on.
Power-down	Recommendation: Adjust $V_{PP}/WP\#$ from V_{HH} to V_{IH}/V_{IL} before V_{CC}/V_{CCQ} goes LOW.

Erase Operations

CHIP ERASE Command

The CHIP ERASE (80/10h) command erases the entire chip. Six bus WRITE operations are required to issue the command and start the program/erase controller.

Protected blocks are not erased. If all blocks are protected, the data remains unchanged. No error is reported when protected blocks are not erased.

During the CHIP ERASE operation, the device ignores all other commands, including ERASE SUSPEND. It is not possible to abort the operation. All bus READ operations during CHIP ERASE output the data polling register on the data I/Os. See the Data Polling Register section for more details.

After the CHIP ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, the device will continue to output the data polling register.

When the operation fails, a READ/RESET command must be issued to reset the error condition and return to read mode. The status of the array must be confirmed through the BLANK CHECK operation and the BLOCK ERASE command re-issued to the failed block.

The CHIP ERASE command sets all of the bits in unprotected blocks of the device to 1. All previous data is lost.

The operation is aborted by performing a reset or by powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the entire chip be erased again.

UNLOCK BYPASS CHIP ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS CHIP ERASE (80/10h) command can be used to erase all memory blocks at one time. The command requires only two bus WRITE operations instead of six using the standard CHIP ERASE command. The final bus WRITE operation starts the program/erase controller.

The UNLOCK BYPASS CHIP ERASE command behaves the same way as the CHIP ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register.

BLOCK ERASE Command

The BLOCK ERASE (80/30h) command erase one block. It sets all bits in the unprotected selected block to 1. All previous data in the selected block are lost. Six bus WRITE operations are required to select the block to be erased.

After the sixth bus WRITE operation, a bus READ operation outputs the data polling register. See the WE#-Controlled Program waveforms for details on how to identify if the program/erase controller has started the BLOCK ERASE operation.

After the BLOCK ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, bus READ operations will continue to output the data polling register. A READ/RESET command must be issued to reset the error condition and return to read mode.

If the selected block is protected, it is ignored and the data remains unchanged. No error condition is given when protected block is not erased.

During the BLOCK ERASE operation, the device ignores all commands except the ERASE SUSPEND command and the READ STATUS command. The operation is aborted by performing a hardware reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted blocks be erased again.

UNLOCK BYPASS BLOCK ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS BLOCK ERASE (80/30h) command can be used to erase one memory block. The command requires two bus WRITE operations instead of six using the standard BLOCK ERASE command. The final bus WRITE operation latches the address of the block and starts the program/erase controller.

The UNLOCK BYPASS BLOCK ERASE command behaves the same way as the BLOCK ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register. See the BLOCK ERASE Command section for details.

ERASE SUSPEND Command

The ERASE SUSPEND (B0h) command temporarily suspends a BLOCK ERASE operation. One bus WRITE operation is required to issue the command. The block address is "Don't Care."

The program/erase controller suspends the ERASE operation within the erase suspend latency time of the ERASE SUSPEND command being issued. However, when the ERASE SUSPEND command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation. After the program/erase controller has stopped, the device operates in read mode, and the erase is suspended.

During an ERASE SUSPEND operation, it is possible to execute these operations in arrays that are not suspended:

- READ (main memory array)
- PROGRAM
- WRITE TO BUFFER PROGRAM
- AUTO SELECT
- READ CFI
- UNLOCK BYPASS
- Extended memory block commands
- READ/RESET

Reading from a suspended block will output the data polling register. If an attempt is made to program in a protected or suspended block, the PROGRAM command is ignored and the data remains unchanged; also, the data polling register is not read and no error condition is given.

Before the RESUME command is initiated, the READ/RESET command must be issued to exit AUTO SELECT and READ CFI operations. In addition, the EXIT UNLOCK BYPASS

and EXIT EXTENDED MEMORY BLOCK commands must be issued to exit unlock bypass and the extended memory block modes.

An ERASE SUSPEND command is ignored if it is written during a CHIP ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device hardware reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended blocks be erased again.

ERASE RESUME Command

The ERASE RESUME (30h) command restarts the program/erase controller after an ERASE SUSPEND operation.

The device must be in read array mode before the RESUME command will be accepted. An erase can be suspended and resumed more than once.

ACCELERATED CHIP ERASE Operations

The ACCELERATED CHIP ERASE operation provides faster performance than the standard CHIP ERASE command sequence. Operations are enabled through $V_{pp}/WP\#$ under the V_{HH} voltage supply.

When the system asserts V_{HH} on input, the device automatically enters the UNLOCK BYPASS mode, which enables the system to use the UNLOCK BYPASS CHIP ERASE (80/30h) command sequence.

When a block is protected, the CHIP ERASE command skips the protected block and continues with next block erase. The command algorithm skips a block that failed to erase and continues with the remaining blocks. The fail flag will be set for the operation.

Removing V_{HH} from the $V_{pp}/WP\#$ upon completion of the embedded erase operation returns the device to normal operation. When an error occurs or when the operation fails, the array status should be confirmed through the BLANK CHECK operation and the BLOCK ERASE command re-issued to the failed block.

Table 14: ACCELERATED CHIP ERASE Requirements and Recommendations

Device Component/State	Requirements/Recommendations
$V_{pp}/WP\#$	Requirement: Must not be at V_{HH} for operations except ACCELERATED PROGRAM and CHIP ERASE; otherwise device can be damaged.
V_{HH} applied to $V_{pp}/WP\#$	Requirement: Maximum cumulative period of 80 hours.
Power-up	Recommendation: Apply V_{HH} on $V_{pp}/WP\#$ after V_{CC}/V_{CCQ} is stable on.
Power-down	Recommendation: Adjust $V_{pp}/WP\#$ from V_{HH} to V_{IH}/V_{IL} before V_{CC}/V_{CCQ} goes LOW.

BLANK CHECK Operation

The BLANK CHECK operation determines whether a specified block is blank (that is, completely erased). It can also be used to determine whether a previous ERASE operation was successful, including ERASE operations that might have been interrupted by power loss.

The BLANK CHECK operation checks for cells that are programmed or over-erased. If it finds any, it returns a failure status, indicating that the block is not blank. If it returns a passing status, the block is guaranteed blank (all 1s) and is ready to program.

Before executing, the ERASE operation initiates an embedded BLANK CHECK operation, and if the target block is blank, the ERASE operation is skipped, benefitting overall cycle performance; otherwise, the ERASE operation continues.

The BLANK CHECK operation can occur in only one block at a time, and during its execution, reading the data polling register is the only other operation allowed. Reading from any address in the device enables reading the data polling register to monitor blank check progress or errors. Operations such as READ (array data), PROGRAM, ERASE, and any suspended operation are not allowed.

After the BLANK CHECK operation has completed, the device returns to read mode unless an error has occurred. When an error occurs, the device continues to output data polling register data. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

Device Protection

Hardware Protection

The $V_{PP}/WP\#$ function provides a hardware method of protecting either the highest or lowest block. When $V_{PP}/WP\#$ is LOW, PROGRAM and ERASE operations on either of these block options is ignored to provide protection. When $V_{PP}/WP\#$ is HIGH, the device reverts to the previous protection status for the highest or lowest block. PROGRAM and ERASE operations can modify the data in either of these block options unless block protection is enabled.

Note: Micron highly recommends driving $V_{PP}/WP\#$ HIGH or LOW. If a system needs to float the $V_{PP}/WP\#$ pin, without a pull-up/pull-down resistor and no capacitor, then an internal pull-up resistor is enabled.

Table 15: $V_{PP}/WP\#$ Functions

$V_{PP}/WP\#$ Settings	Function
V_{IL}	Highest or lowest block is protected.
V_{IH}	Highest or lowest block is unprotected unless software protection is activated.

Software Protection

The following software protection modes are available:

- Volatile protection
- Nonvolatile protection
- Password protection

The device is shipped with all blocks unprotected. On first use, the device defaults to the nonvolatile protection mode but can be activated in either the nonvolatile protection or password protection mode.

The desired protection mode is activated by setting either the nonvolatile protection mode lock bit or the password protection mode lock bit of the lock register (see the Lock Register section). Both bits are one-time-programmable and nonvolatile; therefore, after the protection mode has been activated, it cannot be changed, and the device is set permanently to operate in the selected protection mode. It is recommended that the desired software protection mode be activated when first programming the device.

For the highest or lowest block, a higher level of block protection can be achieved by locking the block using nonvolatile protection mode and holding $V_{PP}/WP\#$ LOW.

Blocks with volatile protection and nonvolatile protection can coexist within the memory array. If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The block protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command (see the Block Protection table).

Refer to the Block Protection Status table and the Software Protection Scheme figure for details on the block protection scheme. Refer to the Protection Operations section for a description of the command sets.

Volatile Protection Mode

Volatile protection enables the software application to protect blocks against inadvertent change and can be disabled when changes are needed. Volatile protection bits are unique for each block and can be individually modified. Volatile protection bits control the protection scheme only for unprotected blocks whose nonvolatile protection bits are cleared to 1. Issuing a PROGRAM VOLATILE PROTECTION BIT or CLEAR VOLATILE PROTECTION BIT command sets to 0 or clears to 1 the volatile protection bits and places the associated blocks in the protected (0) or unprotected (1) state, respectively. The volatile protection bit can be set or cleared as often as needed.

When the device is first shipped, or after a power-up or hardware reset, the volatile protection bits default to 1 (unprotected).

Nonvolatile Protection Mode

A nonvolatile protection bit is assigned to each block. Each of these bits can be set for protection individually by issuing a PROGRAM NONVOLATILE PROTECTION BIT command. Also, each device has one global volatile bit called the nonvolatile protection bit lock bit; it can be set to protect all nonvolatile protection bits at once. This global bit must be set to 0 only after all nonvolatile protection bits are configured to the desired settings. When set to 0, the nonvolatile protection bit lock bit prevents changes to the state of the nonvolatile protection bits. When cleared to 1, the nonvolatile protection bits can be set and cleared using the PROGRAM NONVOLATILE PROTECTION BIT and CLEAR ALL NONVOLATILE PROTECTION BITS commands, respectively.

No software command unlocks the nonvolatile protection bit lock bit unless the device is in password protection mode; in nonvolatile protection mode, the nonvolatile protection bit lock bit can be cleared only by taking the device through a hardware reset or power-up.

Nonvolatile protection bits cannot be cleared individually; they must be cleared all at once using a CLEAR ALL NONVOLATILE PROTECTION BITS command. They will remain set through a hardware reset or a power-down/power-up sequence.

If one of the nonvolatile protection bits needs to be cleared (unprotected), additional steps are required: First, the nonvolatile protection bit lock bit must be cleared to 1, using either a power-cycle or hardware reset. Then, the nonvolatile protection bits can be changed to reflect the desired settings. Finally, the nonvolatile protection bit lock bit must be set to 0 to lock the nonvolatile protection bits. The device now will operate normally.

To achieve the best protection, the PROGRAM NONVOLATILE PROTECTION LOCK BIT command should be executed early in the boot code, and the boot code should be protected by holding $V_{PP}/WP\#$ LOW.

Nonvolatile protection bits and volatile protection bits have the same function when $V_{PP}/WP\#$ is HIGH or when $V_{PP}/WP\#$ is at the voltage for program acceleration (V_{HH}).

Password Protection Mode

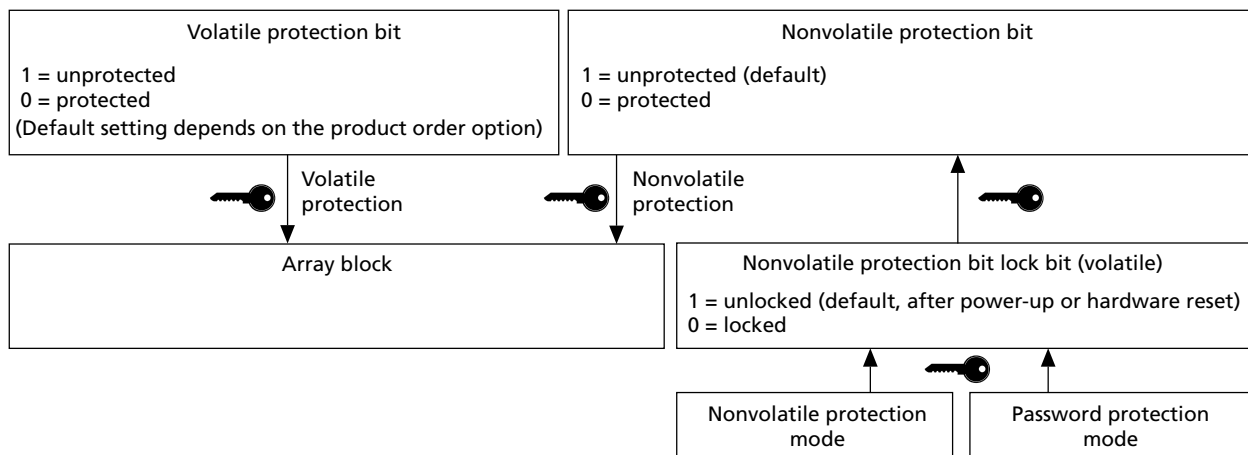
The password protection mode provides a higher level of security than the nonvolatile protection mode by requiring a 64-bit password to unlock the nonvolatile protection bit lock bit. In addition to this password requirement, the nonvolatile protection bit lock bit is set to 0 after power-up and reset to maintain the device in password protection mode.

Executing the UNLOCK PASSWORD command by entering the correct password clears the nonvolatile protection bit lock bit, enabling the block nonvolatile protection bits to be modified. If the password provided is incorrect, the nonvolatile protection bit lock bit remains locked, and the state of the nonvolatile protection bits cannot be modified.

To place the device in password protection mode, the following two steps are required: First, before activating the password protection mode, a 64-bit password must be set and the setting verified. Password verification is allowed only before the password protection mode is activated. Next, password protection mode is activated by programming the password protection mode lock bit to 0. This operation is irreversible. After the bit is programmed, it cannot be erased, the device remains permanently in password protection mode, and the 64-bit password can be neither retrieved nor reprogrammed. In addition, all commands to the address where the password is stored are disabled.

Note: There is no means to verify the password after password protection mode is enabled. If the password is lost after enabling the password protection mode, there is no way to clear the nonvolatile protection bit lock bit.

Figure 12: Software Protection Scheme



- Notes:
1. Volatile protection bits are programmed and cleared individually. Nonvolatile protection bits are programmed individually and cleared collectively.
 2. Once programmed to 0, the nonvolatile protection bit lock bit can be reset to 1 only by taking the device through a power-up or hardware reset.

Table 16: Block Protection Status

Nonvolatile Protection Bit Lock Bit ¹	Nonvolatile Protection Bit ²	Volatile Protection Bit ³	Block Protection Status ⁴	Block Protection Status
1	1	1	00h	Block unprotected; nonvolatile protection bit changeable.
1	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit changeable.
1	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit changeable.
1	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit changeable.
0	1	1	00h	Block unprotected; nonvolatile protection bit unchangeable.
0	1	0	01h	Block protected by volatile protection bit; nonvolatile protection bit unchangeable.
0	0	1	01h	Block protected by nonvolatile protection bit; nonvolatile protection bit unchangeable.
0	0	0	01h	Block protected by nonvolatile protection bit and volatile protection bit; nonvolatile protection bit unchangeable.

- Notes:
1. Nonvolatile protection bit lock bit: when cleared to 1, all nonvolatile protection bits are unlocked; when set to 0, all nonvolatile protection bits are locked.
 2. Block nonvolatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
 3. Block volatile protection bit: when cleared to 1, the block is unprotected; when set to 0, the block is protected.
 4. Block protection status is checked under AUTO SELECT mode.



Block Protection Command Definitions – Address-Data Cycles

Table 17: Block Protection Command Definitions – Address-Data Cycles

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Address and Data Cycles											Notes	
	1st		2nd		3rd		4th		...	nth			
	A	D	A	D	A	D	A	D		A	D		
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	555	AA	2AA	55	555	40							3
PROGRAM LOCK REGISTER (A0h)	X	A0	X	Data									5
READ LOCK REGISTER	X	Data											4, 5, 6
EXIT LOCK REGISTER (90h/00h)	X	90	X	00									3
PASSWORD PROTECTION Commands													
ENTER PASSWORD PROTECTION COMMAND SET (60h)	555	AA	2AA	55	555	60							3
PROGRAM PASSWORD (A0h)	X	A0	PWAn	PWDn									7
READ PASSWORD	00	PWD0	01	PWD1	02	PWD2	03	PWD3					4, 6, 8
UNLOCK PASSWORD (25h/03h)	00	25	00	03	00	PWD0	01	PWD1	...	00	29		8
EXIT PASSWORD PROTECTION (90h/00h)	X	90	X	00									3
NONVOLATILE PROTECTION Commands													
ENTER NONVOLATILE PROTECTION COMMAND SET (C0h)	555	AA	2AA	55	555	C0							3
PROGRAM NONVOLATILE PROTECTION BIT (A0h)	X	A0	BAd	00									9
READ NONVOLATILE PROTECTION BIT STATUS	BAd	READ (DQ0)											4, 6, 9
CLEAR ALL NONVOLATILE PROTECTION BITS (80h/30h)	X	80	00	30									10
EXIT NONVOLATILE PROTECTION (90h/00h)	X	90	X	00									3
NONVOLATILE PROTECTION BIT LOCK BIT Commands													



Table 17: Block Protection Command Definitions – Address-Data Cycles (Continued)

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Address and Data Cycles										Notes	
	1st		2nd		3rd		4th		...	nth		
	A	D	A	D	A	D	A	D		A		D
ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h)	555	AA	2AA	55	555	50	Gray				3	
PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h)	X	A0	X	00	Gray				9			
READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS	X	READ (DQ0)	Gray						4, 6, 9			
EXIT NONVOLATILE PROTECTION BIT LOCK BIT (90h/00h)	X	90	X	00	Gray				3			
VOLATILE PROTECTION Commands												
ENTER VOLATILE PROTECTION COMMAND SET (E0h)	555	AA	2AA	55	555	E0	Gray				3	
PROGRAM VOLATILE PROTECTION BIT (A0h)	X	A0	BAd	00	Gray				9			
READ VOLATILE PROTECTION BIT STATUS	BAd	READ (DQ0)	Gray						4, 6			
CLEAR VOLATILE PROTECTION BIT (A0h)	X	A0	BAd	01	Gray				9			
EXIT VOLATILE PROTECTION (90h/00h)	X	90	X	00	Gray				3			
EXTENDED MEMORY BLOCK Operations												
ENTER EXTENDED MEMORY BLOCK (88h)	555	AA	2AA	55	555	88	Gray					
PROGRAM EXTENDED MEMORY BLOCK (A0h)	555	AA	2AA	55	555	A0	Word address	data	Gray			
READ EXTENDED MEMORY BLOCK	Word address	data	Gray									
EXIT EXTENDED MEMORY BLOCK (90h/00h)	555	AA	2AA	55	555	90	X	00	Gray			

Notes: 1. Key: A = Address and D = Data; X = "Don't Care;" BAd = Any address in the block; PWDn = Password words, n = 0 to 3; PWA_n = Password address, n = 0 to 3; Gray = Not applicable. All values in the table are hexadecimal.

2. DQ[15:8] are "Don't Care" during UNLOCK and COMMAND cycles. A[MAX:16] are "Don't Care" during UNLOCK and COMMAND cycles, unless an address is required.
3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to block 0. READ and WRITE operations from and to any other block are allowed. Also, when an ENTER COMMAND SET command is issued, an EXIT COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock register content.
6. All address cycles shown for this command are READ cycles.
7. Only one portion of the password can be programmed or read by each PROGRAM PASSWORD command.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
9. Both nonvolatile and volatile protection bit settings are as follows: Protected state = 00; Unprotected state = 01.
10. The CLEAR ALL NONVOLATILE PROTECTION BITS command programs all nonvolatile protection bits before erasure. This prevents over-erasure of previously cleared nonvolatile protection bits.

Protection Operations

Blocks can be protected individually against accidental PROGRAM or ERASE operations. The block protection scheme is shown in the Software Protection Scheme figure. Memory block and extended memory block protection is configured through the lock register.

LOCK REGISTER Commands

After the ENTER LOCK REGISTER COMMAND SET (40h) command has been issued, all bus READ or PROGRAM operations can be issued to the lock register.

The PROGRAM LOCK REGISTER (A0h) command allows the lock register to be configured. The programmed data can then be checked with a READ LOCK REGISTER command by driving CE# and OE# LOW with the appropriate address data on the address bus.

PASSWORD PROTECTION Commands

After the ENTER PASSWORD PROTECTION COMMAND SET (60h) command has been issued, the commands related to password protection mode can be issued to the device.

The PROGRAM PASSWORD (A0h) command is used to program the 64-bit password used in the password protection mode. To program the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A[1:0]. By default, all password bits are set to 1. The password can be checked by issuing a READ PASSWORD command.

Note: A password must be programmed per Flash memory die to enable password protection.

The READ PASSWORD command is used to verify the password used in password protection mode. To verify the 64-bit password, the complete command sequence must be entered four times at four consecutive addresses selected by A[1:0]. If the password mode lock bit is programmed and the user attempts to read the password, the device will output 00h onto the I/O data bus.

The UNLOCK PASSWORD (25/03h) command is used to clear the nonvolatile protection bit lock bit, allowing the nonvolatile protection bits to be modified. The UNLOCK PASSWORD command must be issued, along with the correct password, and requires a 6 μ s delay between successive UNLOCK PASSWORD commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay does not occur, the latest command will be ignored. Approximately 6 μ s is required for unlocking the device after the valid 64-bit password has been provided.

NONVOLATILE PROTECTION Commands

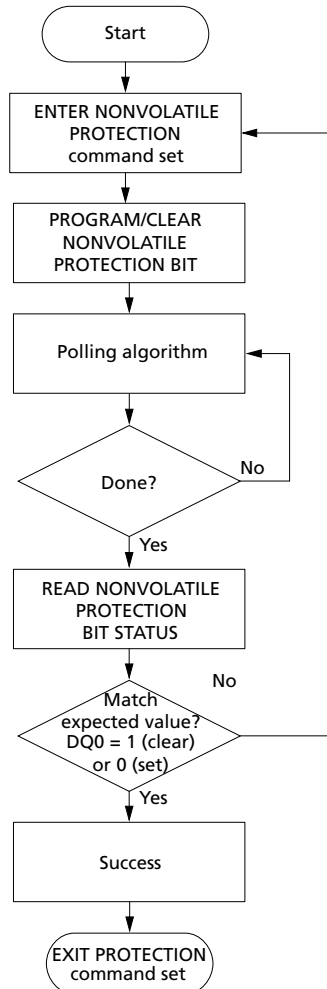
After the ENTER NONVOLATILE PROTECTION COMMAND SET (C0h) command has been issued, the commands related to nonvolatile protection mode can be issued to the device.

A block can be protected from program or erase by issuing a PROGRAM NONVOLATILE PROTECTION BIT (A0h) command, along with the block address. This command sets the nonvolatile protection bit to 0 for a given block.

The status of a nonvolatile protection bit for a given block or group of blocks can be read by issuing a READ NONVOLATILE MODIFY PROTECTION BIT command, along with the block address.

The nonvolatile protection bits are erased simultaneously by issuing a CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h) command. No specific block address is required. If the nonvolatile protection bit lock bit is set to 0, the command fails.

Figure 13: Set/Clear Nonvolatile Protection Bit Algorithm Flowchart



- Notes:
1. See the Block Protection Command Definitions table for address-data cycle details.
 2. DQ5 and DQ1 are ignored in this algorithm flow.

NONVOLATILE PROTECTION BIT LOCK BIT Commands

After the ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h) command has been issued, the commands that allow the nonvolatile protection bit lock bit to be set can be issued to the device.

The PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h) command is used to set the nonvolatile protection bit lock bit to 0, thus locking the nonvolatile protection bits and preventing them from being modified.

The READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS command is used to read the status of the nonvolatile protection bit lock bit.

VOLATILE PROTECTION Commands

After the ENTER VOLATILE PROTECTION COMMAND SET (E0h) command has been issued, commands related to the volatile protection mode can be issued to the device.

The PROGRAM VOLATILE PROTECTION BIT (A0h) command individually sets a volatile protection bit to 0 for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit (see the Block Protection Status table).

The status of a volatile protection bit for a given block can be read by issuing a READ VOLATILE PROTECTION BIT STATUS command along with the block address.

The CLEAR VOLATILE PROTECTION BIT (A0h) command individually clears (sets to 1) the volatile protection bit for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit (see the Block Protection Status table).

EXTENDED MEMORY BLOCK Commands

The device has one extra 512-word extended memory block that can be accessed only by the ENTER EXTENDED MEMORY BLOCK (88h) command. It is used as a security block to provide a permanent 128-bit secure ID number or to store additional information. The device can be shipped with the extended memory block prelocked permanently by Micron, including the 128-bit security identification number. Or, the device can be shipped with the extended memory block unlocked, enabling customers to permanently program and lock it (default) (see Lock Register, the AUTO SELECT command, and the Block Protection table.)

Table 18: Extended Memory Block Address and Data

Address	Data	
	Micron Prelocked	Customer Lockable
000000h–000007h	Secure ID number	Determined by customer (default)
000008h–0001FFh	Protected and unavailable	

After the ENTER EXTENDED MEMORY BLOCK command has been issued, the device enters the extended memory block mode. All bus READ or PROGRAM operations are conducted on the extended memory block, and the extended memory block is addressed using the addresses occupied by block 0 in the other operating modes (see the Memory Map table).

In extended memory block mode, ERASE, CHIP ERASE, ERASE SUSPEND, and ERASE RESUME commands are not allowed. The extended memory block cannot be erased, and each bit of the extended memory block can only be programmed once.

The extended memory block is protected from further modification by programming lock register bit 0. Once invoked, this protection cannot be undone.

The device remains in extended memory block mode until the EXIT EXTENDED MEMORY BLOCK (90/00h) command is issued, which returns the device to read mode, or until power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading memory blocks in the main array.

EXIT PROTECTION Command

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

Note that the READ/RESET command (F0h) is ignored under these modes.

Common Flash Interface

The common Flash interface (CFI) is a JEDEC-approved, standardized data structure that can be read from the Flash memory device. It allows a system's software to query the device to determine various electrical and timing parameters, density information, and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the READ CFI command is issued, the device enters CFI query mode and the data structure is read from memory. The following tables show the addresses (A[7:0]) used to retrieve the data. The query data is always presented on the lowest order data outputs (DQ[7:0]), and the other data outputs (DQ[15:8]) are set to 0.

Table 19: Query Structure Overview

Note 1 applies to the entire table

Address	Subsection Name	Description
10h	CFI query identification string	Command set ID and algorithm data offset
1Bh	System interface information	Device timing and voltage information
27h	Device geometry definition	Flash device layout
40h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.

Table 20: CFI Query Identification String

Note 1 applies to the entire table

Address	Data	Description	Value
10h	0051h	Query unique ASCII string "QRY"	"Q"
11h	0052h		"R"
12h	0059h		"Y"
13h 14h	0002h 0000h	Primary algorithm command set and control interface ID code 16-bit ID code defining a specific algorithm	–
15h 16h	0040h 0000h	Address for primary algorithm extended query table (see the Primary Algorithm-Specific Extended Query Table)	P = 40h
17h 18h	0000h 0000h	Alternate vendor command set and control interface ID code second vendor-specified algorithm supported	–
19h 1Ah	0000h 0000h	Address for alternate algorithm extended query table	–

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.



Table 21: CFI Query System Interface Information

Note 1 applies to the entire table

Address	Data	Description	Value
1Bh	0027h	V _{CC} logic supply minimum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	2.7V
1Ch	0036h	V _{CC} logic supply maximum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	3.6V
1Dh	0085h	V _{HH} (programming) supply minimum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	8.5V
1Eh	0095h	V _{HH} (programming) supply maximum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 10mV	9.5V
1Fh	0005h	Typical timeout for single byte/word program = 2 ⁿ μs	32μs
20h	0009h	Typical timeout for maximum size buffer program = 2 ⁿ μs	512μs
21h	0008h	Typical timeout per individual block erase = 2 ⁿ ms	256ms
22h	0011h	Typical timeout for full chip erase = 2 ⁿ ms	131s
23h	0003h	Maximum timeout for byte/word program = 2 ⁿ times typical	256μs
24h	0002h	Maximum timeout for buffer program = 2 ⁿ times typical	2048μs
25h	0002h	Maximum timeout per individual block erase = 2 ⁿ times typical	1100ms
26h	0003h	Maximum timeout for chip erase = 2 ⁿ times typical	1048s

Note: 1. The values in this table are valid for all packages.

Table 22: Device Geometry Definition

Address	Data	Description	Value
27h	001Ah	Device size = 2 ⁿ in number of bytes	64MB
28h	0001h	Flash device interface code description	x16 asynchronous
29h	0000h		
2Ah	000Ah	Maximum number of bytes in multi-byte program or page = 2 ⁿ	1024
2Bh	0000h		
2Ch	0001h	Number of erase block regions. It specifies the number of regions containing contiguous erase blocks of the same size.	1
2Dh	00FFh	Erase block region 1 information	512
2Eh	0001h	Number of identical-size erase blocks = 01FFh + 1	
2Fh	0000h	Erase block region 1 information	128KB
30h	0002h	Block size in region 1 = 0200h × 256 bytes	
31h	0000h	Erase block region 2 information	0
32h	0000h		
33h	0000h		
34h	0000h		

Table 22: Device Geometry Definition (Continued)

Address	Data	Description	Value
35h	0000h	Erase block region 3 information	0
36h	0000h		
37h	0000h		
38h	0000h		
39h	0000h	Erase block region 4 information	0
3Ah	0000h		
3Bh	0000h		
3Ch	0000h		
3Dh	FFFFh	Reserved	-
3Eh	FFFFh		
3Fh	FFFFh		

Table 23: Primary Algorithm-Specific Extended Query Table

Note 1 applies to the entire table

Address	Data	Description	Value
40h	0050h	Primary algorithm extended query table unique ASCII string "PRI"	"P"
41h	0052h		"R"
42h	0049h		"I"
43h	0031h	Major version number, ASCII	"1"
44h	0035h	Minor version number, ASCII	"5"
45h	001Ch	Address sensitive unlock (bits[1:0]): 00 = Required 01 = Not required Process technology (bits [7:2]) 0111b: Second generation	Required
46h	0002h	Erase suspend: 00 = Not supported 01 = Read only 02 = Read and write	2
47h	0001h	Block protection: 00 = Not supported x = Number of blocks per group	1
48h	0000h	Temporary block unprotect scheme: 00 = Not supported 01 = Supported	Not supported
49h	0008h	Protect/unprotect scheme: 08 = Advanced sector protection method	8
4Ah	0000h	Simultaneous operations: Not supported	-
4Bh	0000h	Burst mode: 00 = Not supported 01 = Supported	Not supported

Table 23: Primary Algorithm-Specific Extended Query Table (Continued)

Note 1 applies to the entire table

Address	Data	Description	Value
4Ch	0003h	Page mode: 00 = Not supported 01 = 4-word page 02 = 8-word page 03 = 16-word page	16-word page
4Dh	0085h	V _{HH} supply minimum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	8.5V
4Eh	0095h	V _{HH} supply maximum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	9.5V
4Fh	00xxh	WP# protection: xx = 04h: Uniform device, HW protection for lowest block xx = 05h: Uniform device, HW protection for highest block	Uniform + V _{pp} /WP# protecting highest or lowest block
50h	0001h	Program suspend: 00 = Not supported 01 = Supported	Supported
51h	0001h	Unlock bypass: 00 = Not supported 01 = Supported	Supported
52h	000Ah	Extended memory block (customer OTP area): 2 ⁿ bytes	1024 bytes

Table 23: Primary Algorithm-Specific Extended Query Table (Continued)

Note 1 applies to the entire table

Address	Data	Description	Value
53h	008Fh	Software Features	-
		bit 0: Status register polling 00 = Not supported 01 = Supported)	
		bit 1: DQ polling 00 = Not supported 01 = Supported)	
		bit 2: Program suspend/resume commands 00 = Not supported 01 = Supported)	
		bit 3: Word programming 00 = Not supported 01 = Supported)	
		bit 4: Bit-field programming 00 = Not supported 01 = Supported)	
		bit 5: Autodetect programming 00 = Not supported 01 = Supported)	
		bit 6: RFU	
		bit 7: Multiple writes per line 00 = Not supported 01 = Supported)	
54h	0005h	Page size: 2 ⁿ bytes	32 bytes
55h	0005h	Erase suspend timeout maximum: 2 ⁿ (μs)	32μs
56h	0004h	Program suspend timeout maximum: 2 ⁿ (μs)	16μs
57h to 77h	FFFFh	Reserved	-
78h	0005h	^t PLRH maximum: 2 ⁿ (μs)	32μs
79h	0009h	^t VCCPH maximum: 2 ⁿ (μs) Power-on reset	512μs

Note: 1. The values in this table are valid for both packages.

Power-Up and Reset Characteristics

Table 24: Power-Up Specifications

Note 1 applies to entire table.

Parameter	Symbol		Min	Unit	Notes
	Legacy	JEDEC			
V _{CC} HIGH to V _{CCQ} HIGH	–	t _{VCHVCQH}	0	μs	2
V _{CC} HIGH to rising edge of RST#	t _{VCS}	t _{VCHPH}	300	μs	3, 4
V _{CCQ} HIGH to rising edge of RST#	t _{VIOS}	t _{VCQHPH}	0	μs	3, 4
RST# HIGH to chip enable LOW	t _{RH}	t _{PHEL}	50	ns	
RST# HIGH to write enable LOW	–	t _{PHWL}	150	ns	

- Notes:
1. Sampled only; not 100% tested.
 2. V_{CC} should attain V_{CC,min} from V_{SS} simultaneously with or prior to applying V_{CCQ} during power up. V_{CC} should attain V_{SS} during power down.
 3. If RST# is not stable for t_{VCS} or t_{VIOS}, the device will not allow any READ or WRITE operations, and a hardware reset is required.
 4. Power supply transitions should only occur when RST# is LOW.

Figure 14: Power-Up Timing

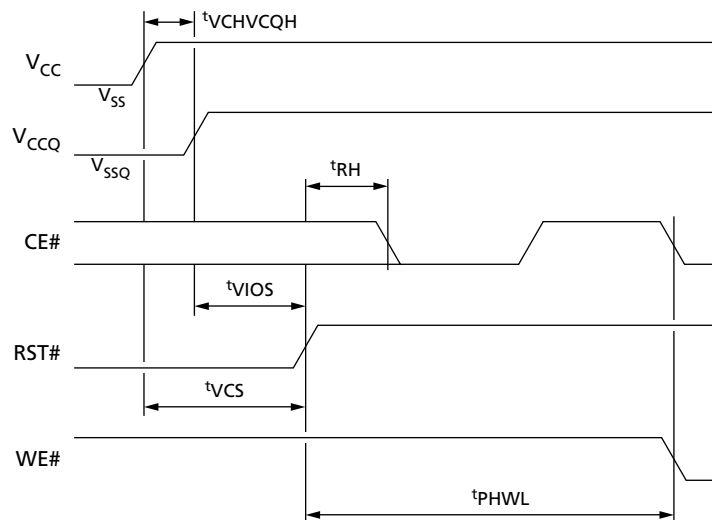


Table 25: Reset AC Specifications

Condition/Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
RST# LOW to read mode during program or erase	t_{READY}	t_{PLRH}	–	25	μs	1
RST# pulse width	t_{RP}	t_{PLPH}	100	–	ns	
RST# HIGH to CE# LOW, OE# LOW	t_{RH}	$t_{\text{PHEL}}, t_{\text{PHGL}}$	50	–	ns	1
RST# LOW to standby mode during read mode	t_{RPD}	–	0	–	μs	
RST# LOW to standby mode during program or erase			0	–	μs	
RY/BY# HIGH to CE# LOW, OE# LOW	t_{RB}	$t_{\text{RHEL}}, t_{\text{RHGL}}$	0	–	ns	1

Note: 1. Sampled only; not 100% tested.

Figure 15: Reset AC Timing – No PROGRAM/ERASE Operation in Progress

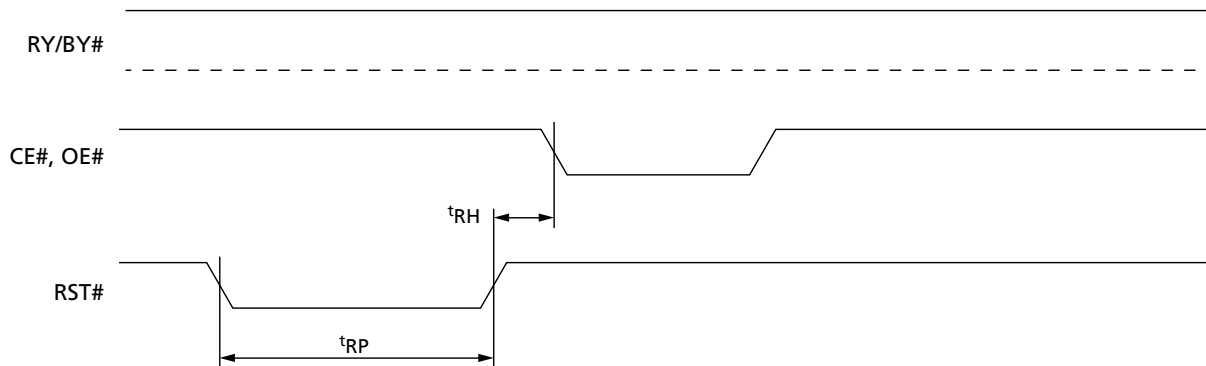
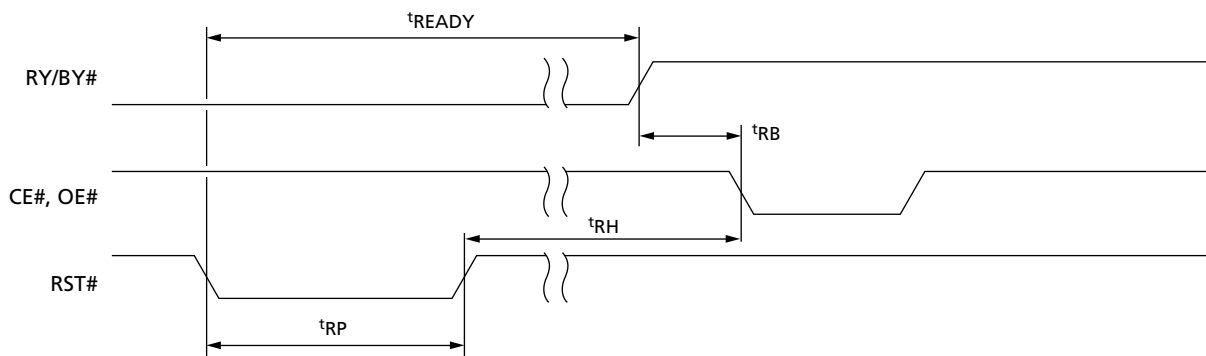


Figure 16: Reset AC Timing During PROGRAM/ERASE Operation



Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 26: Absolute Maximum/Minimum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Temperature under bias	T_{BIAS}	-50	125	°C	
Storage temperature	T_{STG}	-65	150	°C	
Supply voltage	V_{CC}	-0.6	$V_{CC} + 2$	V	1, 2
Input/output supply voltage	V_{CCQ}	-0.6	$V_{CCQ} + 2$	V	1, 2
Program/erase voltage	V_{PP}	-0.6	9.5	V	3

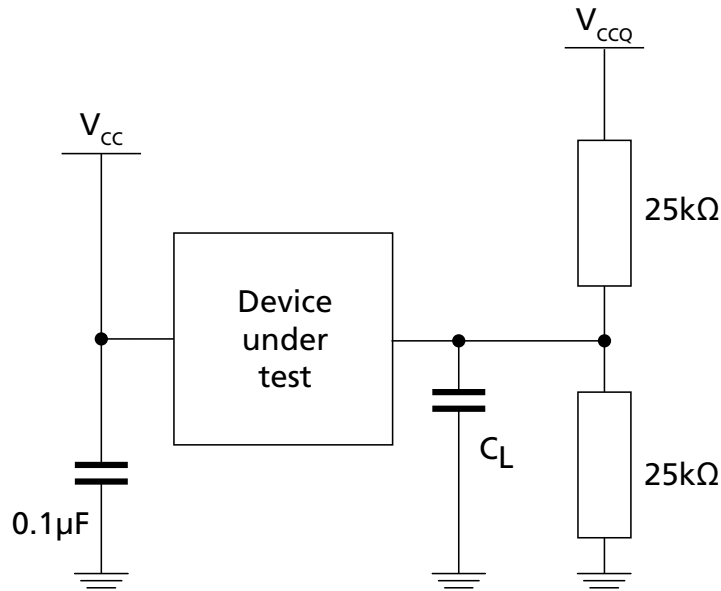
- Notes:
1. During signal transitions, minimum voltage may undershoot to $-2V$ for periods less than 20ns.
 2. During signal transitions, maximum voltage may overshoot to $V_{CC} + 2V$ for periods less than 20ns.
 3. V_{PP} must not remain at 9.5V for more than 80 hours cumulative.

Table 27: Operating Conditions

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	2.7	3.6	V	
Input/output supply voltage ($V_{CCQ} \leq V_{CC}$)	V_{CCQ}	1.65	3.6	V	
Accelerated buffered program/chip erase voltage	V_{HH}	8.5	9.5	V	
Ambient operating temperature	T_A	-40	105	°C	
Load capacitance	C_L	30		pF	
Input rise and fall times (V_{IL} to V_{IH})	-	0.3	2.5	ns	1, 2
Input pulse voltages	-	0 to V_{CCQ}		V	
Input and output timing reference voltages	-	$V_{CCQ}/2$		V	
Address to address skew	-	-	3	ns	

- Notes:
1. If the rise/fall time is slower than 2.5ns, all timing specs must be derated by 0.5ns for every nanosecond push-out in rise/fall time. (Example: for a 10ns rise/fall time, all timing specs must be derated by $(10 - 2.5) \times (0.5ns) = 3.75ns$.)
 2. Applies to Address, CE#, OE#, and WE# signals.

Figure 17: AC Measurement Load Circuit



Note: 1. C_L includes jig capacitance.

Figure 18: AC Measurement I/O Waveform

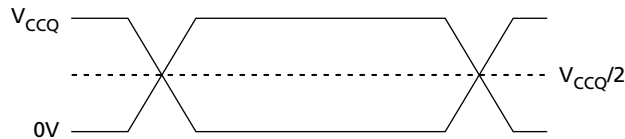


Table 28: Input/Output Capacitance

Parameter	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	3	11	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0V$	3	7	pF

DC Characteristics

Table 29: DC Current Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes	
Input load current	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$	-	-	± 1	μA	1	
Output leakage current	I_{LO}	$0V \leq V_{OUT} \leq V_{CC}$	-	-	± 1	μA		
V_{CC} read current	Random read	I_{CC1} $CE\# = V_{IL}, OE\# = V_{IH},$ $f = 5 \text{ MHz}$	-	26	31	mA		
	Page read		-	12	16	mA		
V_{CC} standby current	I_{CC2}	$CE\# = V_{CCQ} \pm 0.2V,$ $RST\# = V_{CCQ} \pm 0.2V$	-	70	200	μA		
V_{CC} automatic power saving (APS) current	$I_{CC \text{ APS}}$	$V_{CC} = V_{CC,max},$ $V_{CCQ} = V_{CCQ,max}$ $CE\# = V_{SSQ},$ $RST\# = V_{CCQ},$ All inputs are at V_{CCQ} or V_{SS}	-	-	2	mA		
V_{CC} program/erase/blank check current	I_{CC3}	Program/erase controller active	$V_{pp}/WP\# = V_{IL}$ or V_{IH}	-	35	50	mA	2
			$V_{pp}/WP\# = V_{HH}$	-	35	50	mA	
V_{pp} current	Read	I_{pp1}	$V_{pp}/WP\# \leq V_{CC}$	-	2	15	μA	
	Standby			I_{pp2}	-	0.2	5	
	PROGRAM operation ongoing	I_{pp3}	$V_{pp}/WP\# = V_{HH}$	-	5	10	mA	
			$V_{pp}/WP\# = V_{CC}$	-	0.05	0.10	mA	
	ERASE operation ongoing	I_{pp4}	$V_{pp}/WP\# = V_{HH}$	-	5	10	mA	
		$V_{pp}/WP\# = V_{CC}$	-	0.05	0.10	mA		

- Notes: 1. The maximum input load current is $\pm 5\mu A$ on the $V_{pp}/WP\#$ pin.
2. Sampled only; not 100% tested.

Table 30: DC Voltage Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Input LOW voltage	V_{IL}	$V_{CC} \geq 2.7V$	-0.5	-	0.8	V	
Input HIGH voltage	V_{IH}	$V_{CC} \geq 2.7V$	$0.7V_{CCQ}$	-	$V_{CCQ} + 0.4$	V	
Output LOW voltage	V_{OL}	$I_{OL} = 100\mu A,$ $V_{CC} = V_{CC,min},$ $V_{CCQ} = V_{CCQ,min}$	-	-	$0.15V_{CCQ}$	V	
Output HIGH voltage	V_{OH}	$I_{OH} = 100\mu A,$ $V_{CC} = V_{CC,min},$ $V_{CCQ} = V_{CCQ,min}$	$0.85V_{CCQ}$	-	-	V	
Voltage for $V_{pp}/WP\#$ program acceleration	V_{pp}	-	8.5	-	9.5	V	1
Program/erase lockout supply voltage	V_{LKO}	-	2.0	-	-	V	2, 3

- Notes:
1. V_{pp} must not remain at 9.5V for more than 80 hours cumulative.
 2. Sampled only; not 100% tested.
 3. WRITE operations are not valid when V_{CC} supply drops below V_{LKO} .



Read AC Characteristics

Table 31: Read AC Characteristics – $V_{CC} = V_{CCQ} = 2.7\text{--}3.6\text{V}$

Parameter	Symbol		Condition	Min	Max	Unit	Notes
	Legacy	JEDEC					
Address valid to next address valid	t_{RC}	t_{AVAV}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	105	–	ns	
Address valid to output valid	t_{ACC}	t_{AVQV}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	–	105	ns	
Address valid to output valid (page)	t_{PAGE}	t_{AVQV1}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	–	20	ns	
CE# LOW to output valid	t_{CE}	t_{ELQV}	$OE\# = V_{IL}$	–	105	ns	
OE# LOW to output valid	t_{OE}	t_{GLQV}	$CE\# = V_{IL}$	–	25	ns	
CE# HIGH to output High-Z	t_{HZ}	t_{EHQZ}	$OE\# = V_{IL}$	–	20	ns	1
OE# HIGH to output High-Z	t_{DF}	t_{GHQZ}	$CE\# = V_{IL}$	–	15	ns	1
CE# HIGH, OE# HIGH, or address transition to output transition	t_{OH}	t_{EHQX} , t_{GHQX} , t_{AXQX}	–	0	–	ns	

Note: 1. Sampled only; not 100% tested.

Table 32: Read AC Characteristics – $V_{CCQ} = 1.65\text{V--}V_{CC}$

Parameter	Symbol		Condition	Min	Max	Unit	Notes
	Legacy	JEDEC					
Address valid to next address valid	t_{RC}	t_{AVAV}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	110	–	ns	
Address valid to output valid	t_{ACC}	t_{AVQV}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	–	110	ns	
Address valid to output valid (page)	t_{PAGE}	t_{AVQV1}	$CE\# = V_{IL}$, $OE\# = V_{IL}$	–	25	ns	
CE# LOW to output valid	t_{CE}	t_{ELQV}	$OE\# = V_{IL}$	–	110	ns	
OE# LOW to output valid	t_{OE}	t_{GLQV}	$CE\# = V_{IL}$	–	25	ns	
CE# HIGH to output High-Z	t_{HZ}	t_{EHQZ}	$OE\# = V_{IL}$	–	20	ns	1
OE# HIGH to output High-Z	t_{DF}	t_{GHQZ}	$CE\# = V_{IL}$	–	15	ns	1
CE# HIGH, OE# HIGH, or address transition to output transition	t_{OH}	t_{EHQX} , t_{GHQX} , t_{AXQX}	–	0	–	ns	

Note: 1. Sampled only; not 100% tested.

Figure 19: Random Read AC Timing

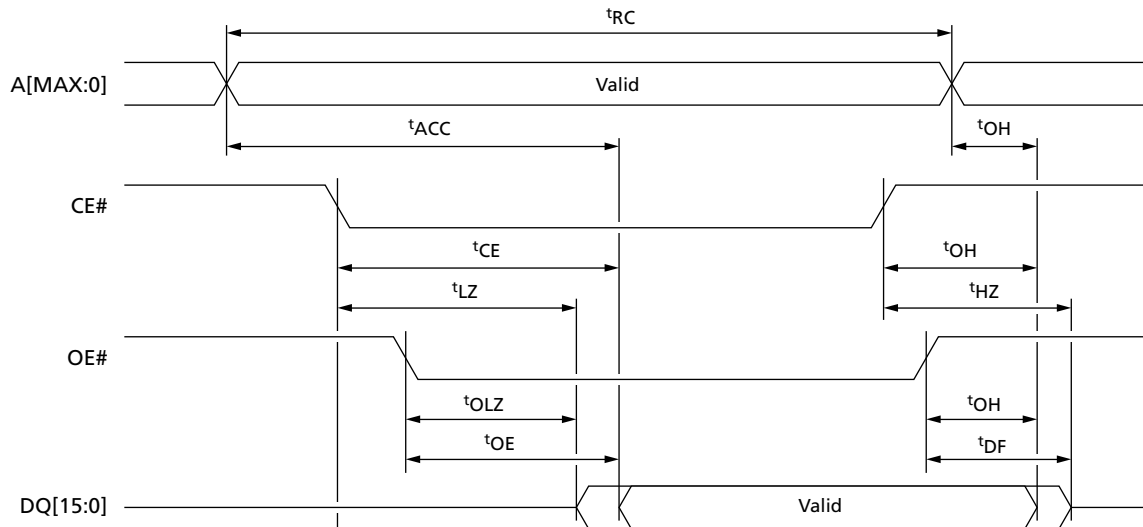
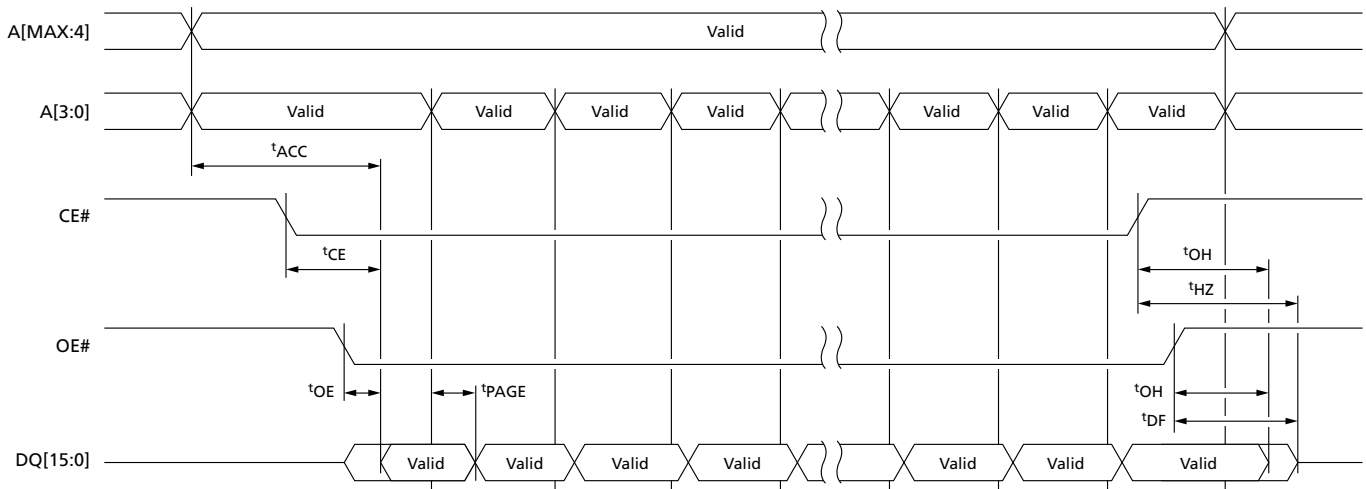


Figure 20: Page Read AC Timing



Note: 1. Page size is 16 words and is addressed by address inputs A[3:0].

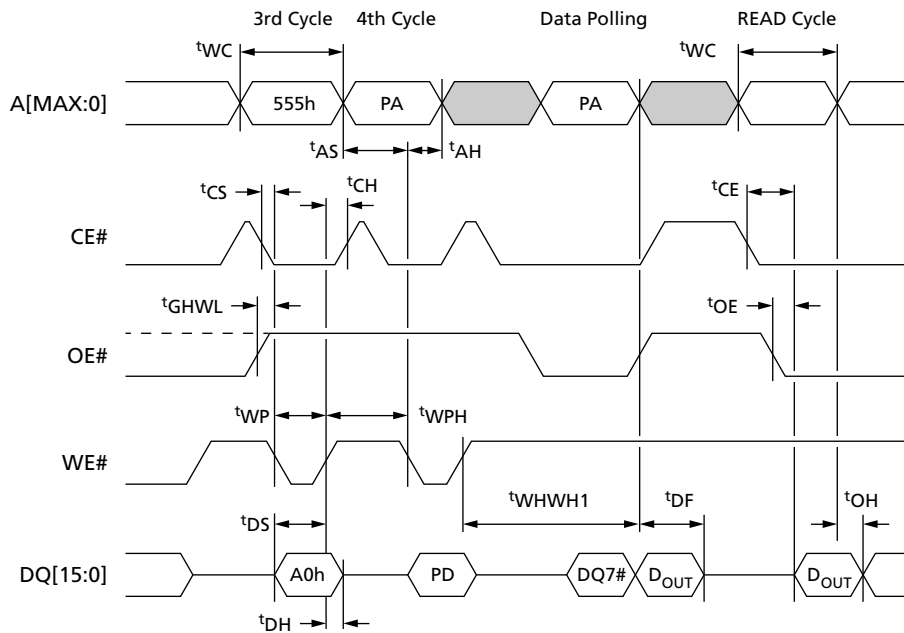
Write AC Characteristics

Table 33: WE#-Controlled Write AC Characteristics

Parameter	Symbol		Min	Typ	Max	Unit	Notes
	Legacy	JEDEC					
WRITE cycle time	t ^{WC}	–	60	–	–	ns	
CE# LOW to WE# LOW	t ^{CS}	t ^{ELWL}	0	–	–	ns	
WE# LOW to WE# HIGH	t ^{WP}	t ^{WLWH}	35	–	–	ns	
Input valid to WE# HIGH	t ^{DS}	t ^{DVWH}	30	–	–	ns	1
WE# HIGH to input transition	t ^{DH}	t ^{WHDX}	0	–	–	ns	
WE# HIGH to CE# HIGH	t ^{CH}	t ^{WHEH}	0	–	–	ns	
WE# HIGH to WE# LOW	t ^{WPH}	t ^{WHWL}	20	–	–	ns	
Address valid to WE# LOW	t ^{AS}	t ^{AVWL}	0	–	–	ns	
WE# LOW to address transition	t ^{AH}	t ^{WLAX}	45	–	–	ns	
OE# HIGH to WE# LOW	–	t ^{GHWL}	0	–	–	ns	
WE# HIGH to OE# LOW	t ^{OEH}	t ^{WHGL}	0	–	–	ns	
Program/erase valid to RY/BY# LOW	t ^{BUSY}	t ^{WHRL}	–	–	90	ns	2
WE# HIGH to OE# valid	–	t ^{WHQV}	t ^{AVQV} + 30	–	–	ns	
V _{HH} rise or fall time on V _{pp} /WP#	–	t ^{VHVPP}	250	–	–	ns	

- Notes:
1. The user's write timing must comply with this specification. Any violation of this write timing specification may result in permanent damage to the NOR Flash device.
 2. Sampled only; not 100% tested.

Figure 21: WE#-Controlled Program AC Timing



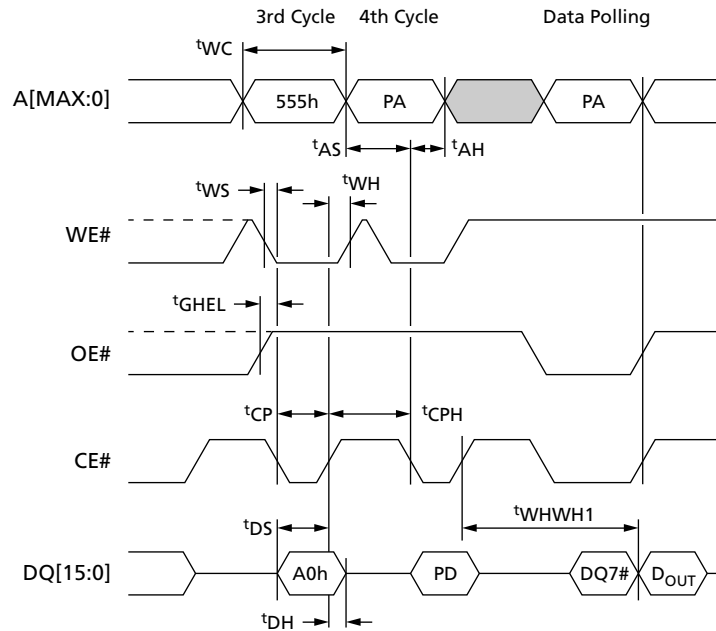
- Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
 2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
 3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
 4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.
 5. For t_{WHWH1} timing details, see the Program/Erase Characteristics table.

Table 34: CE#-Controlled Write AC Characteristics

Parameter	Symbol		Min	Typ	Max	Unit	Notes
	Legacy	JEDEC					
WRITE cycle time	t ^{WC}	–	60	–	–	ns	
WE# LOW to CE# LOW	t ^{WS}	t ^{WLEL}	0	–	–	ns	
CE# LOW to CE# HIGH	t ^{CP}	t ^{ELEH}	35	–	–	ns	
Input valid to CE# HIGH	t ^{DS}	t ^{DVEH}	30	–	–	ns	1
CE# HIGH to input transition	t ^{DH}	t ^{EHDX}	0	–	–	ns	
CE# HIGH to WE# HIGH	t ^{WH}	t ^{EHWH}	0	–	–	ns	
CE# HIGH to CE# LOW	t ^{CPH}	t ^{EHEL}	20	–	–	ns	
Address valid to CE# LOW	t ^{AS}	t ^{AVEL}	0	–	–	ns	
CE# LOW to address transition	t ^{AH}	t ^{ELAX}	45	–	–	ns	
OE# HIGH to CE# LOW	–	t ^{GHEL}	0	–	–	ns	
V _{HH} rise or fall time on V _{pp} /WP#	–	t ^{VHVPP}	250	–	–	ns	
Program/erase valid to RY/BY# LOW	t ^{BUSY}	t ^{WHRL}	–	–	90	ns	2
WE# HIGH to OE# valid	–	t ^{WHQV}	t ^{AVQV} + 30	–	–	ns	

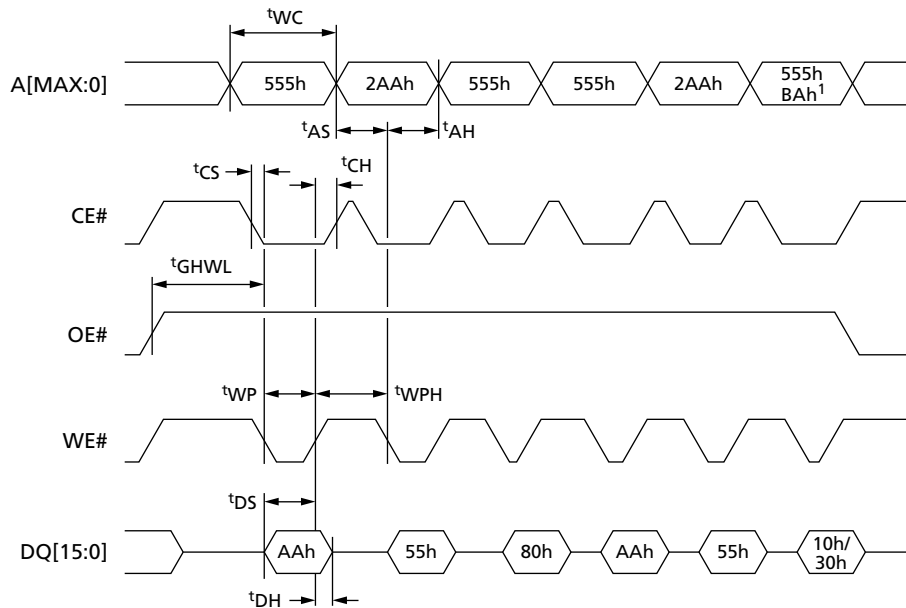
- Notes:
1. The user's write timing must comply with this specification. Any violation of this write timing specification may result in permanent damage to the NOR Flash device.
 2. Sampled only; not 100% tested.

Figure 22: CE#-Controlled Program AC Timing



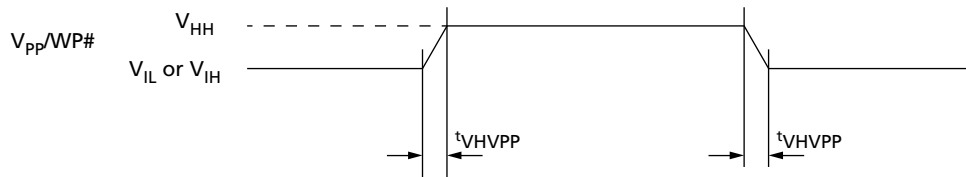
- Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
 2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
 3. DQ7 is the complement of the data bit being programmed to DQ7 (See Data Polling Bit [DQ7]).
 4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.
 5. For tWHWH1 timing details, see the Program/Erase Characteristics table.

Figure 23: Chip/Block Erase AC Timing



- Notes:
1. For a CHIP ERASE command, the address is 555h, and the data is 10h; for a BLOCK ERASE command, the address is BAd, and the data is 30h.
 2. BAd is the block address.
 3. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.
 4. For t_{WHWH1} timing details, see the Program/Erase Characteristics table.

Figure 24: Accelerated Program AC Timing



Data Polling/Toggle AC Characteristics

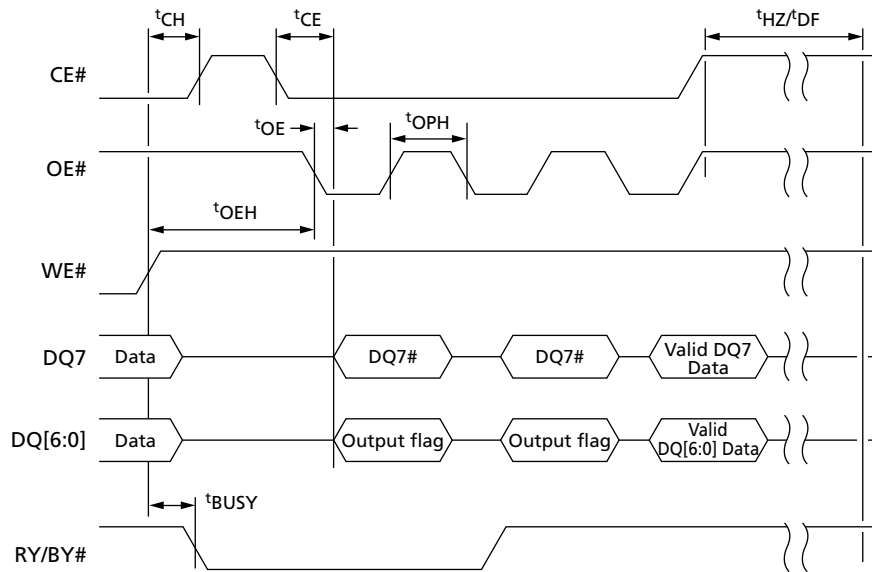
Table 35: Data Polling/Toggle AC Characteristics

Note 1 applies to entire table

Parameter	Symbol		Min	Max	Unit
	Legacy	JEDEC			
Address setup time to CE# or OE# LOW	t_{ASO}	t_{AXGL}	15	–	ns
Address hold time from OE# or CE# HIGH	t_{AHT}	t_{GHAX}, t_{EHAX}	0	–	ns
CE# HIGH time	t_{EPH}	t_{EHEL2}	20	–	ns
OE# HIGH time	t_{OPH}	t_{GHGL2}	20	–	ns
WE# HIGH to OE# LOW (toggle and data polling)	t_{OEH}	t_{WHGL2}	10	–	ns

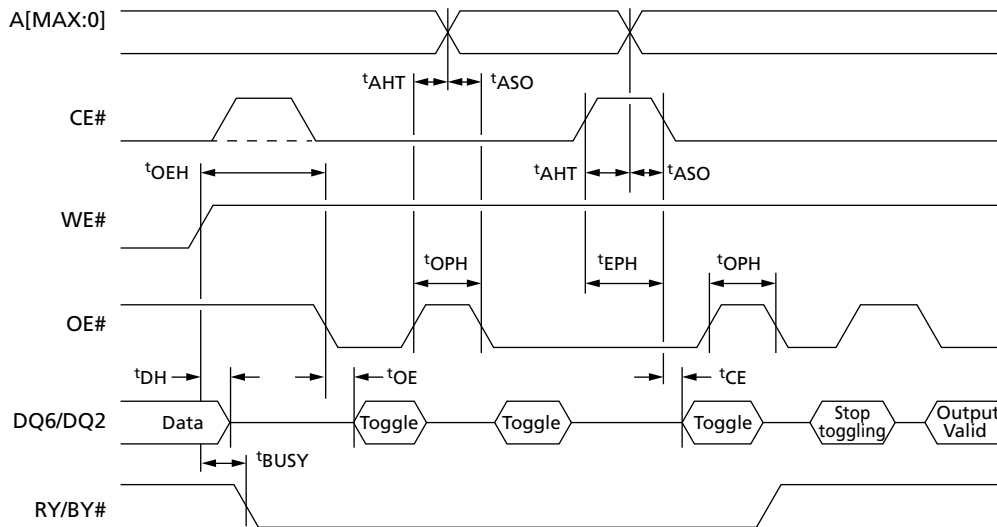
Note: 1. Sampled only; not 100% tested.

Figure 25: Data Polling AC Timing



- Notes:
1. DQ7 returns a valid data bit when the PROGRAM or ERASE command has completed.
 2. See the following tables for timing details: Read AC Characteristics and Data Polling/Toggle AC Characteristics.

Figure 26: Toggle/Alternative Toggle Bit Polling AC Timing



- Notes:
1. DQ6 stops toggling when the PROGRAM or ERASE command has completed. DQ2 stops toggling when the CHIP ERASE or BLOCK ERASE command has completed.
 2. See the following tables for timing details: Read AC Characteristics and Data Polling/Toggle AC Characteristics.



Program/Erase Characteristics

Table 36: Program/Erase Characteristics

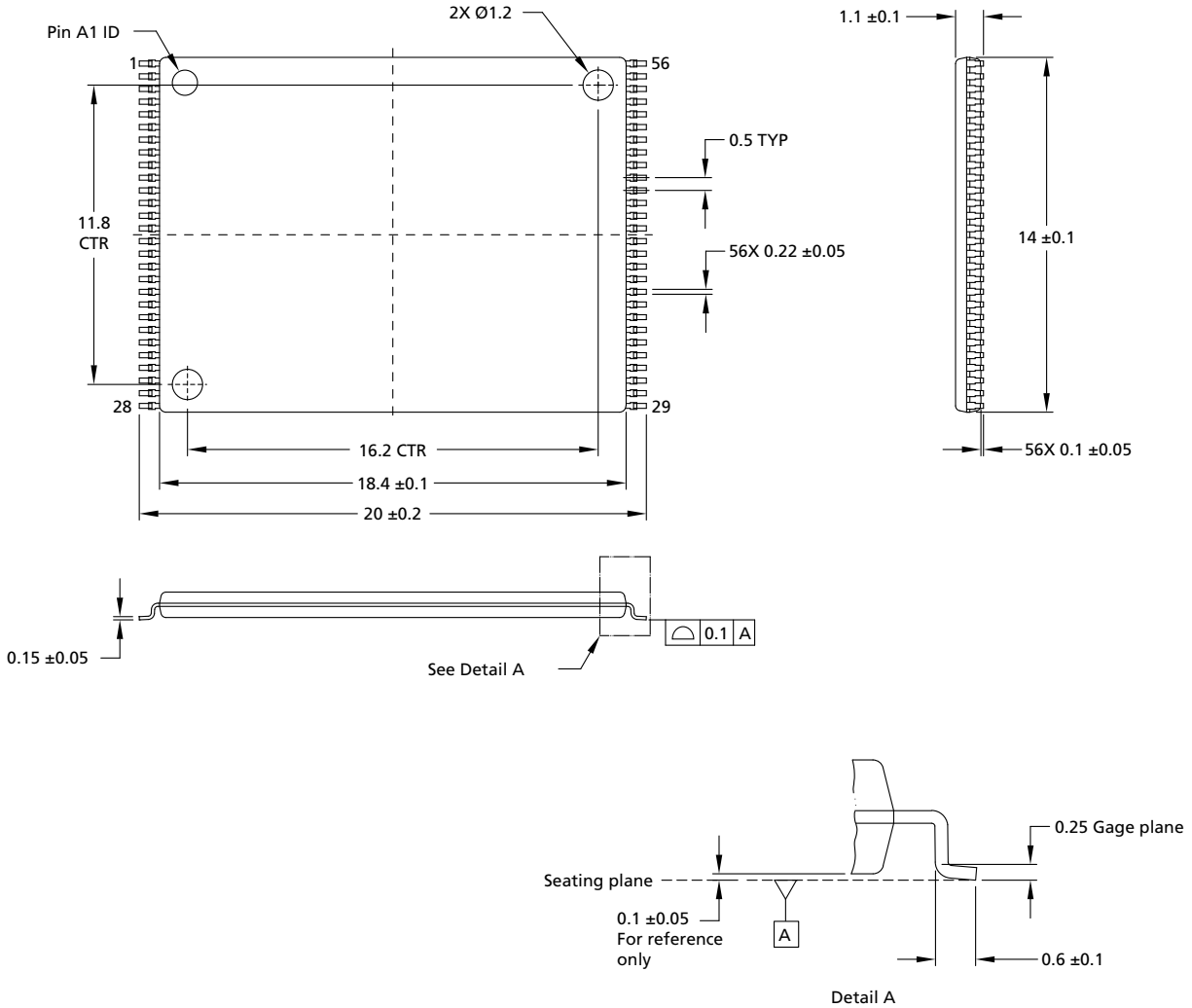
Notes 1 and 2 apply to entire table

Parameter	Buffer Size	Byte	Word	Min	Typ	Max	Unit	Notes
Erase								
Block erase (128KB)	–	–	–	–	2	1100	ms	–
Chip erase	–	–	–	–	104	–	s	–
Erase suspend latency time	–	–	–	–	–	20	µs	–
Erase or erase resume to suspend	–	–	–	–	100	–	µs	3, 4
Accelerated chip erase	–	–	–	–	95	–	s	–
Program								
Single-word program	–	–	–	–	25	200	µs	–
Buffer Program								
Word write to buffer program (^t WHWH1)	32	–	32	–	92	460	µs	–
	64	–	64	–	117	600	µs	–
	128	–	128	–	171	900	µs	–
	256	–	256	–	285	1500	µs	–
	512	–	512	–	512	2000	µs	–
Effective write to buffer program per word (^t WHWH1)	32	–	1	–	2.88	14.38	µs	–
	64	–	1	–	1.83	9.38	µs	–
	128	–	1	–	1.34	7.03	µs	–
	256	–	1	–	1.11	5.86	µs	–
	512	–	1	–	1.0	3.90	µs	–
Accelerated full buffer program time	–	–	–	–	410	–	µs	–
Program suspend latency time	–	–	–	–	–	15	µs	–
Nonvolatile protection								
Set nonvolatile protection bit time	–	–	–	–	25	320	µs	–
Clear nonvolatile protection bit time	–	–	–	–	80	1100	ms	–
Blank Check, CRC, and Program/Erase Endurance								
Blank check: main block	–	–	–	–	3.2	–	ms	–
CRC check time: main block	–	–	–	–	5	–	ms	–
CRC check time: full chip (512Mb)	–	–	–	–	5	–	s	–
PROGRAM/ERASE cycles (per block)	–	–	–	100,000	–	–	cycles	–

- Notes:
1. Typical values measured at room temperature and nominal voltages ($V_{CC} = 3V$).
 2. Typical and maximum values are sampled, but not 100% tested.
 3. Erase to suspend is the time between an initial BLOCK ERASE or ERASE RESUME command and a subsequent ERASE SUSPEND command.
 4. This typical value allows an ERASE operation to progress to completion—it is important to note that the algorithm might never finish if the ERASE operation is *always* suspended less than this specification.

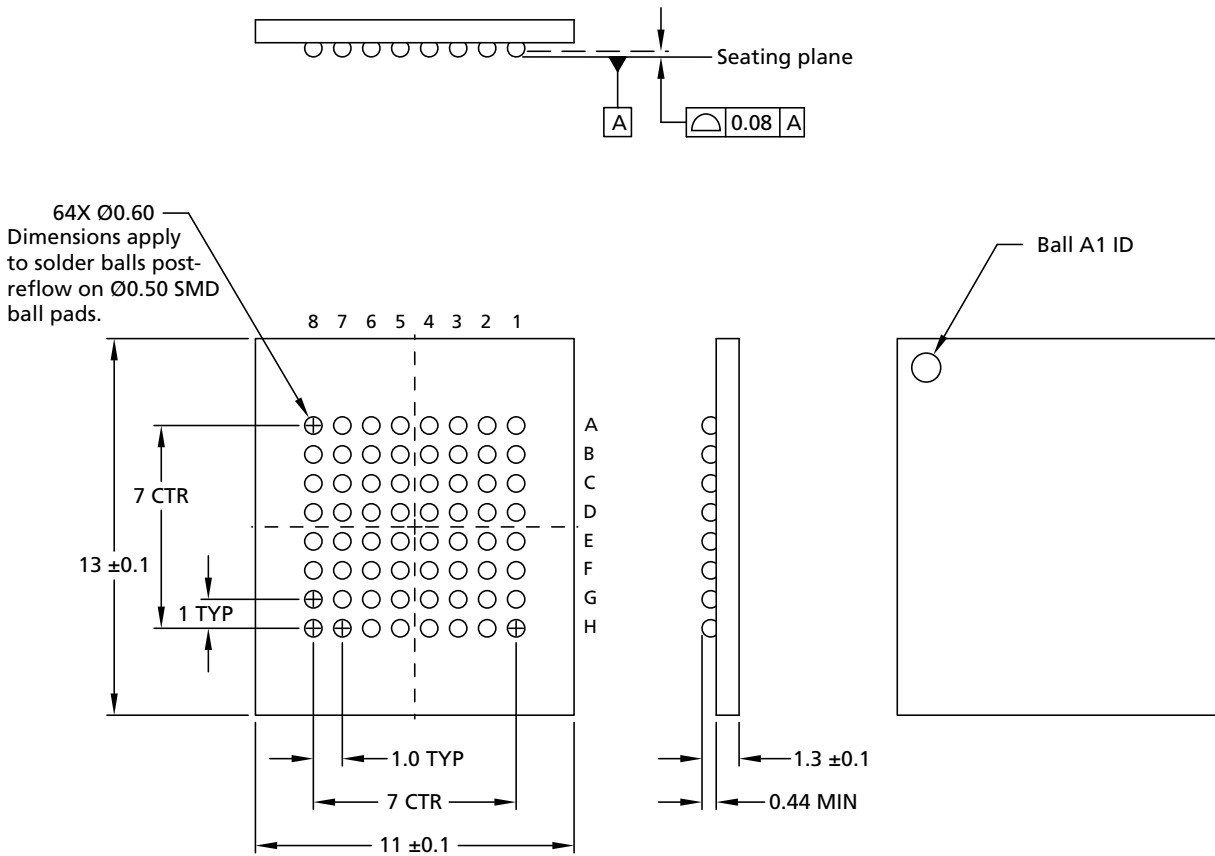
Package Dimensions

Figure 27: 56-Pin TSOP – 14mm x 20mm (Package Code: JS)



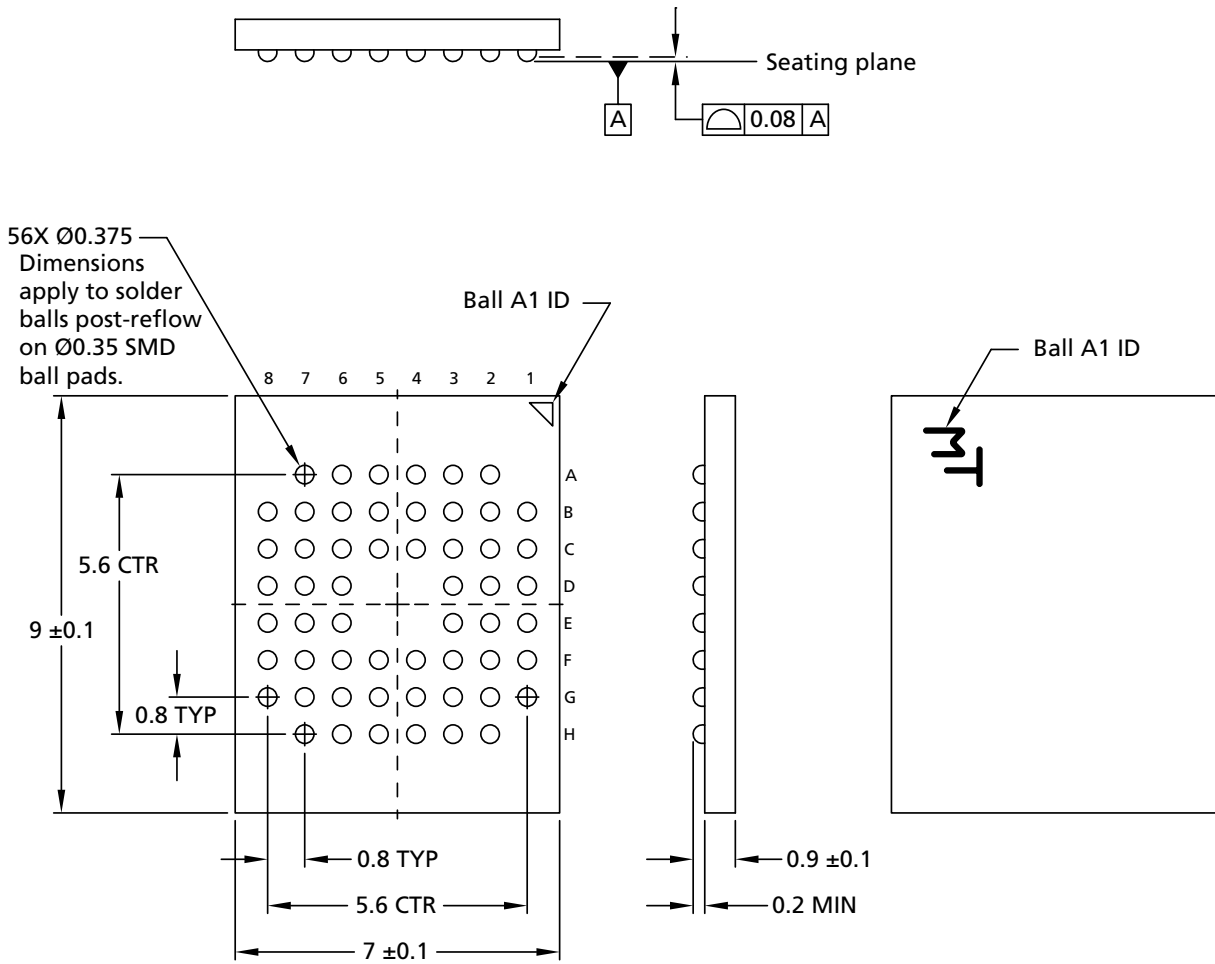
- Notes:
1. All dimensions are in millimeters.
 2. Pin A1 ID diameter is 1mm.
 3. New package assembly site has effected an ASE process change (original ASE process is Amkor). The package shows two eject pins on the package mark: one in the corner by pin 56 and one in the corner by pin 28, each with diameter 2mm x 1.2mm.
 4. Package width and length include mold flash.

Figure 28: 64-Ball LBGGA – 11mm x 13mm (Package Code: PC)



Note: 1. All dimensions are in millimeters.

Figure 29: 56-Ball VFBGA 7mm x 9mm (Package Code: PN)



Note: 1. All dimensions are in millimeters.

Revision History

Rev. F – 11/16

- Updated 56-pin dimension drawing
- Added Note 4 to 56-pin dimension drawing

Rev. E – 9/15

- Updated Table 31: Read AC Characteristics – t_{PAGE} in Read AC Characteristics

Rev. D – 01/15

- Promoted the document from Preliminary to Production status

Rev. C – 12/14

- Updated Figure 4: 64-Ball LPGA in Signal Assignments
- Updated Table 21: CFI Query System Interface Information in Common Flash Interface
- Updated Table 23: Primary Algorithm-Specific Extended Query Table in Common Flash Interface
- Updated Table 28: Input/Output Capacitance in Absolute Ratings and Operating Conditions
- Updated Table 31: Read AC Characteristics – $V_{CC} = V_{CCQ} = 2.7\text{-}3.6\text{V}$ in Read AC Characteristics
- Updated Table 32: Read AC Characteristics – $V_{CCQ} = 1.65\text{V}$ - V_{CC} in Read AC Characteristics
- Updated Table 36: Program/Erase Characteristics in Program/Erase Characteristics

Rev. B – 07/14

- Preliminary status

Rev. A – 05/14

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.