MP8758H

High-Current, 10A, 22V, Synchronous Step-Down Converter with Hiccup OCP, PFM/PWM Mode Selection, and Auto-Retry Thermal Shutdown

The Future of Analog IC Technology

DESCRIPTION

The MP8758H is a fully integrated, high-frequency, synchronous, rectified, step-down converter. It offers a very compact solution to achieve a 10A output current with excellent load and line regulation over a wide input supply range.

The MP8758H employs a constant-on-time (COT) control scheme, which provides fast transient response and eases loop stabilization. The COT control scheme provides a seamless transition into PFM mode at light-load operation, which boosts light-load efficiency.

An open-drain power good signal indicates that the output voltage is within its nominal voltage range.

Full protection features include over-current protection (OCP), over-voltage and under-voltage protection (OVP, UVP), and thermal shutdown.

The MP8758H requires a minimal number of readily available, external components and is available in a QFN-21 (3mmx4mm) package.

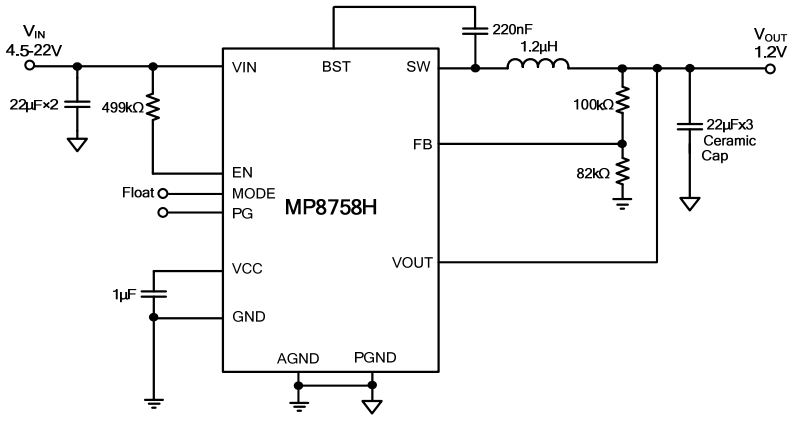
FEATURES

- Wide 4.5V to 22V Operating Input Range
- 10A Continuous Output Current
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction
- Internal Soft Start
- Output Discharge
- 500kHz Switching Frequency
- PFM/PWM Mode Selection
- Hiccup Mode, OCP, OVP, and UVP
- Auto-Retry Thermal Shutdown
- Output Adjustable from 0.604V

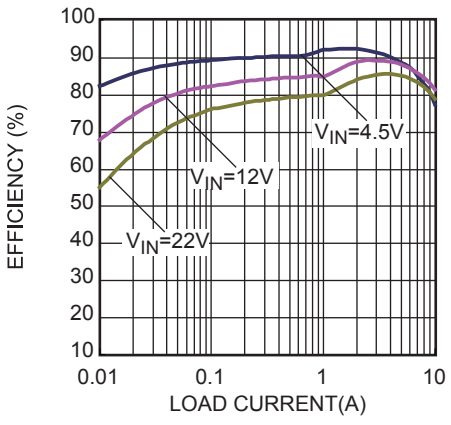
APPLICATIONS

- Set-Top Boxes and Multi-Function Printers
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency vs. Output Current



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8758HGL	QFN-21 (3mmx4mm)	*See Below*

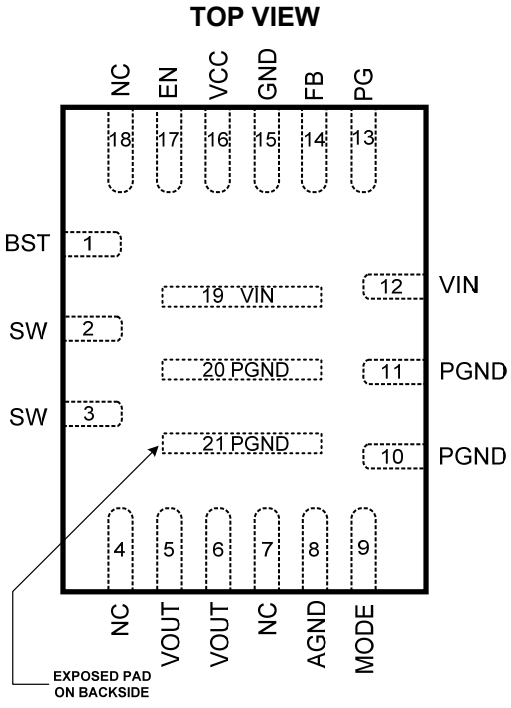
* For Tape & Reel, add suffix –Z (e.g. MP8758HGL–Z)

TOP MARKING

MPYW
8758
HLLL

MP: MPS prefix
Y: Year code
W: Week code
8758H: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-21 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 24V
V_{SW} .....-0.3V to 24.3V
V_{SW} (30ns).....-3V to 28V
V_{SW} (5ns).....-6V to 28V
V_{BST} ..... V_{SW} + 5.5V
V_{EN} 12V
Enable current (I_{EN}) (2)..... 2.5mA
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A=+25°C)(3)
QFN-21 (3mmx4mm). 2.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4.5V to 22V
Output voltage (V_{OUT}).....
0.604V to V_{IN}xD_{MAX} or 5.5V
Enable current (I_{EN})..... 1mA
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-21 (3mmx4mm).....50 ..... 12 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS MAX rating, please refer to the "EN Control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{SD}	V_{EN} = 0V		0	1	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V	160	190	220	μA
MOSFET						
High-side switch-on resistance	HS_{RDS-ON}	T_J = 25°C		25		mΩ
Low-side switch-on resistance	LS_{RDS-ON}	T_J = 25°C		9		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}		10	11	12	A
Switching Frequency and Minimum Off Time						
Switching frequency	F_{SW}		400	500	600	kHz
Minimum off time(6)	T_{OFF}		250	300	350	ns
Output Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP_OUT}		110	115	120	$\%V_{REF}$
OVP hysteresis				10		$\%V_{REF}$
OVP delay	T_{OVPDEL}			2.5		μs
UVP threshold	V_{UVP}		55	60	65	$\%V_{REF}$
UVP delay	T_{UVPDEL}			12		μs
Reference and Soft Start						
Reference voltage	V_{REF}		595	604	613	mV
Feedback current	I_{FB}	V_{FB} = 0.604V		10	50	nA
Soft-start time	T_{SS}	V_{OUT} from 10% to 90%		2.9		ms
Enable and UVLO						
Enable input low voltage	VIL_{EN}		1.15	1.25	1.35	V
Enable hysteresis	V_{EN-HYS}			100		mV
Enable input current	I_{EN}	V_{EN} = 2V		3		μA
		V_{EN} = 0V		0		
VCC under-voltage lockout threshold rising	VCC_{Vth}			4.2	4.35	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			400		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC regulator	V_{CC}		4.8	5.1	5.3	V
VCC load regulation		Icc = 8mA		2		%
Mode Selection						
Mode high level			VCC-0.4V			V
Mode low level					0.4V	V
Mode internal pull-up resistor				1		MΩ
Power Good						
FB rising (good)	PG_{Vth-Hi}			95		%V_{REF}
FB falling (fault)	PG_{Vth-Lo}			85		
FB rising (fault)	PG_{Vth-Hi}			115		
FB falling (good)	PG_{Vth-Lo}			105		
Power-good low to high delay	PG_{Td}			800		µs
Power-good sink-current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			1	µA
Thermal Protection						
Thermal shutdown(6)	T_{SD}			150		°C
Thermal shutdown hysteresis(6)				25		°C

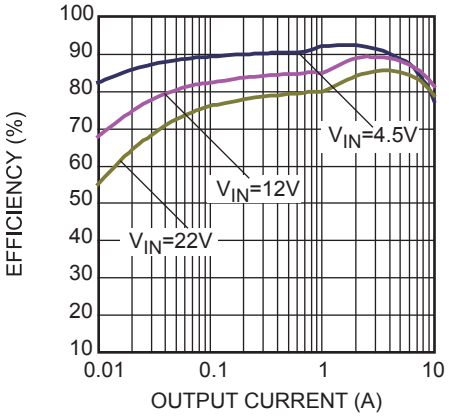
NOTE:

6) Guaranteed by design and engineering sample characterization.

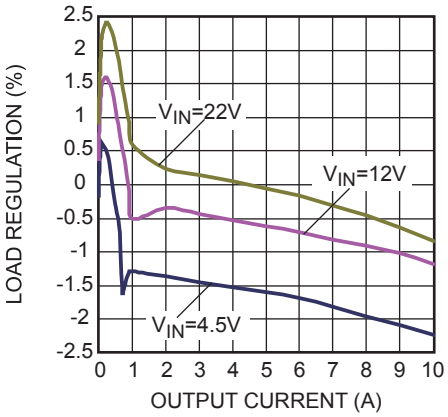
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.2µH, T_A = +25°C, unless otherwise noted.

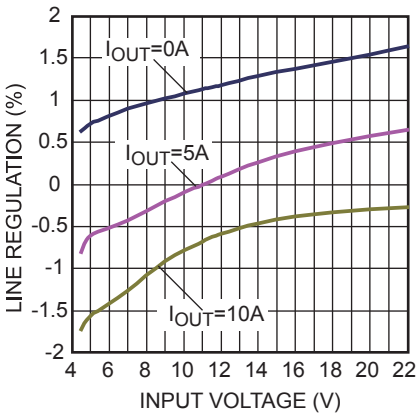
Efficiency vs. Output Current



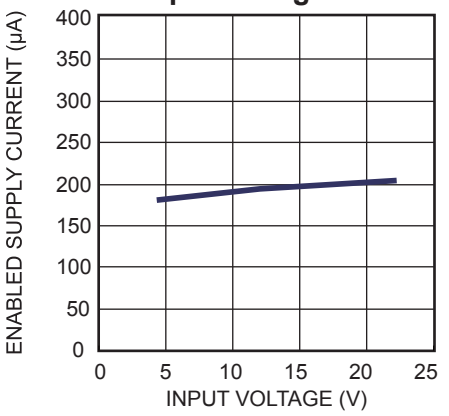
Load Regulation



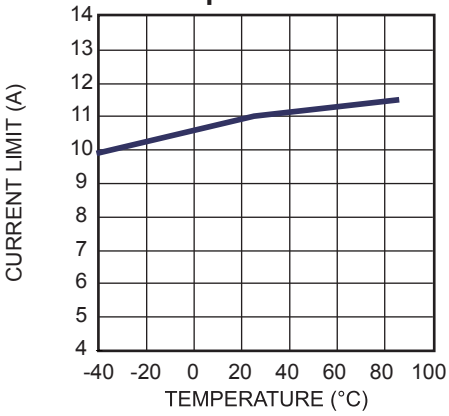
Line Regulation



Enabled Supply Current vs. Input Voltage



Valley Current Limit vs. Temperature

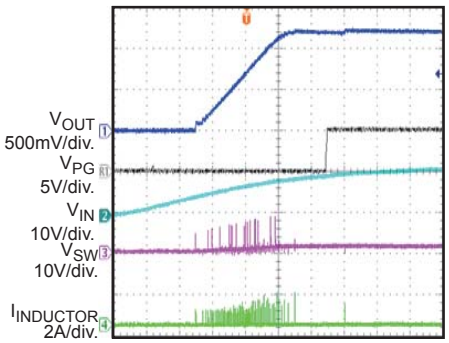


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.2µH, T_A = +25°C, unless otherwise noted.

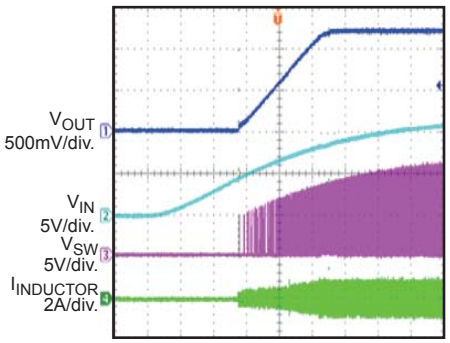
Start-Up through V_{IN}

I_{OUT}=0A, PFM



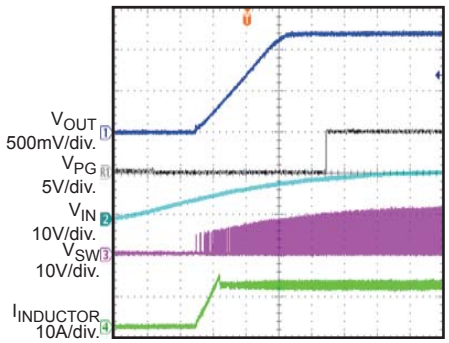
Start-Up through V_{IN}

I_{OUT}=0A, PWM



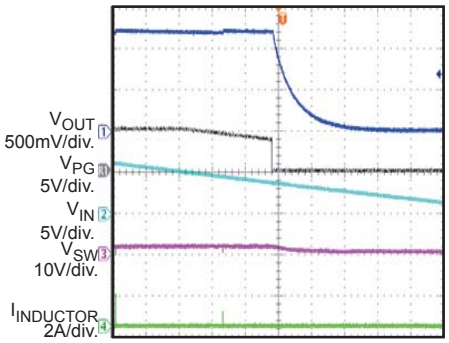
Start-Up through V_{IN}

I_{OUT}=10A



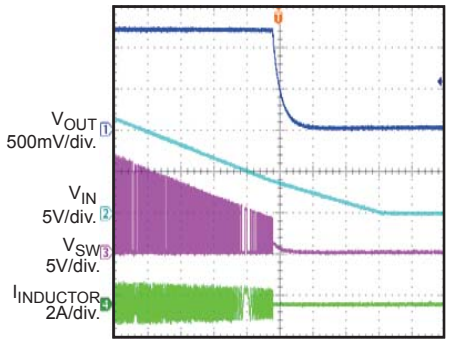
Shutdown through V_{IN}

I_{OUT}=0A, PFM



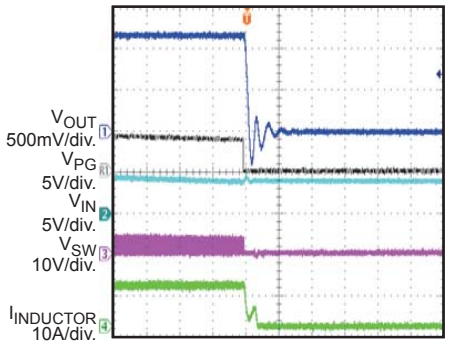
Shutdown through V_{IN}

I_{OUT}=0A, PWM



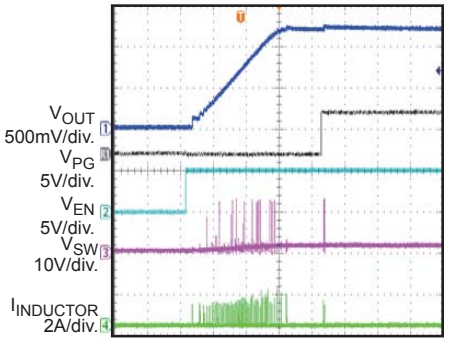
Shutdown through V_{IN}

I_{OUT}=10A



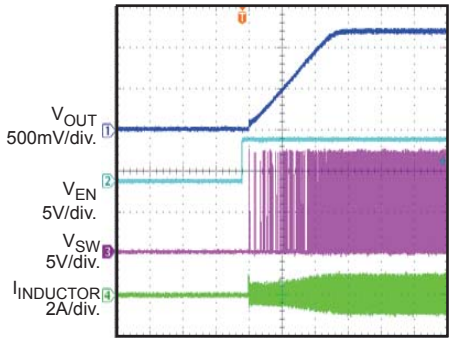
Start-Up through EN

I_{OUT}=0A, PFM



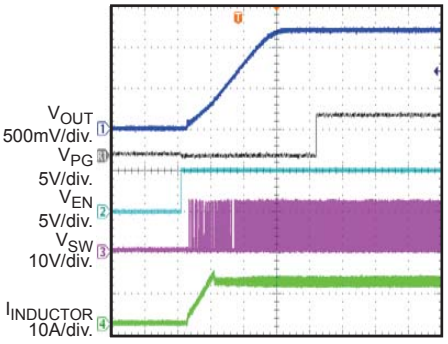
Start-Up through EN

I_{OUT}=0A, PWM



Start-Up through EN

I_{OUT}=10A

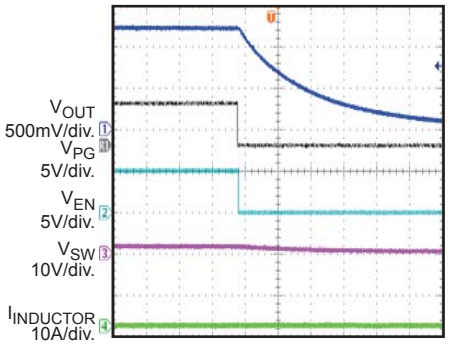


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.2µH, T_A = +25°C, unless otherwise noted.

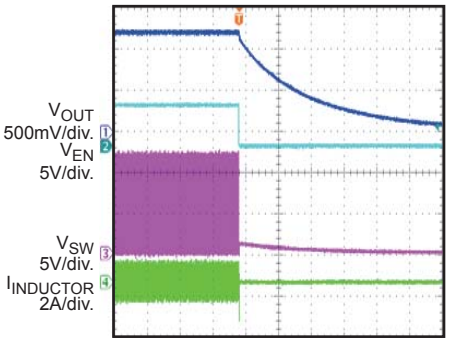
Shutdown through EN

I_{OUT}=0A, PFM



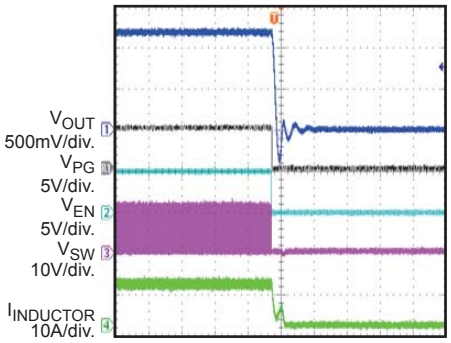
Shutdown through EN

I_{OUT}=0A, PWM



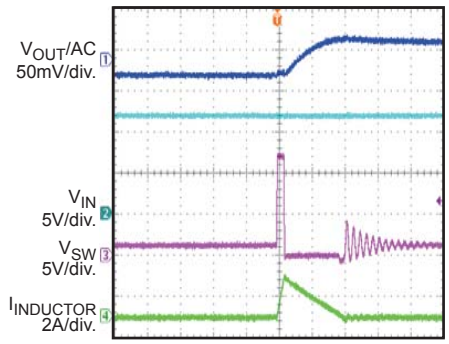
Shutdown through EN

I_{OUT}=10A



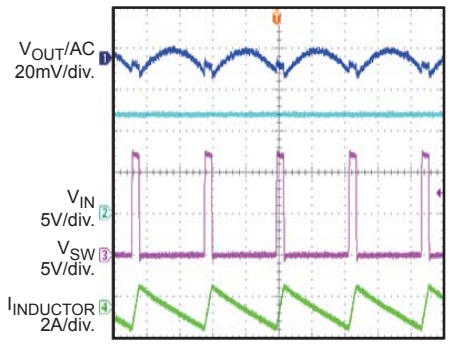
Output Voltage Ripple

I_{OUT}=0A, PFM



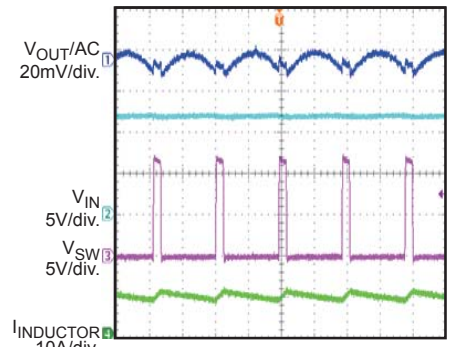
Output Voltage Ripple

I_{OUT}=0A, PWM



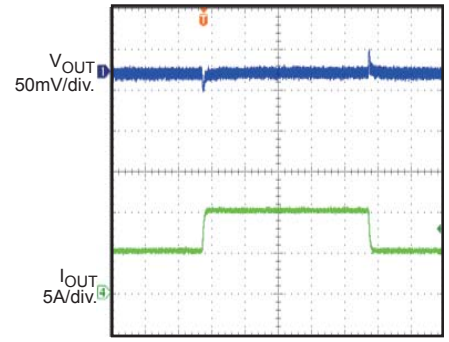
Output Voltage Ripple

I_{OUT}=10A



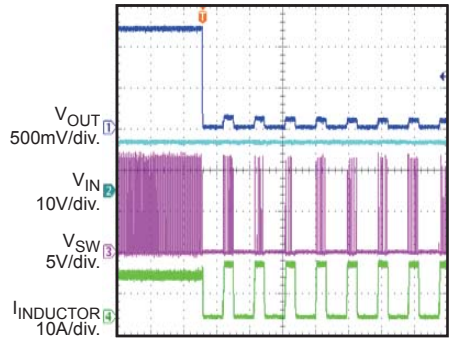
Load Transient Response

I_{OUT}=5A to 10A



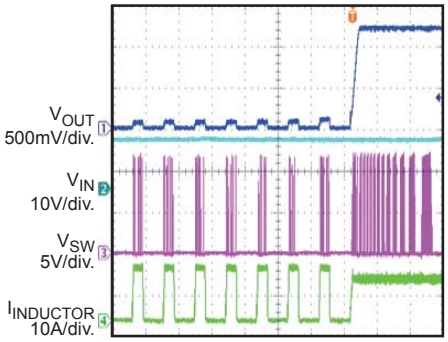
Short-Circuit Entry

I_{OUT}=10A



Short-Circuit Recovery

I_{OUT}=10A

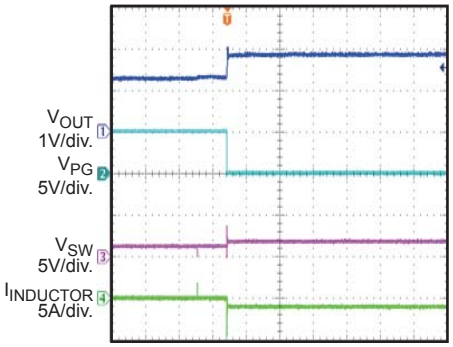


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1.2µH, T_A = +25°C, unless otherwise noted.

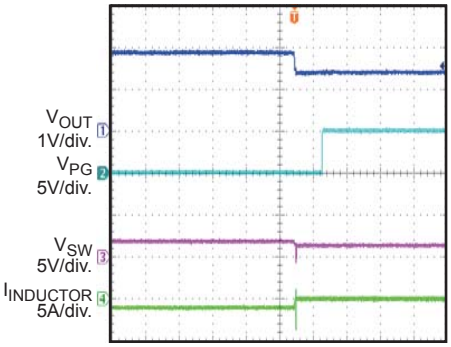
Output OVP Entry

I_{OUT}=0A, PFM



Output OVP Recovery

I_{OUT}=0A, PFM



PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
2, 3	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW negative during the off-time. The on resistance of the low-side switch and the internal diode fix the negative voltage. Use wide and short PCB traces to make the connection and try to minimize the area of the SW pattern.
4, 7, 18	NC	**Not connected.** Leave NC floating.
5, 6	VOUT	**Buck regulator output voltage sense.** Connect VOUT directly to the output capacitor of the regulator.
8	AGND	**Analog ground.** The internal reference is referred to AGND. Connect GND of the FB resistor divider to AGND for better load regulation.
9	MODE	**Mode selection.** Pull MODE high to set PFM mode. Pull MODE low to set forced PWM mode. MODE is pulled up internally. Floating MODE sets PFM mode.
10,11, Exposed Pad 20, 21	PGND	**Power ground.** Connect using wide PCB traces and multiple vias.
12, Exposed Pad 19	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulator. The MP8758H operates on a +4.5V to +22V input rail. An input capacitor is needed to decouple the input rail. Connect using wide PCB traces and multiple vias.
13	PG	**Power good output.** The output of PG is an open-drain signal and is low if the output voltage is out of the regulation window.
14	FB	**Feedback.** An external resistor divider from the output to GND (tapped to FB) sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces.
15	GND	**Ground.** GND must be connected to either PGND or AGND for normal operation.
16	VCC	**Internal 5V LDO output.** The driver and control circuits are powered from VCC. Decouple with a minimum 1μF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended because of their stable temperature characteristics.
17	EN	**Enable.** EN is a digital input, which is used to enable or disable the regulators. When EN=1, the regulator output turns on; when EN=0, the regulator turns off.

FUNCTIONAL BLOCK DIAGRAM

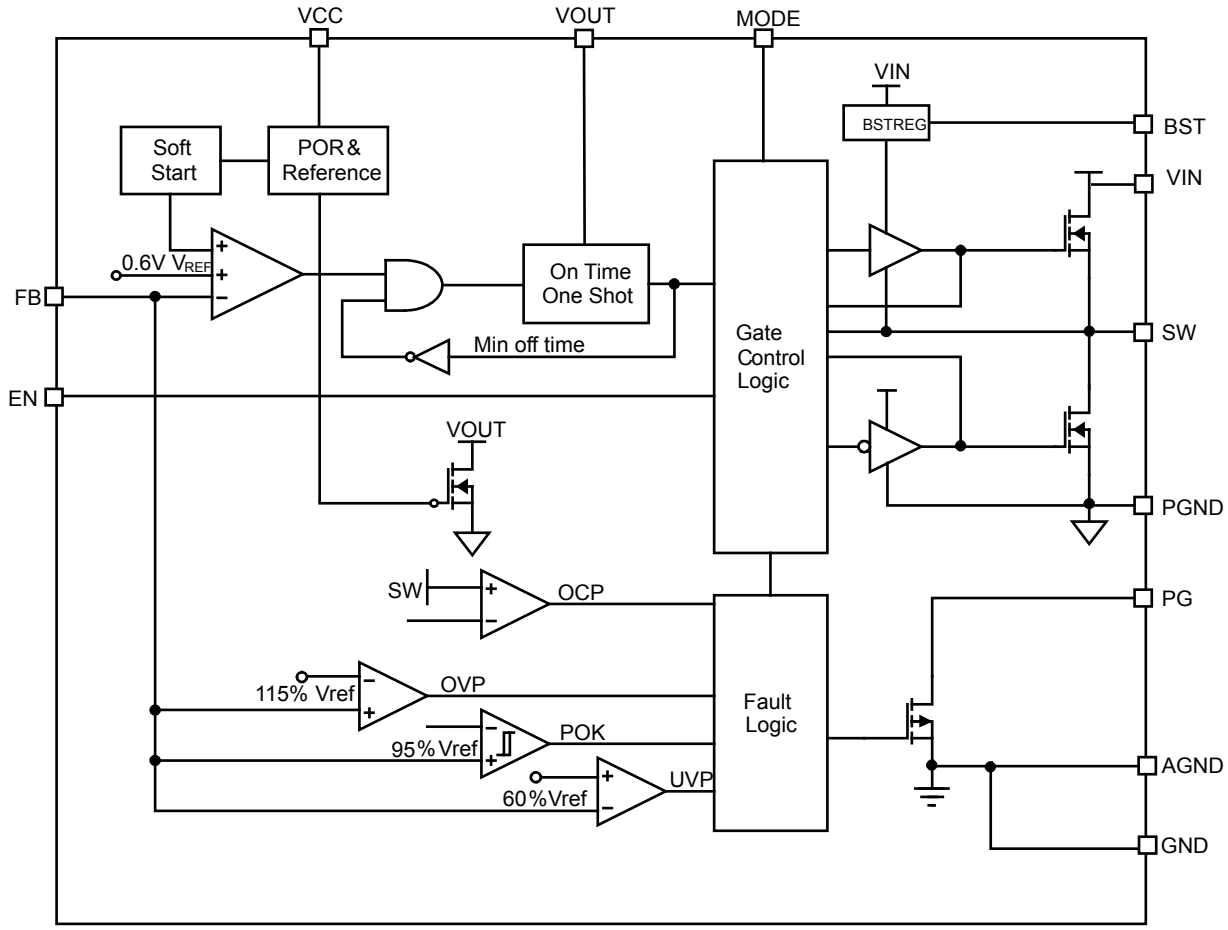


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP8758H is a fully integrated, synchronous, rectified, step-down, switch-mode converter that employs a constant-on-time (COT) control scheme to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) falls below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by both the output and input voltages to make the switching frequency constant over the input voltage range.

After the on period elapses, the HS-FET turns off off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize the conduction loss. There will be a dead short between the input and GND if both the HS-FET and the LS-FET are turned on at the same time. This is called a shoot-through. In order to avoid a shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on time period or the LS-FET off and the HS-FET on time period.

Internal compensation is applied for COT control to ensure more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

MODE Selection

The MP8758H has MODE selection. When MODE is pulled high, the part works in PFM mode. When MODE is pulled low, the part works in forced PWM mode. MODE is pulled up internally. Floating MODE sets PFM mode.

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps. CCM (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by a one-shot on-timer. The one-shot timer is controlled by the input and output voltages, so that the switching frequency can be fairly fixed at 500kHz for different input and output conditions. When the HS-FET is turned off, the LS-FET turns on until the next period.

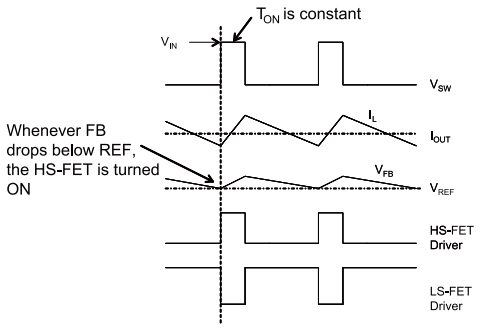


Figure 2: Heavy-Load Operation

PWM mode occurs in CCM operation, where the switching frequency is fairly constant.

Light-Load Operation

Forced PWM Mode Operation

The MP8758H enters continuous conduction mode (CCM) when working in forced PWM mode. In this mode, the HS-FET and the LS-FET repeat the on/off operation, even if the inductor current drops to zero or a negative value. The switching frequency (F_{SW}) is fairly constant.

PFM Mode Operation

The inductor current decreases as the load decreases. Once the inductor current reaches zero, the operation transitions from continuous conduction mode (CCM) to discontinuous conduction mode (DCM).

When the MP8758H works in PFM mode during light-load operation, the switching frequency is reduced automatically to maintain high efficiency (see Figure 3). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero.

In PFM operation, V_{FB} does not reach V_{REF} when the inductor current approaches zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. As a result, the efficiency at a light-load condition is improved greatly. At a light-load condition, the HS-FET is not turned on as often as it is at a heavy load condition. This is called skip mode.

At a light-load or no-load condition, the output drops very slowly until the MP8758H reduces the switching frequency, achieving high efficiency at light load.

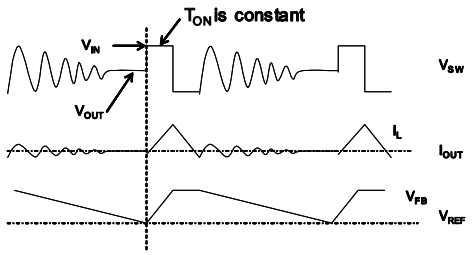


Figure 3: Light-Load Operation

As the output current increases from the light-load condition, the time period within the current modulator becomes shorter. The HS-FET turns on more frequently and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current is determined by Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

PWM mode begins once the output current exceeds the critical level. The switching frequency then stays fairly constant over the output current range.

Jitter and FB Ramp Slope

Jitter occurs in both PWM and skip mode when noise on the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 4 and Figure 5). Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, the V_{FB} ripple does not directly affect noise immunity.

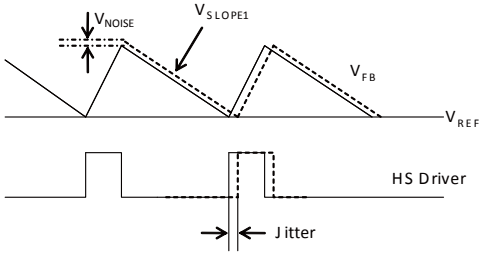


Figure 4: Jitter in PWM Mode

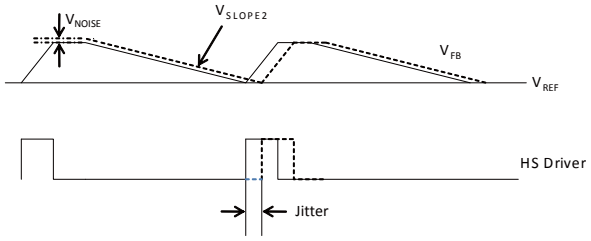


Figure 5: Jitter in Skip Mode

Operating without External Ramp Compensation

The traditional constant-on-time control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to act as an effective current sense resistor. Usually, ceramic capacitors cannot be used as output capacitors.

To determine the stability, calculate the ESR value with Equation (2):

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (2)$$

Where T_{SW} is the switching period.

The MP8758H has a built-in internal ramp compensator to ensure that the system is stable, even without the help of the output capacitor's ESR. Use a ceramic capacitor to significantly reduce the output ripple, total BOM cost, and board area.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. Please refer to the Application Information section on page 17 for design steps without external compensation.

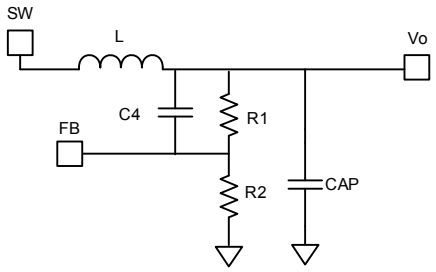


Figure 6: Simplified Circuit in PWM Mode without External Ramp Compensation

When using a large ESR capacitor on the output, add a ceramic capacitor with a value of 10µF or less in parallel to minimize the effect of the ESL.

Operating with External Ramp Compensation

Usually, the MP8758H is able to support ceramic output capacitors without an external ramp. In some cases, the internal ramp may not be enough to stabilize the system, and external ramp compensation is needed. Please refer to the Application Information section on page 17 for design steps with external ramp compensation.

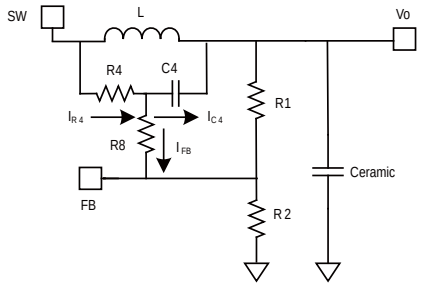


Figure 7: Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows a simplified external ramp compensation (R4 and C4) for PWM mode. Chose R1, R2, R8, and C4 of the external ramp to meet the condition shown in Equation (3) and Equation (4):

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} + R_8 \right) \quad (3)$$

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (4)$$

V_{RAMP} on V_{FB} can then be estimated with Equation (5):

$$V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R_4 \times C_4} \times T_{ON} \times \frac{R_1 // R_2}{R_1 // R_2 + R_8} \quad (5)$$

The downward slope of the V_{FB} ripple can be estimated with Equation (6):

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (6)$$

If there is instability in PWM mode, either R4 or C4 can be reduced. If C4 cannot be reduced further due to limitation from Equation (3), then only R4 can be reduced. For stable PWM operation, estimate V_{slope1} with Equation (7):

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} C_{OUT}}{2 \times L \times C_{OUT}} V_{OUT} + \frac{Io \times 10^{-3}}{T_{SW} - T_{on}} \quad (7)$$

Where Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is the same whether the external ramp is used or not. Figure 8 shows the simplified circuit in skip mode when both the HS-FET and the LS-FET are off.

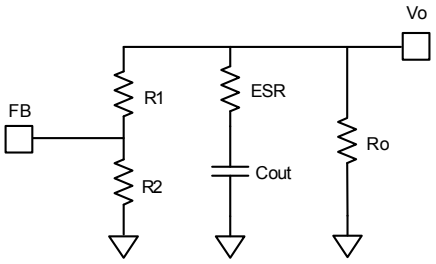


Figure 8: Simplified Circuit in Skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined with Equation (8):

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1 + R_2) // Ro) \times C_{OUT}} \quad (8)$$

Where Ro is the equivalent load resistor.

As described in Figure 5, V_{SLOPE2} in skip mode is lower than it is in PWM mode, and the jitter is larger as well. For a system with less jitter during a light-load condition, the values of the V_{FB} resistors should not be too large. However, this will decrease the light-load efficiency.

EN Control

The regulator turns on when EN is high and turns off when EN is low.

For automatic start-up, pull EN up to the input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) to determine the automatic start-up voltage using Equation (9):

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} (V) \quad (9)$$

For example, if R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, then $V_{IN-START}$ is 4.93V.

A 10nF ceramic capacitor from EN to GND is recommended to avoid noise.

There is an internal Zener diode on EN, which clamps the EN voltage to prevent runaway. EN is clamped internally using a 12V Zener diode, which limits the pull-up current to a maximum of 1mA.

When EN is driven by an external logic signal, the EN voltage should be lower than 12V. When EN is connected to VIN through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure that the maximum pull-up current less than 1mA.

If a resistive voltage divider is being used and VIN is higher than 12V, calculate the allowed minimum pull-up resistor (R_{UP}) with Equation (10):

$$\frac{V_{IN}(V)-12}{R_{UP}(k\Omega)}-\frac{12}{R_{DOWN}(k\Omega)}<1(mA) \quad (10)$$

If only the pull-up resistor (R_{UP}) is being used and the pull-down resistor is not connected, $V_{IN\text{-}START}$ is determined by the UVLO input. Calculate the minimum resistor value with Equation (11):

$$R_{UP}(k\Omega)>\frac{V_{IN}(V)-12}{1(mA)} \quad (11)$$

A typical pull-up resistor is 499kΩ.

Soft Start (SS)

The MP8758H employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN pulls high, both the internal reference voltage and the output voltage ramp up gradually. Once the reference voltage reaches its target value, the soft start finishes and the MP8758H enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high- and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Power Good (PG)

The MP8758H uses a power good (PG) output to indicate whether the output voltage of the regulator is ready. PG is the open drain of the MOSFET. Connect PG to VCC or another voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on, and PG is pulled to GND before SS is ready. When the soft start finishes and the FB voltage is higher than 95% and lower than 105% of the internal reference voltage, PG is pulled high after a short delay of 0.8ms.

When the FB voltage is lower than 85% and higher than 115% of the internal reference voltage, PG is pulled low.

Over-Current Protection and Hiccup Mode

The MP8758H has a cycle-by-cycle, over-current limit. The current limit circuit employs a "valley" current-sensing algorithm. The $R_{DS(ON)}$ of the LS-FET is used as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the control logic is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND and SW. Since GND is used as the positive current sensing node, GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the HS-FET off and the LS-FET on state, the OC trip level sets the valley level of the inductor current. Calculate the load current at the over-current threshold (I_{OC}) with Equation (12):

$$I_{OC}=I\_limit+\frac{\Delta I_{inductor}}{2} \quad (12)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor, and the output voltage falls off. The output voltage drops until V_{FB} is below the under-voltage (UV) threshold, typically 60% below the reference. Once UV is triggered, the MP8758H enters hiccup mode to restart the part periodically. The chip disables the output power stage, discharges the soft-start capacitor, and tries to soft start again automatically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed. The MP8758H then exits hiccup mode and the output rises back to regulation level.

Over- and Under-Voltage Protection (OVP/UVP)

The MP8758H monitors a resistor divided feedback voltage to detect over- and under-voltage. When the feedback voltage rises higher than 115% of the target voltage, the controller enters OVP. During this period, the LS-FET is forced on with a negative current limit of -1A,

discharges the output, and tries to keep it within the normal range. The part exits OVP when FB falls below 105% of the target voltage.

If OTP occurs during OVP, the LS-FET turns off and stops discharging the output until the silicon temperature falls below 125°C.

When the feedback voltage falls below 60% of the target voltage, the UVP comparator output goes high. If the UV still occurs after a 12μs delay, then hiccup mode is triggered.

Under-Voltage Lockout (UVLO)

The MP8758H has under-voltage lockout protection (UVLO). When VCC is higher than UVLO's rising threshold voltage, the part powers up, and shuts off when VCC falls below the UVLO falling threshold voltage. This is called non-latch protection. If an application requires a higher UVLO, use two external resistors on EN to adjust the input voltage UVLO (see Figure 9). It is recommended to use the EN resistors to set the UVLO falling threshold (V_{STOP}) above 4.2V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations.

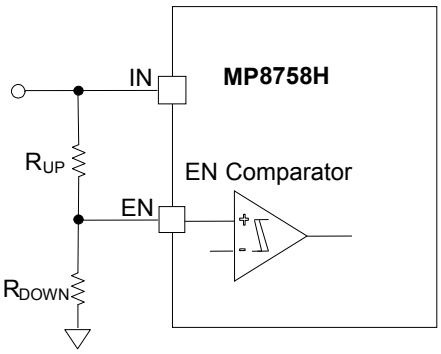


Figure 9: Adjustable UVLO

Thermal Shutdown

The MP8758H has thermal shutdown protection. The junction temperature of the IC is monitored internally. The converter shuts off if the junction temperature exceeds the threshold value, typically 150ºC. This is called non-latch protection. Hysteresis is about 25ºC. Once the junction temperature drops to about 125ºC, a soft start is initiated.

Output Discharge

The MP8758H discharges the output when EN is low, or when the controller is turned off by the protection functions (UVLO and thermal shutdown). The part uses an internal 6Ω MOSFET to discharge the output.

APPLICATION INFORMATION

Setting the Output Voltage without External Compensation

The MP8758H can support different types of output capacitors, including POSCAP, electrolytic capacitors, and ceramic capacitors without external ramp compensation. The output voltage is then set by feedback resistors R1 and R2 (see Figure 10).

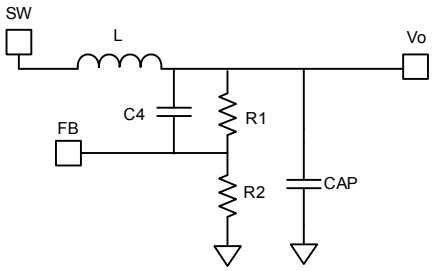


Figure 10: Simplified Circuit of POS Capacitor

First, carefully choose a value for R2, as a small value for R2 will lead to considerable quiescent current loss, while too large a value for R2 will make the FB noise sensitive. Set the current through R2 around 5-10μA for good balance, system stability, and no load loss. Considering the output ripple, calculate R1 with Equation (13):

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (13)$$

Where ΔV_{OUT} is the output ripple.

In addition to feedback resistors, a feed-forward capacitor (C4) is usually applied for better transient performance. When using ceramic capacitors, a capacitor value around 100pF-1nF is suggested for better transient response while also keeping the system stable with noise immunity. If the system is noise sensitive because of the zero induced by this capacitor, add a resistor (R8) between the capacitor and FB to form a pole. This resistor can be set according to Equation (16) on page 18.

Setting the Output Voltage with External Compensation

If the system is not stable enough when the low ESR ceramic capacitor is used on the output, add an external voltage ramp to FB through resistor R4 and capacitor C4.

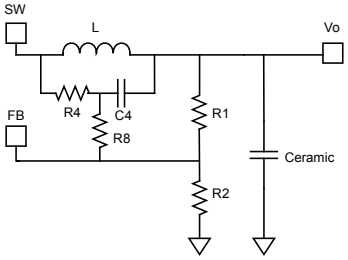


Figure 11: Simplified Circuit of Ceramic Capacitor

The output voltage is influenced by V_{RAMP} beside the R divider (see Figure 11). V_{RAMP} can be calculated with Equation (5) on page 14. R2 should be chosen carefully, as a small value for R2 will lead to considerable quiescent current loss while too large a value for R2 will make the FB noise sensitive. Use a comparatively larger R2 when Vo is low (e.g. 1.05V), and a smaller R2 when Vo is high. The value of R1 can then be calculated with Equation (14):

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT}-V_{FB(AVG)})} - \frac{R_2}{R_4+R_8}} \quad (14)$$

$V_{FB(AVG)}$ is the average value on FB. $V_{FB(AVG)}$ varies with V_{IN}, V_{OUT}, and load condition. Since the value in skip mode is lower than in PWM mode, the load and line regulations are strictly related to $V_{FB(AVG)}$. If a better load or line regulation is needed, use a lower V_{RAMP}, as long as the criterion shown in Equation (7) are met.

For PWM operation, $V_{FB(AVG)}$ can be determined with Equation (15):

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2}V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_8} \quad (15)$$

R8 is set to 0Ω and can be set using Equation (16) for better noise immunity. Also, it should be five times smaller than R1//R2 to minimize its influence on V_{RAMP}. R8 can be calculated with Equation (16):

$$R_8 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (16)$$

Using Equation (14) on page 17 to calculate R1 can be complicated. To simplify the calculation, a DC-blocking capacitor (CDC) can be added to filter the DC influence from R4 and R8. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using the simplified equation for PWM mode shown in Equation (17):

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R_2 \quad (17)$$

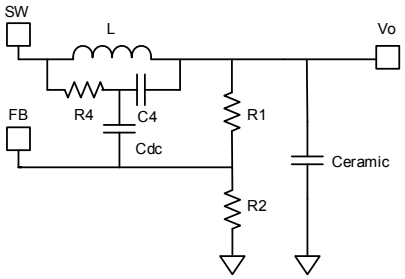


Figure 12: Simplified Circuit of Ceramic Capacitor with DC Blocking Capacitor

CDC is suggested to be at least 10 times larger than C4 for better DC-blocking performance, and should not be larger than 0.47μF, considering start-up performance. If a larger CDC is needed for better FB noise immunity, combine it with reduced R1 and R2 to limit CDC reasonably without affecting the system start-up. Note that even when the CDC is applied, the load and line regulations are still V_{RAMP}-related.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. For best performance, use a ceramic capacitor placed as close to VIN as possible. Ceramic capacitors with X5R and X7R dielectrics are recommended because of their low ESR and small temperature coefficients.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (18):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (19):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (19)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (20):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (21):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (21)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (22):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (22)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (23):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

Since the output voltage ripple caused by the ESR is very small, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. Since the ramp voltage generated from the ESR is high enough to stabilize the system, an external ramp is not needed. A minimum ESR value of around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated with Equation (24):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

The maximum output capacitor limitation should be considered during design application. The MP8758H has a soft-start time period of around 2.9ms. If the output capacitor value is too large, the output voltage cannot reach the design value during the soft-start time and cannot regulate. The maximum output capacitor value limitation (C_{o_max}) can be estimated using Equation (25):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (25)$$

Where I_{LIM_AVG} is the average start-up current during a soft-start period, and T_{ss} is the soft-start time.

Selecting the Inductor

The inductor is necessary to supply a constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, a higher series resistance, and a lower saturation current. When determining the inductance value, select the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (26):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be estimated with Equation (27):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (27)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 13 and follow the guidelines below.

1. Place the high-current paths (PGND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitors as close to VIN and PGND as possible.
3. Place the decoupling capacitor as close to VCC and AGND as possible. If the distance is long, place the capacitor close to VCC. If a via is required to reduce the leakage inductance, use >3 vias.
4. Keep the switching node (SW) short and away from the feedback network.
5. Place the external feedback resistors next to FB, ensuring that there is no via on the FB trace.
6. Keep the BST voltage path as short as possible.
7. Keep the VIN and PGND pads connected with large copper traces, using at least two layers for the IN and PGND traces to achieve better thermal performance. To help with thermal dissipation, add several vias with 10mil_drill/18mil_copper_width close to the VIN and PGND pads. A four-layer layout is recommended strongly to achieve better thermal performance.

NOTE:

Please refer to the PCB Layout Application Note for more details.

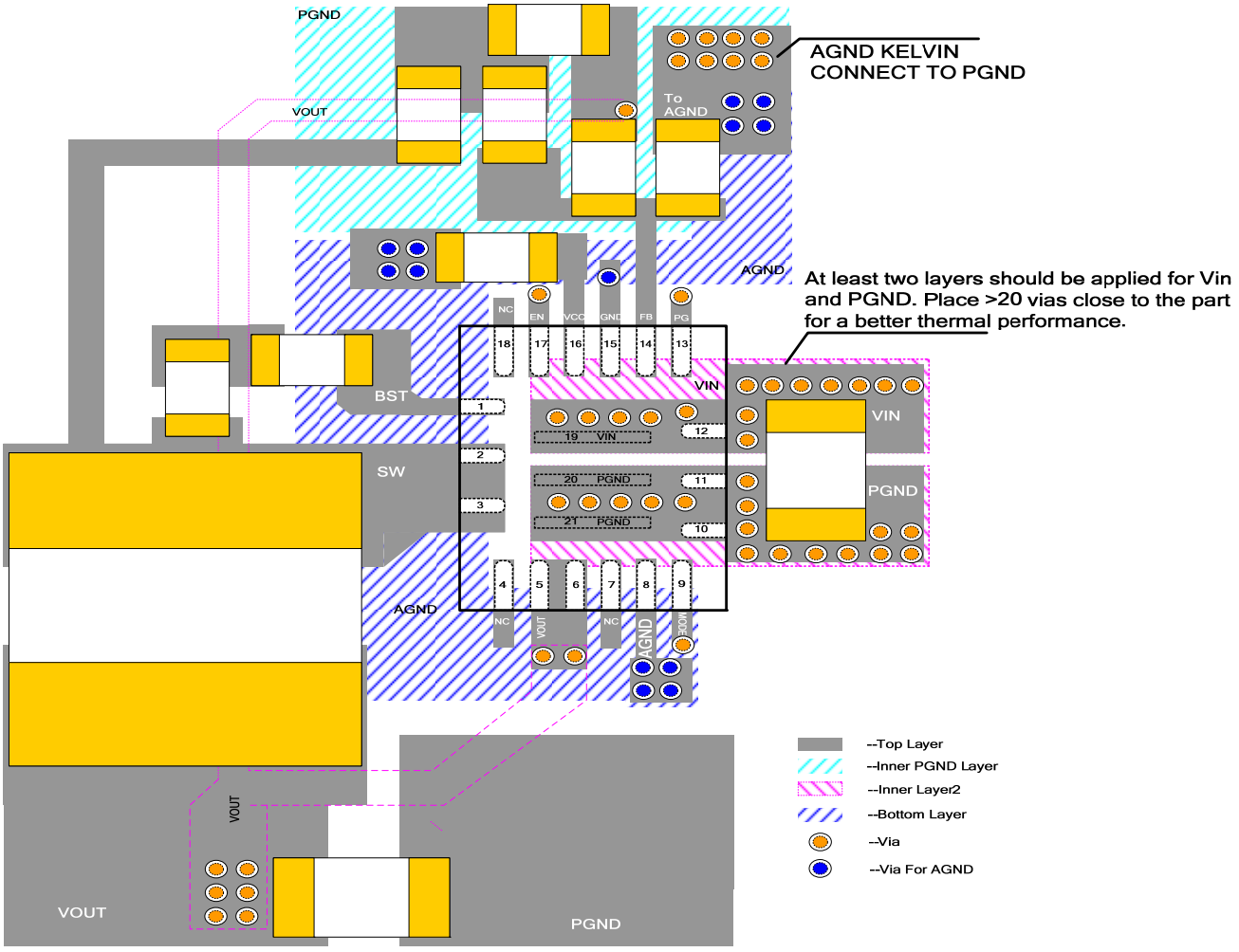


Figure 13: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2 : Design Example

V_{OUT} (V)	Cout (F)	L (µH)	R4 (Ω)	C4 (F)	R1 (kΩ)	R2 (kΩ)
1.05	22µx3	1.2	NS	220p	59	82
1.2	22µx3	1.2	NS	220p	100	100
1.35	22µx3	1.2	NS	220p	100	82
3.3	22µx4	2	1M	220p	88.7	18
5	22µx4	2	1M	220p	150	18

The detailed application schematics for 1.2V and 5V application (when low ESR capacitors are applied) are shown in Figure 14 and Figure 15. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

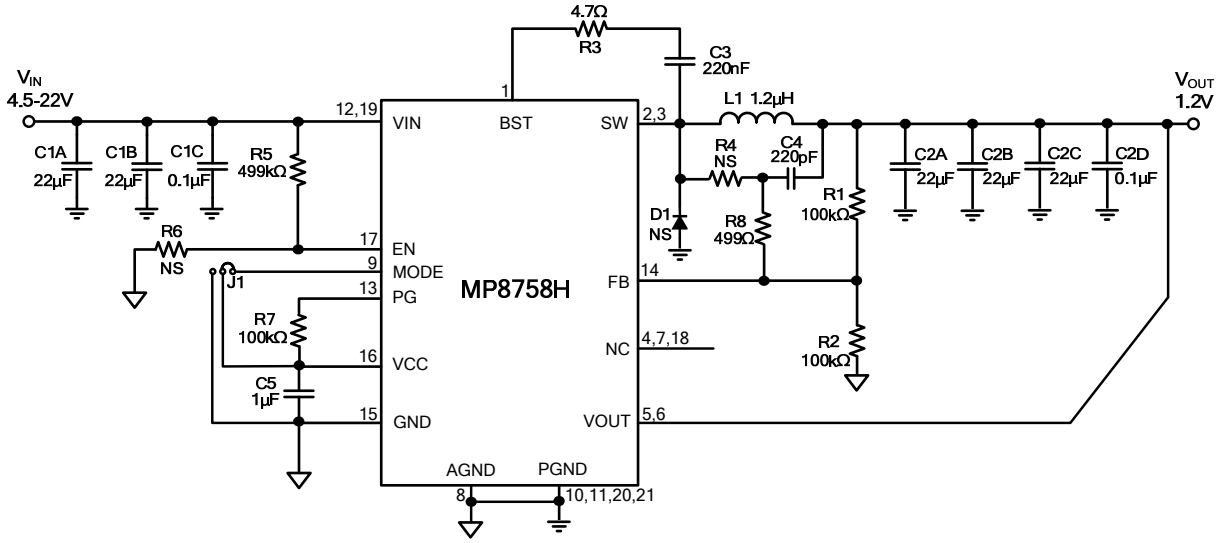


Figure 14: Typical Application Circuit with Low ESR Ceramic Output Capacitor

V_{IN}=4.5-22V, V_{OUT}=1.2V

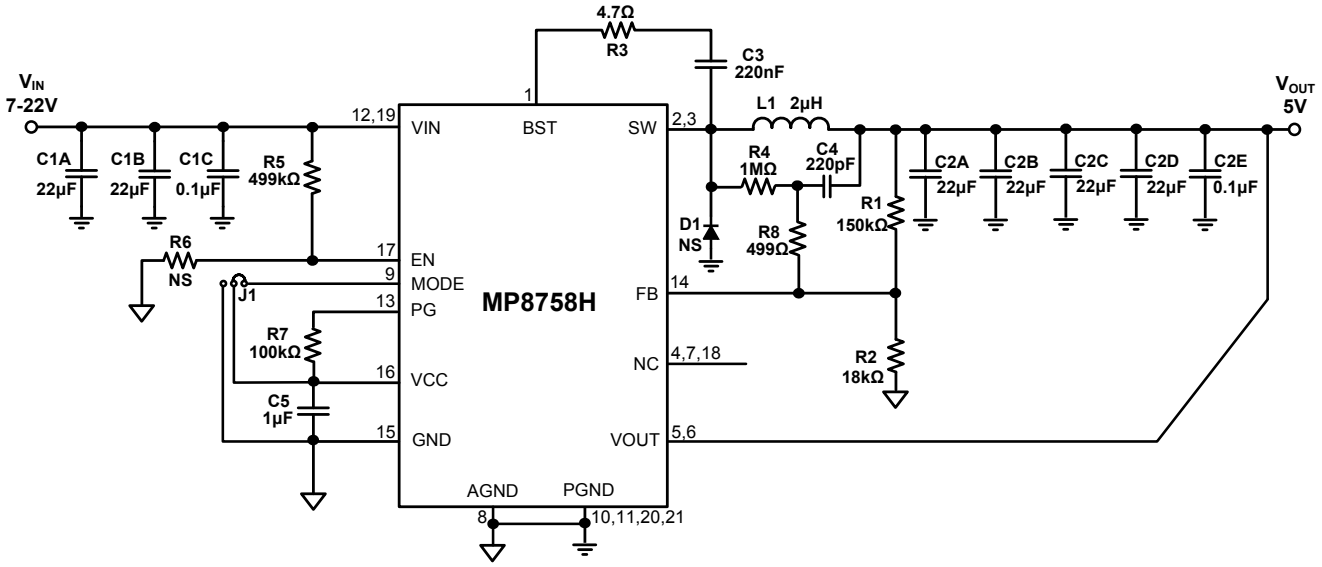
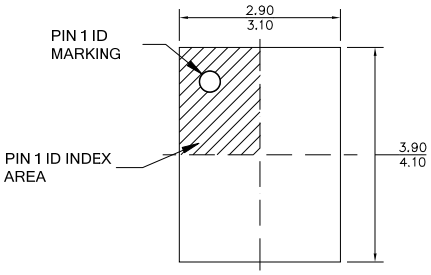


Figure 15: Typical Application Circuit with Low ESR Ceramic Output Capacitor

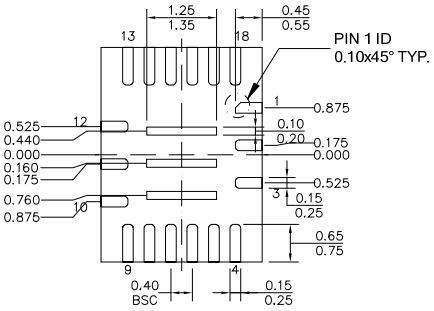
V_{IN}=7-22V, V_{OUT}=5V

PACKAGE INFORMATION

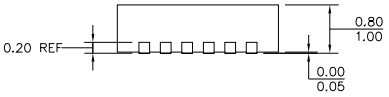
QFN-21 (3mmx4mm)



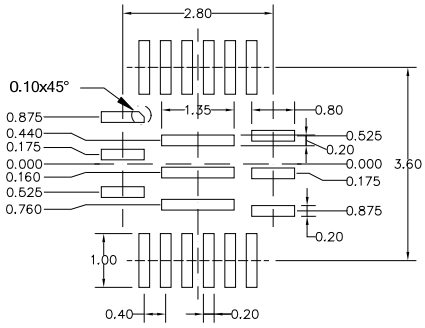
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.