

100V, 2.5A, High Frequency Half-Bridge Gate Driver

DESCRIPTION

The MP18021A is a high-frequency, 100V, half bridge, N-channel power MOSFET driver. Its low side and high side driver channels are independently controlled and matched with a time delay of less than 5ns. Under-voltage lockout on both high side and low side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

FEATURES

- Drives N-Channel MOSFET Half Bridge
- 100V V_{BST} Voltage Range
- On-Chip Bootstrap Diode
- Typical 16ns Propagation Delay Time
- Less Than 5ns Gate Drive Matching
- Drives 1nf Load with 12ns/9ns Rise/Fall Times with 12V VDD
- TTL Compatible Input
- Less Than 150μA Quiescent Current
- UVLO for Both High Side and Low Side
- In SOIC8E and QFN8 (3×3mm) Packages

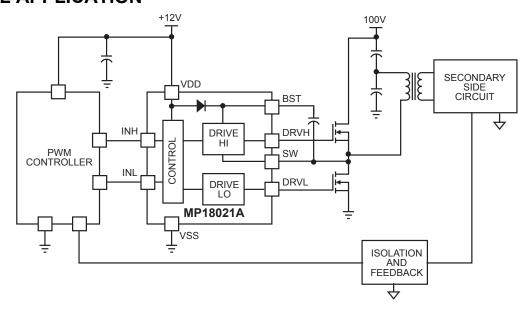
APPLICATIONS

- Telecom Half Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

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TYPICAL APPLICATION





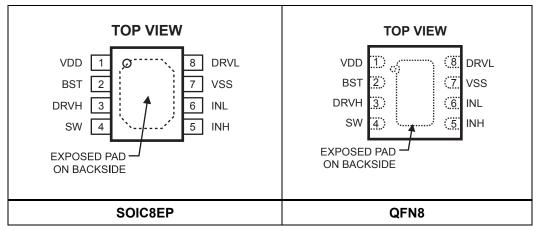
ORDERING INFORMATION

Part Number	Package	Top Marking
MP18021HN-A*	SOIC8E	MP18021A
MP18021HQ-A**	QFN8 (3x3mm)	ACP

* For Tape & Reel, add suffix –Z (e.g. MP18021HN–A–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP18021HN–A–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP18021HQ–A–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP18021HQ–A–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V _{DD})SW Voltage (V _{SW})	0.3V to +20V 5.0V to +105V
BST Voltage (V _{BST})	0.3V to +120V
BST to SW	
DRVH to SW0.3V to	(BST-SW) + 0.3V
DRVL to VSS0.3\	to (VDD + 0.3V)
All Other Pins0.3	$8V \text{ to } (V_{DD} + 0.3V)$
Continuous Power Dissipation	$(T_A = 25^{\circ}C)^{(2)}$
SOIC8E	2.6W
QFN8 (3x3mm)	2.5W
Continuous Power Dissipation	$(T_A=100^{\circ}C)^{(2)}$
SOIC8E	
QFN8 (3x3mm)	0.5W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (V _{DD})	9.0V to 18V
	1.0V to +100V
• (•,	<50V/nsec
Operating Junction T	emp. (T _J)40°C to +125°C

Thermal Resistance (4)	$oldsymbol{ heta}_{JA}$	$oldsymbol{ heta}_{JC}$
SOIC8E	48	10 °C/W
QFN8 (3x3mm)	50	12 °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.



ELECTRICAL CHARACTERISTICS

 $V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, No load at DRVH and DRVL, $T_A = 25$ °C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units	
Supply Currents							
VDD quiescent current	I_{DDQ}	INL=INH=0		100	150	μΑ	
VDD operating current	I _{DDO}	f _{sw} =500kHz		2.8	3.5	mA	
Floating driver quiescent current	I _{BSTQ}	INL=INH=0		60	90	μΑ	
Floating driver operating current	I _{BSTO}	f _{sw} =500kHz		2.1	3	mA	
Leakage Current	I_{LK}	BST=SW=100V		0.05	1	μΑ	
Inputs							
INL/INH High				2	2.4	V	
INL/INH Low			1	1.4		V	
INL/INH internal pull-down	R _{IN}			185		kΩ	
resistance	IN			100		NS2	
Under Voltage Protection	r					,	
VDD rising threshold	V_{DDR}		7.7	8.1	8.5	V	
VDD hysteresis	V_{DDH}			0.5		V	
(BST-SW) rising threshold	V_{BSTR}		6.7	7.1	7.5	V	
(BST-SW) hysteresis	V_{BSTH}			0.55		V	
Bootstrap Diode							
Bootstrap diode VF @ 100uA	V_{F1}			0.5		V	
Bootstrap diode VF @ 100mA	V_{F2}			0.9		V	
Bootstrap diode dynamic R	R_D	@ 100mA		2.5		Ω	
Low Side Gate Driver							
Low level output voltage	V_{OLL}	I _O =100mA		0.15	0.22	V	
High level output voltage to rail	V_{OHL}	I _O =-100mA		0.45	0.6	V	
Peak pull-up current	I _{OHL}	V_{DRVL} =0V, V_{DD} =12V		1.5		Α	
l eak pull-up current		V_{DRVL} =0V, V_{DD} =16V		2.5		Α	
Peak pull-down current	ı	V _{DRVL} =V _{DD} =12V		2.5		Α	
Peak pull-down current	I _{OLL}	V _{DRVL} =V _{DD} =16V		3.5		Α	
Floating Gate Driver							
Low level output voltage	V_{OLH}	I _O =100mA		0.15	0.22	V	
High level output voltage to rail	V_{OHH}	I _O =-100mA		0.45	0.6	V	
Peak pull-up current	I _{OHH}	V _{DRVH} =0V, V _{DD} =12V		1.5		Α	
r eak puil-up cuitetit		V _{DRVH} =0V, V _{DD} =16V		2.5		Α	
Peak pull-down current	1-	V _{DRVH} =V _{DD} =12V		2.5		Α	
r eak puil-down current	I _{OLH}	V _{DRVH} =V _{DD} =16V		3.5		Α	



ELECTRICAL CHARACTERISTICS (continued)

 $V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, No load at DRVH and DRVL, $T_A = 25$ °C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Switching Spec Low Side Gate Driver						
Turn-off propagation delay INL falling to DRVL falling				16		ns
Turn-on propagation delay INL rising to DRVL rising	Turn-on propagation delay			16		
DRVL rise time		C _L =1nF		12		ns
DRVL fall time		C _L =1nF		9		ns
Switching Spec Floating Gate	e Driver					
Turn-off propagation delay INL falling to DRVH falling	T_{DHFF}			16		ns
Turn-on propagation delay INL rising to DRVH rising	T_{DHRR}			16		ns
DRVH rise time		C _L =1nF		12		ns
DRVH fall time		C _L =1nF		9		ns
Switching Spec Matching						
Floating driver turn-off to low side drive turn-on	T_{MON}			1	5	ns
Low side driver turn-off to floating driver turn-on				1	5	ns
Minimum input pulse width that changes the output					50 ⁽⁵⁾	ns
Bootstrap diode turn-on or turn-off time	T _{BS}			10 ⁽⁵⁾		ns
Over Temperature Protection ⁽⁵⁾			•			
OTP entry threshold				160		
OTP recovery threshold				140		°C
OTP hysteresis				20		

Note:

⁵⁾ Derived from bench characterization. Not tested in production.

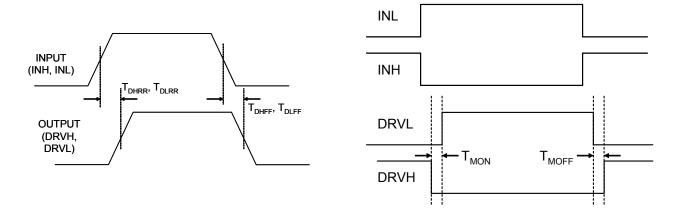


Figure 1—Timing Diagram



PIN FUNCTIONS

Pin#	Name	Description
1	VDD	Supply input. This pin supplies power to all the internal circuitry. A decoupling capacitor to ground must be placed close to this pin to ensure stable and clean supply.
2	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
3	DRVH	Floating driver output.
4	SW	Switching node.
5	INH	Control signal input for the floating driver.
6	INL	Control signal input for the low side driver.
7	VSS, Exposed Pad	Chip ground. Connect exposed pad to VSS for proper thermal operation.
8	DRVL	Low side driver output.



TYPICAL PERFORMANCE CHARACTERISTICS

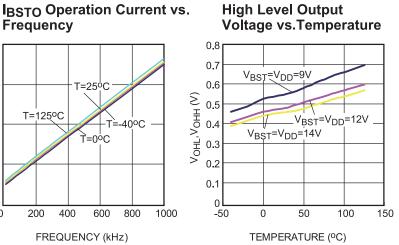
 V_{DD} =12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

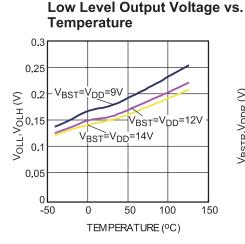
Frequency 5 T=-40°C =0°C lppo (mA) 3 T=25°C 2 T=125°C 200 400 600 800 1000

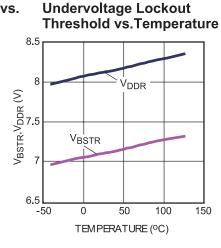
FREQUENCY (kHz)

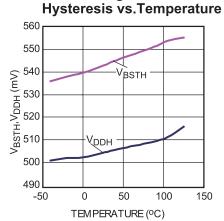
IDDO Operation Current vs.

Frequency 3 T=25^oC IBSTO (mA) T=125°C -40°C T=00C 0 200 400 600 800 1000 FREQUENCY (kHz)

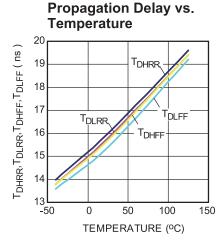


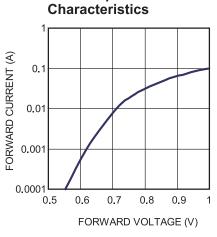




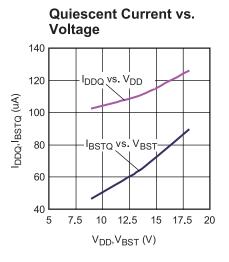


Undervoltage Lockout





Bootstrap Diode I-V

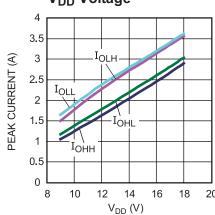




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 V_{DD} =12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

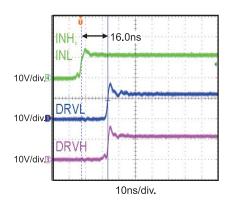
Peak Current vs. V_{DD} Voltage

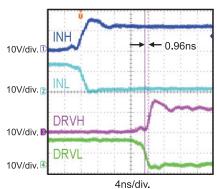


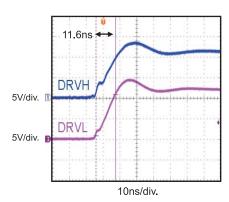
Turn-on Propagation Delay

Gate Drive Matching TMOFF

Drive Rise Time (1nF Load)



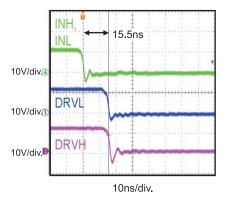


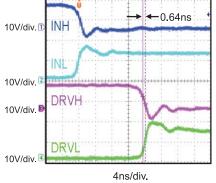


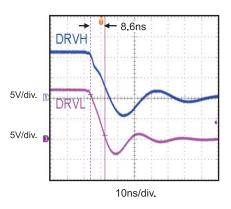
Turn-off Propagation Delay

Gate Drive Matching TMON

Drive Fall Time (1nF Load)









BLOCK DIAGRAM

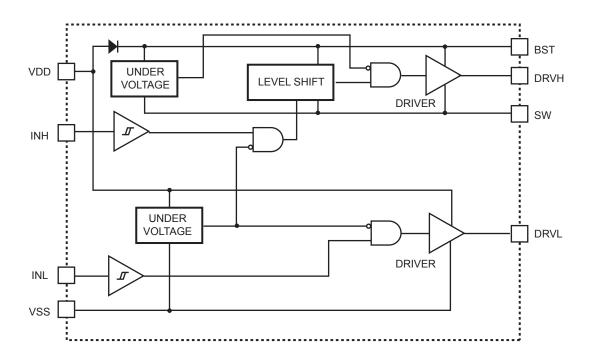
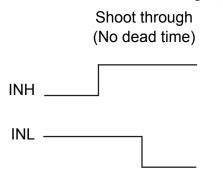


Figure 2—Function Block Diagram

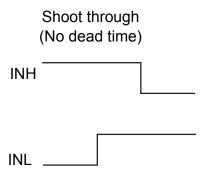


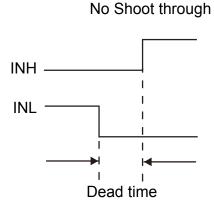
APPLICATION

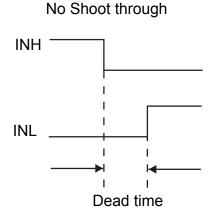
The input signals of INH and INL can be controlled independently. If both INH and INL are controlling HSFET and LSFET of the same bridge, then users must avoid shoot through by



setting sufficient dead time between INH and INL low, and vice versa. See below figure. Dead time is defined as the time internal between INH low and INL low.









REFERENCE DESIGN CIRCUITS

Half Bridge Converter

In half-bridge converter topology, the MOSFETs are driven alternately with some dead time. Therefore, INH and INL are driven with

alternating signals from the PWM controller. The input voltage can be up to 100V in this application.

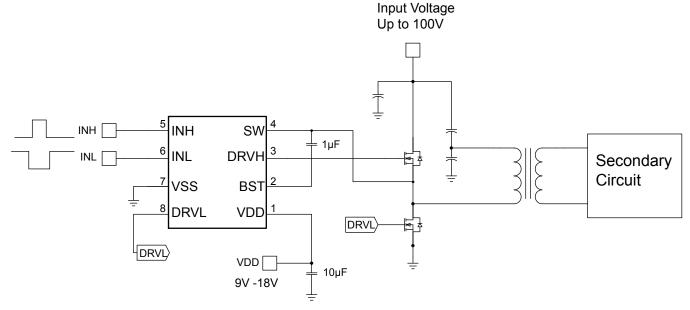


Figure 3 - Half Bridge Converter

Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off together. The input signal (INH and INL) comes from the PWM controller, which senses the output voltage (and output current if current-mode control is used).

The Schottky diodes clamp the reverse swing of the power transformer and must be rated at the input voltage. The input voltage can be up to 100V in this circuit.

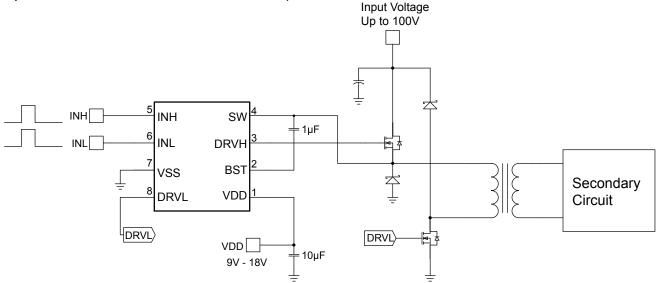


Figure 4 – Two-Switch Forward Converter



Active-Clamp Forward Converter

In active-clamp forward converter topology, the MOSFETs are driven alternately. The high-side MOSFET, along with capacitor C_{reset} , is used to reset the power transformer in a lossless manner.

This topology lends itself well to run at duty cycles exceeding 50%. For these reasons, the input voltage may not be able to run at 100V for this application.

Input Voltage

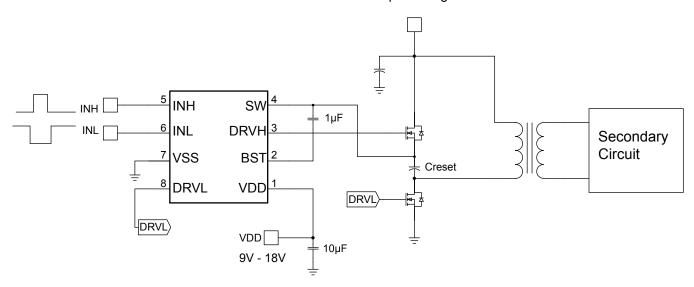
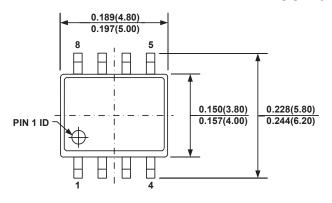


Figure 5 - Active-Clamp Forward Converter

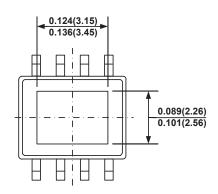


PACKAGE INFORMATION

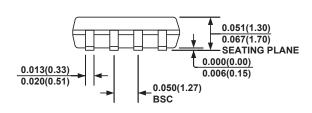
SOIC8E



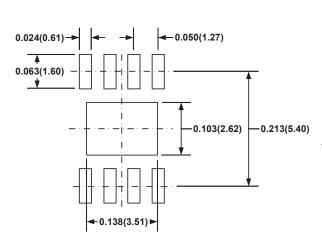
TOP VIEW



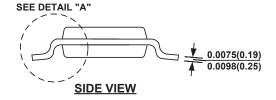
BOTTOM VIEW

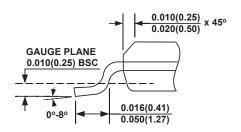


FRONT VIEW



RECOMMENDED LAND PATTERN





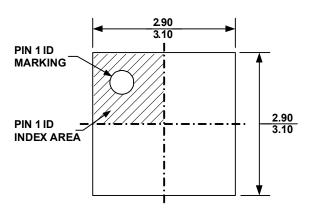
DETAIL "A"

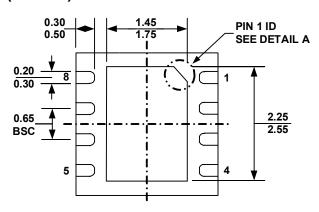
NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.



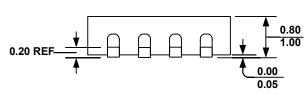
QFN8 (3×3mm)



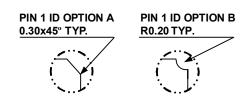


TOP VIEW

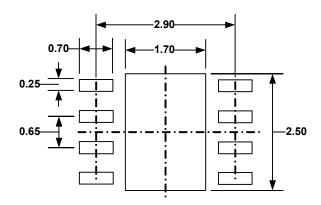
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
- 3) LEAD COPLANARITY SHALL BED.10 MILLIMETER MAX
- 4) DRAWING CONFORMS TO JEDEC MO229, VARIATION VEEC-2.
- 5) DRAWING IS NOT TO SCALE

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