MIC95410 Evaluation Board

6.6mΩ $R_{DS(ON)}$, 7A, 5.5V_{IN} Load Switch in 1.2mm x 2.0mm QFN Package

General Description

The MIC95410 is a high-side load switch used for computing and for ultra-dense embedded computing boards where high-current, low-voltage rails from sub-1V to 5.5V have to be sectioned. The integrated 6.6mΩ $R_{DS(ON)}$ N-channel MOSFET ensures low voltage drop and low power dissipation while delivering up to 7A of load current.

The MIC95410 provides user-adjustable slew-rate-controlled turn-on to limit the inrush current to the input supply voltage.

The MIC95410 is available in thermally efficient, space-saving 10-pin 1.2mm × 2.0mm QFN package with 0.5mm pin pitch and an operating junction temperature range from –40°C to +125°C.

The basic parameters of the MIC95410 evaluation board are the IN supply of 1V to 5.5V and the separated bias voltage from 2.7V to 9V. It also includes a TTL-logic level turn-on command (CTL) and an output discharge function when disabled.

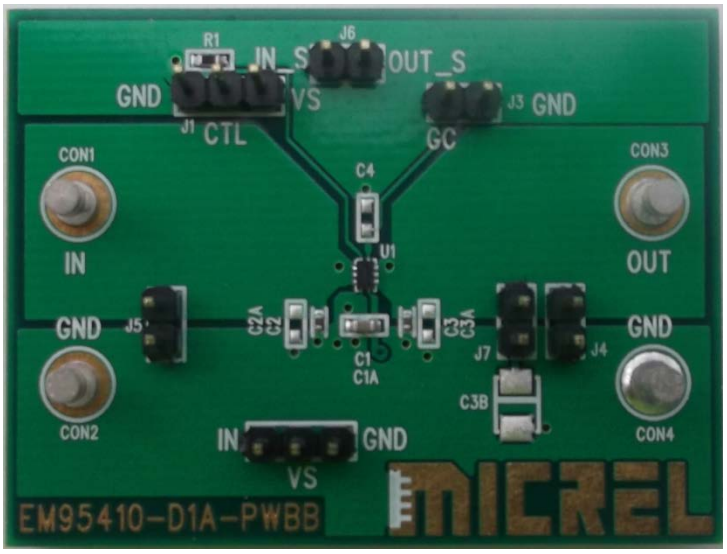
Due to the optimized pinout of the MIC95410, the evaluation board can achieve a two-layer-only routing (top and bottom), while internal planes are connected to GND and kept as solid GND planes for best thermal performance. See PCB Layout section.

MIC95410 datasheet and support documentation are available on Micrel's web site at: www.micrel.com.

Ordering Information

Part Number	Description
MIC95410YFL EV	MIC95410 Evaluation Board

Evaluation Board



Getting Started

Recommended Setup

The MIC95410 evaluation board setup comprises of the following points:

- A power supply with at least 7A of current capability for IN, not to exceed 5.5V.
- A passive or active load which can handle up to 7A at 5.5V, connected at OUT (CON3) / GND (CON4).
- A low-power bias supply for VS, 2.7V ≤ V_{VS} ≤ 9V.
- A function generator for driving CTL.
- A digital multi-meter (DMM).

The bias supply pin VS can be shorted to IN by means of the VS header located at the bottom of the board near the label. In this case, evaluation can be performed for 2.7V ≤ VIN ≤ 5.5V, and the low-power bias supply for VS can be avoided. Similarly, the CTL pin can be shorted to VS by means of header J1, making the function generator redundant.

Power-Up Precautions

The evaluation board does not have reverse polarity protection. Applying a negative voltage to the IN or VS terminals may damage the device.

The turn-on of the MIC95410, especially in the presence of large output capacitive loads associated with long input leads, may cause some L-C ringing. The ringing may cause false current readings and generate voltage overshoot. Reducing the length of the input leads as much as possible (10cm or less) or using a large electrolytic decoupling capacitor (up to some mF) between IN (CON1) and GND (CON2) of the evaluation board is recommended.

Recommended Steps

1. **Ensure no jumper is installed at J1.**

   R1 will pull down the CTL pin and keep the MIC95410 disabled until Step 8.

2. **Connect the VS supply.**

   Connect the VS bias supply to terminals J2-2 (VS)/J2-1 (GND). J2 is the connector at the bottom edge of the evaluation board.
   Alternatively, VS can be shorted to IN by installing a jumper across positions J2-3 (IN) and J2-2 (VS). This is possible only for 2.7V ≤ V_{IN} ≤ 5.5V. If V_{IN} is lower than 2.7V, an external independent bias supply for VS is mandatory.

3. **Connect the IN supply.**

   Connect the power supply to the IN (CON1) and GND (CON2) terminals and regulate its current limit to approximately 7.5A. An ammeter may be placed between the input supply and the IN terminal to the evaluation board. Ensure that the supply voltage is monitored at the IN terminal (CON1 or J5), because the ammeter and/or power lead resistance can reduce the voltage supplied to the input. Keep the power supply disabled; do not apply power until Step 7.

4. **Connect the load to the output terminals.**

   Connect the load across the terminals OUT (CON3)/GND (CON4). Adjust the load. Do not exceed a 7A current. Output voltage may be monitored at J4.

5. **Connect the DMM across the MIC95410.**

   Set the DMM to a mV voltage reading and connect it between J6-1 (IN_S, positive terminal) and J6-2 (OUT_S, negative terminal). This is for reading the voltage drop across the MIC95410.

6. **Connect the function generator to CTL.**

   Connect the function generator between J1-2 (CTL) and J1-1 (GND). Set it to DC mode with the level between 2.4V and V_{VS} (unterminated). Keep the output disabled.

7. **Enable the IN and VS supplies.**

8. **Enable the MIC95410.**

   Enable the MIC95410 by enabling the function generator output. Alternatively, install a jumper across J1-2 (CTL) and J1-3 (VS).
   Verify that the input voltage passes to the output and monitor the voltage drop across the MIC95410 with the DMM.

Evaluation Board Description

J1 - CTL (Control) Input

The MIC95410 can be turned ON or OFF by setting a TTL high logic level to pin CTL (J1-2). Pin J1-2 is pulled to GND through R1, such that CTL is not left floating.

CTL can be driven either at DC (static) or by a square wave signal. For square wave drive, ensure the frequency of the signal is low enough to limit the turn-on/turn-off power dissipation within safe limits. Also depending on the load, frequencies of 1Hz or lower are recommended.

For static drive, installing/removing a jumper across positions J2-2 (CTL) and J2-3 (VS) is adequate.

J2 - VS Supply

The MIC95410 has a separate bias pin (VS) for powering the charge pump ($2.7V \le V_{VS} \le 9V$). The bias power supply should be connected at J2-2 (VS)/J2-1 (GND). Alternatively, VS can be shorted to IN by installing a jumper across positions J2-3 (IN) and J2-2 (VS). This is possible only for $2.7V \le V_{IN} \le 5.5V$.

J3 - GC

GC (gate connection of power MOSFET switch) can be monitored at J3. Because the current sourcing capability of GC is limited, ensure that the impedance of the monitoring input does not cause excessive loading.

Install a capacitor in position C4 to adjust the turn-on speed/inrush current.

J4 - OUT

J4 can be used to monitor the output voltage.

The MIC95410 output capacitance can be increased by installing a 0603 ceramic capacitor in position C3A.

Note, this is a two-pin header with one pin connected to a power supply voltage and the other pin connected to GND. Never install a jumper on this header because it will short the power supply to GND.

J5 - IN

J5 can be used to monitor the input voltage.

The MIC95410 input capacitance can be increased by installing a 0603 ceramic capacitor in position C2A.

Note that this is a two-pin header with one pin connected to a power supply voltage and the other pin connected to GND. Never install a jumper on this header because it will short the power supply to GND.

J6 – Voltage Drop Sensing

J6 can be used to monitor the voltage drop across the MIC95410.

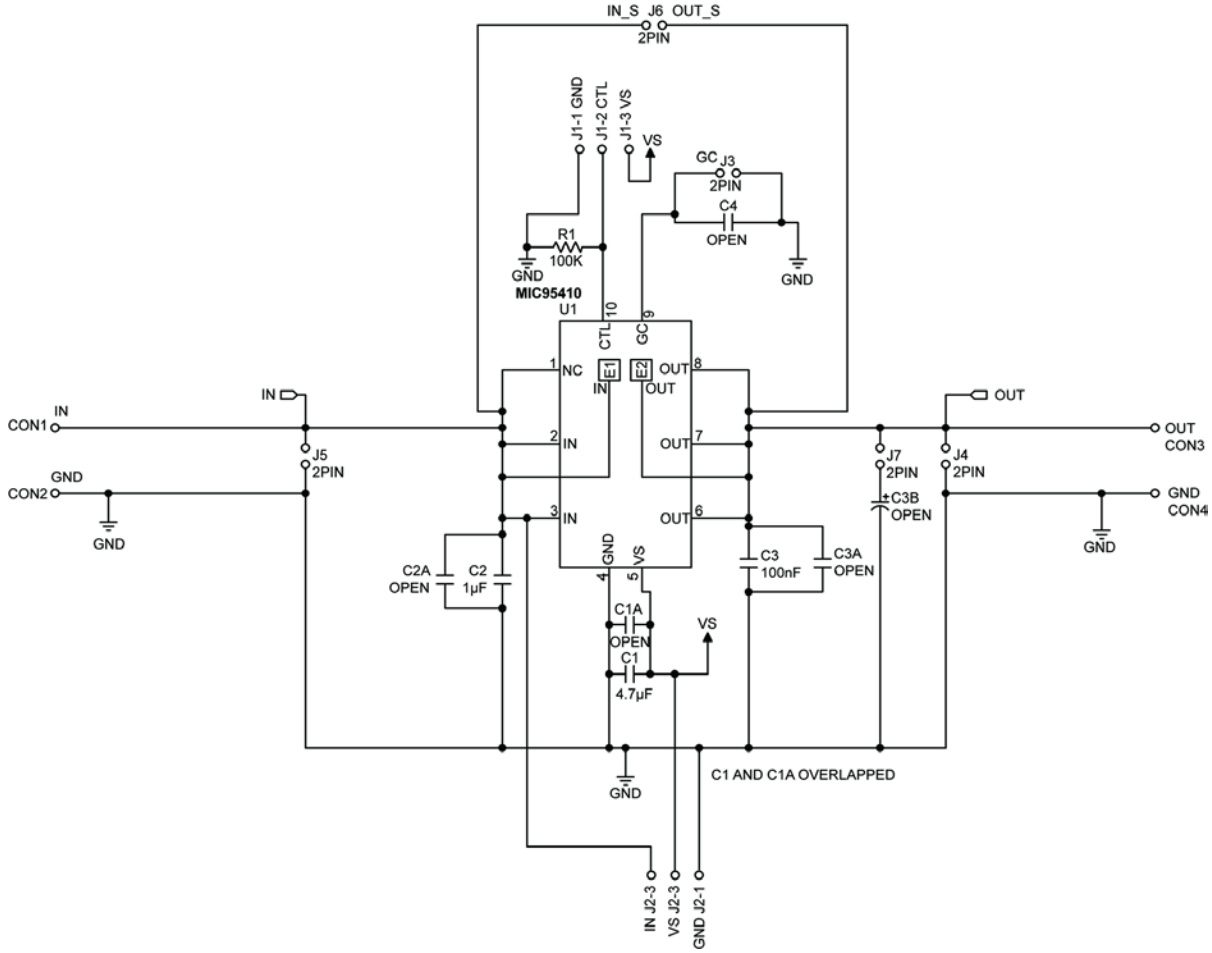
Please note that the solder joints and some unavoidable copper trace distance also add up to the $R_{DS(ON)}$ of the MIC95410 and, therefore, the measured resistive drop is slightly larger than the pure intrinsic $R_{DS(ON)}$ contribution.

J7 – Capacitive LOAD

To emulate the effect of large load capacitors at the output side of the MIC95410, it is possible to install a capacitor in position C3B.

J7 can be used to connect/disconnect C3B.

Evaluation Board Schematic



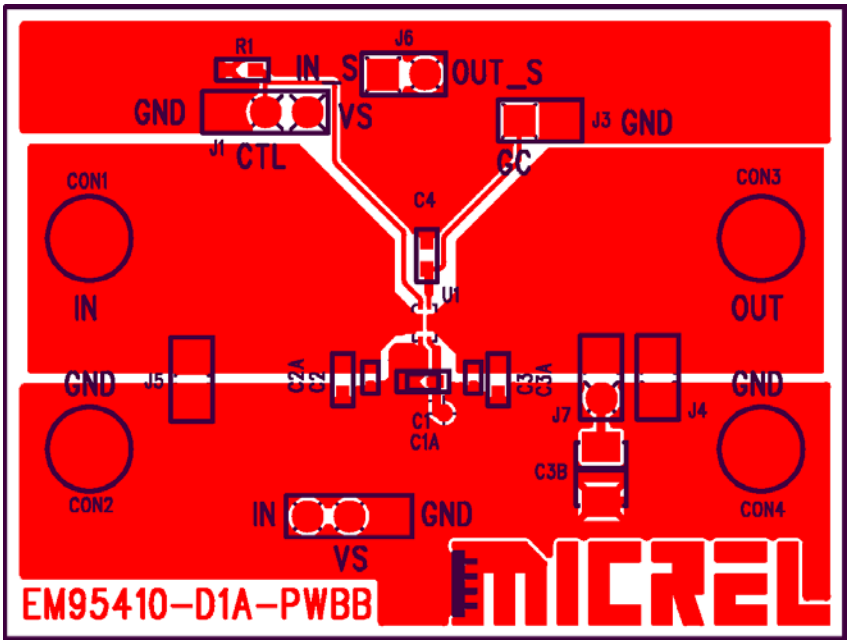
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	GRM188R61C475KE11	Murata[1]	Capacitor, ceramic, X5R, 4.7uF 16V 10%, Size 0603.	1
C2	GRM155R61C105MA12	Murata	Capacitor, ceramic, X5R, 1uF 16V 20%, Size 0402.	1
C3	GRM155R61H104ME14	Murata	Capacitor, ceramic, X5R, 100nF 50V 20%, Size 0402.	1
C1A		ANY	Not Installed, Size 0402.	
C4 C2A C3A		ANY	Not Installed, Size 0603.	
C3B		ANY	Not installed, Size EIA-3528.	
R1	RC0603-104J	ANY	Resistor, 100kΩ 5%, Size 0603.	1
U1	**MIC95410YFL**	**Micrel, Inc.**[2]	**6.6mΩ $R_{DS(ON)}$, 7A, 5.5V_{IN} Load Switch in 1.2mm × 2.0mm QFN Package.**	**1**

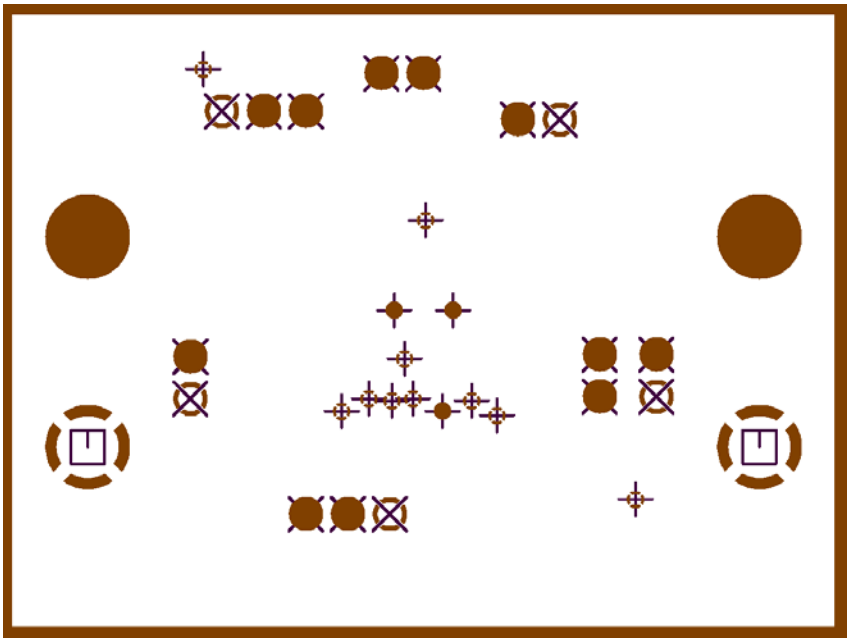
Notes:

1. Murata: www.murata.com.
2. **Micrel, Inc.:** www.micrel.com.

PCB Layout

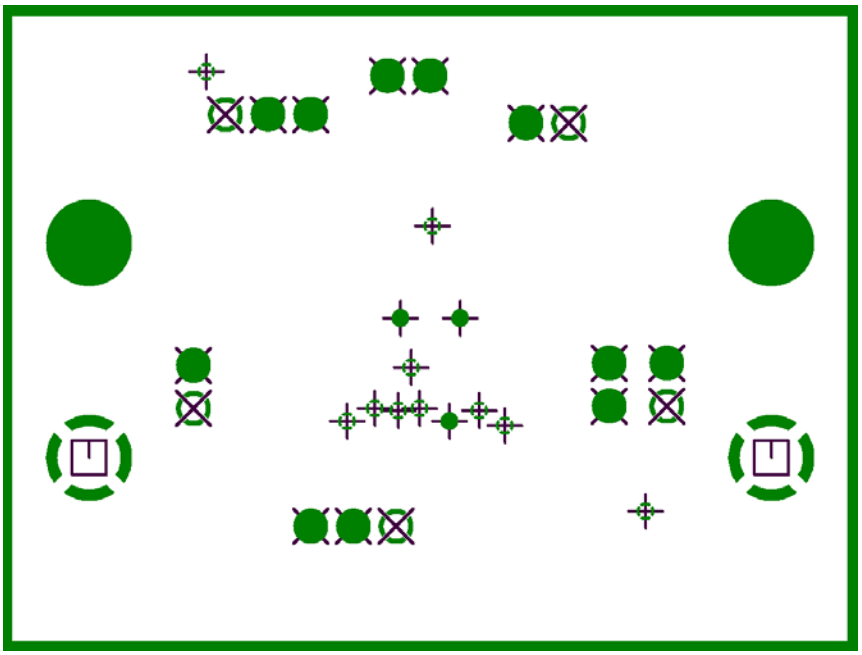


Top Layer (Routing)

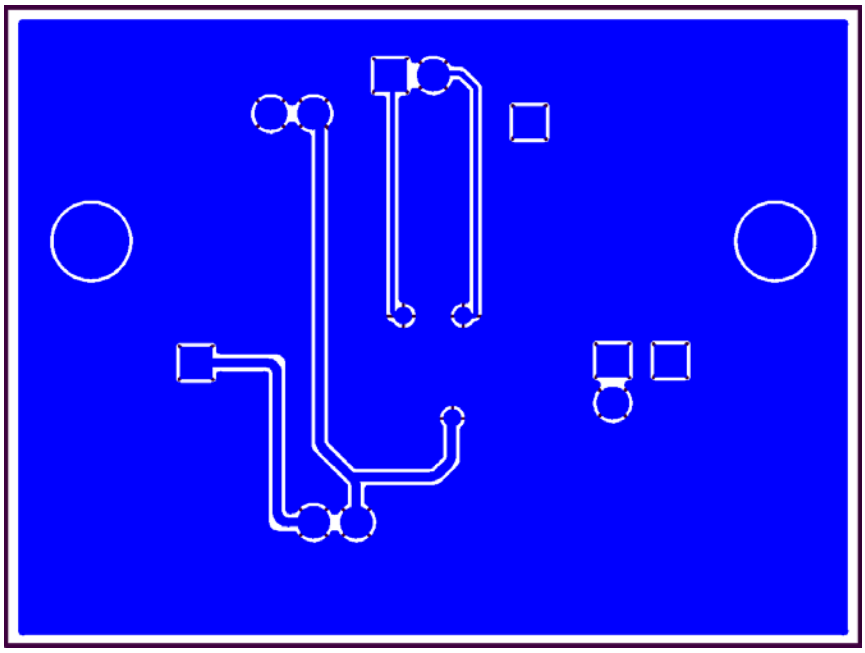


Mid Layer 1 (GND plane)

PCB Layout (Continued)



Mid Layer 2 (GND plane)



Bottom Layer (Routing) – Top View

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