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74LVC2G240-Q100

Dual inverting buffer/line driver; 3-state

Rev. 2 — 14 December 2016   **Product data sheet**

1. General description

The 74LVC2G240-Q100 is a dual inverting buffer/line driver with 3-state outputs. The output enable inputs $1\overline{OE}$ and $2\overline{OE}$, control the 3-state outputs. A HIGH level at pins $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G240-Q100 as a translator in a mixed 3.3 V and 5 V environment.

It is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
    - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
    - JESD8-7 (1.65 V to 1.95 V)
    - JESD8-5 (2.3 V to 2.7 V)
    - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
    - MIL-STD-883, method 3015 exceeds 2000 V
    - HBM JESD22-A114F exceeds 2000 V
    - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V

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3. Ordering information

Table 1.   Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVC2G240DP-Q100	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74LVC2G240DC-Q100	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
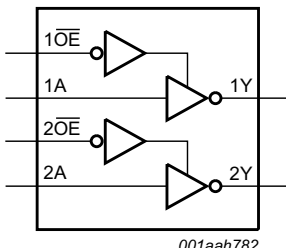
4. Marking

Table 2.   Marking codes

Type number	Marking code[1]
74LVC2G240DP-Q100	V240
74LVC2G240DC-Q100	V40

[1]   The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

Fig 1.   Logic symbol

Fig 2.   IEC logic symbol

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6. Pinning information

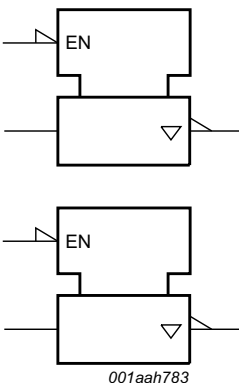## 6.1 Pinning

74LVC2G240-Q100

1$\overline{\text{OE}}$	1		8	V$_{CC}$
1A	2		7	2$\overline{\text{OE}}$
2Y	3		6	1Y
GND	4		5	2A

aaa-015347
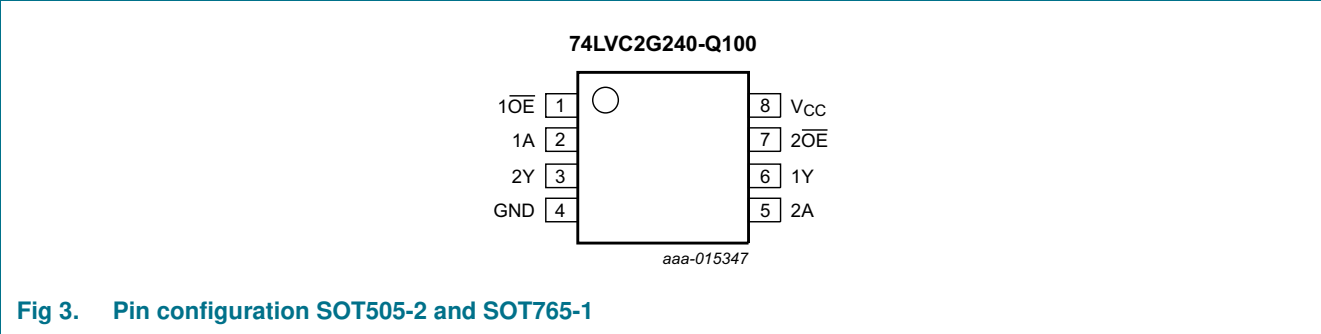
Fig 3.   Pin configuration SOT505-2 and SOT765-1

6.2 Pin description

Table 3.   Pin description

Symbol	Pin	Description
1$\overline{\text{OE}}$	1	output enable input 1$\overline{\text{OE}}$ (active LOW)
1A	2	data input
2Y	3	data output
GND	4	ground (0 V)
2A	5	data input
1Y	6	data output
2$\overline{\text{OE}}$	7	output enable input 2$\overline{\text{OE}}$ (active LOW)
V$_{CC}$	8	supply voltage

7. Functional description

Table 4.   Function table[1]

Input		Output
n$\overline{\text{OE}}$	nA	nY
L	L	H
L	H	L
H	X	Z

[1]   H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1]	−0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Enable mode	[1]	−0.5	V_{CC} + 0.5	V
		Disable mode	[1]	−0.5	+6.5	V
		Power-down mode	[1][2]	−0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			−100	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C	[3]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.
For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly at 8.0 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	V_{CC} = 1.65 V to 5.5 V; Enable mode	0	V_{CC}	V
		V_{CC} = 1.65 V to 5.5 V; Disable mode	0	5.5	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −100 μA; V_{CC} = 1.65 V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	-	-	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±2	μA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	0.1	4	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	μA
C_I	input capacitance		-	2	-	pF

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Table 7. **Static characteristics** *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T$_{amb}$ = −40 °C to +125 °C						
V$_{IH}$	HIGH-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	0.65 × V$_{CC}$	-	-	V
		V$_{CC}$ = 2.3 V to 2.7 V	1.7	-	-	V
		V$_{CC}$ = 2.7 V to 3.6 V	2.0	-	-	V
		V$_{CC}$ = 4.5 V to 5.5 V	0.7 × V$_{CC}$	-	-	V
V$_{IL}$	LOW-level input voltage	V$_{CC}$ = 1.65 V to 1.95 V	-	-	0.35 × V$_{CC}$	V
		V$_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		V$_{CC}$ = 2.7 V to 3.6 V	-	-	0.8	V
		V$_{CC}$ = 4.5 V to 5.5 V	-	-	0.3 × V$_{CC}$	V
V$_{OL}$	LOW-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = 100 μA; V$_{CC}$ = 1.65 V to 5.5 V	-	-	0.1	V
		I$_O$ = 4 mA; V$_{CC}$ = 1.65 V	-	-	0.70	V
		I$_O$ = 8 mA; V$_{CC}$ = 2.3 V	-	-	0.45	V
		I$_O$ = 12 mA; V$_{CC}$ = 2.7 V	-	-	0.60	V
		I$_O$ = 24 mA; V$_{CC}$ = 3.0 V	-	-	0.80	V
		I$_O$ = 32 mA; V$_{CC}$ = 4.5 V	-	-	0.80	V
V$_{OH}$	HIGH-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = −100 μA; V$_{CC}$ = 1.65 V to 5.5 V	V$_{CC}$ − 0.1	-	-	V
		I$_O$ = −4 mA; V$_{CC}$ = 1.65 V	0.95	-	-	V
		I$_O$ = −8 mA; V$_{CC}$ = 2.3 V	1.7	-	-	V
		I$_O$ = −12 mA; V$_{CC}$ = 2.7 V	1.9	-	-	V
		I$_O$ = −24 mA; V$_{CC}$ = 3.0 V	2.0	-	-	V
		I$_O$ = −32 mA; V$_{CC}$ = 4.5 V	3.4	-	-	V
I$_I$	input leakage current	V$_I$ = 5.5 V or GND; V$_{CC}$ = 0 V to 5.5 V	-	-	±1	μA
I$_{OZ}$	OFF-state output current	V$_I$ = V$_{IH}$ or V$_{IL}$; V$_O$ = 5.5 V or GND; V$_{CC}$ = 3.6 V	-	-	±2	μA
I$_{OFF}$	power-off leakage current	V$_I$ or V$_O$ = 5.5 V; V$_{CC}$ = 0 V	-	-	±2	μA
I$_{CC}$	supply current	V$_I$ = 5.5 V or GND; I$_O$ = 0 A; V$_{CC}$ = 1.65 V to 5.5 V	-	-	4	μA
ΔI$_{CC}$	additional supply current	per pin; V$_I$ = V$_{CC}$ − 0.6 V; I$_O$ = 0 A; V$_{CC}$ = 2.3 V to 5.5 V	-	-	500	μA

[1] Typical values are measured at V$_{CC}$ = 3.3 V and T$_{amb}$ = 25 °C.

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11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 6.

Symbol	Parameter	Conditions		−40 °C to +85 °C			−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 4	[2]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.1	9.5	1.0	11.9	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	2.6	5.2	0.5	6.5	ns
		V_{CC} = 2.7 V		1.0	3.0	5.5	1.0	6.9	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.5	4.6	0.5	5.8	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.0	4.0	0.5	5.0	ns
t_{en}	enable time	nOE to nY; see Figure 5	[3]						
		V_{CC} = 1.65 V to 1.95 V		1.5	4.5	10.3	1.5	12.9	ns
		V_{CC} = 2.3 V to 2.7 V		1.0	2.9	5.6	1.0	7.0	ns
		V_{CC} = 2.7 V		1.5	3.4	5.6	1.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.5	4.7	0.5	5.9	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.0	3.8	0.5	4.8	ns
t_{dis}	disable time	nOE to nY; see Figure 5	[4]						
		V_{CC} = 1.65 V to 1.95 V		1.0	3.5	11.6	1.0	14.1	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	1.9	5.8	0.5	7.6	ns
		V_{CC} = 2.7 V		1.0	2.8	4.5	1.0	5.8	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.7	4.4	1.0	5.7	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	1.9	3.4	0.5	4.6	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[5]						
		output enabled		-	18	-	-	-	pF
		output disabled		-	5	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] t_{en} is the same as t_{PZH} and t_{PZL}

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

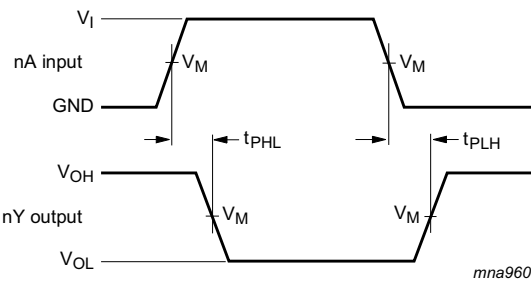f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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12. Waveforms

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

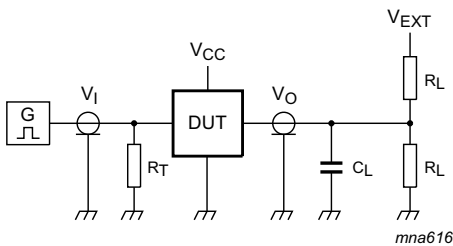**Fig 4.** The data input (nA) to output (nY) propagation delays
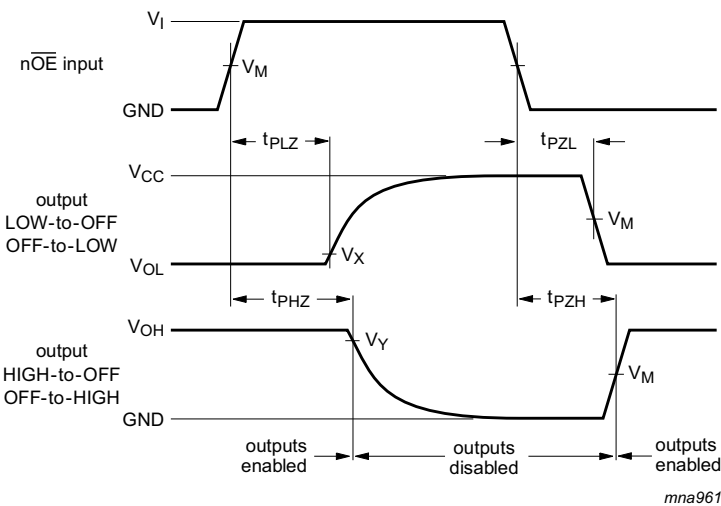
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. 3-state enable and disable times

Table 9.   Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V

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Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 6.   Test circuit for measuring switching times

Table 10.   Test data

Supply voltage	Input	Load		V_{EXT}		
	V_I	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm   **SOT505-2**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	HₑE	L	Lₚ	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

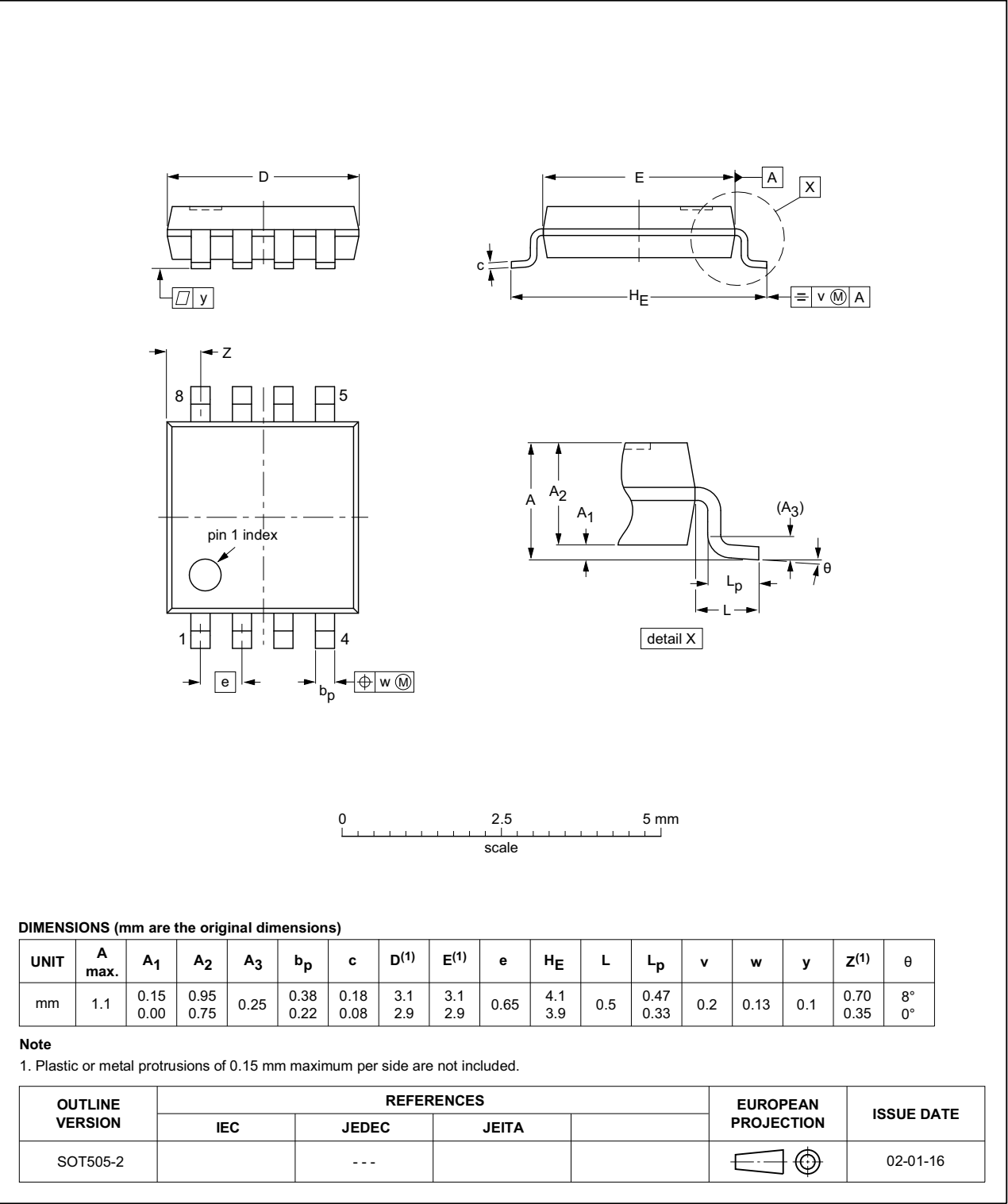| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 7.   Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

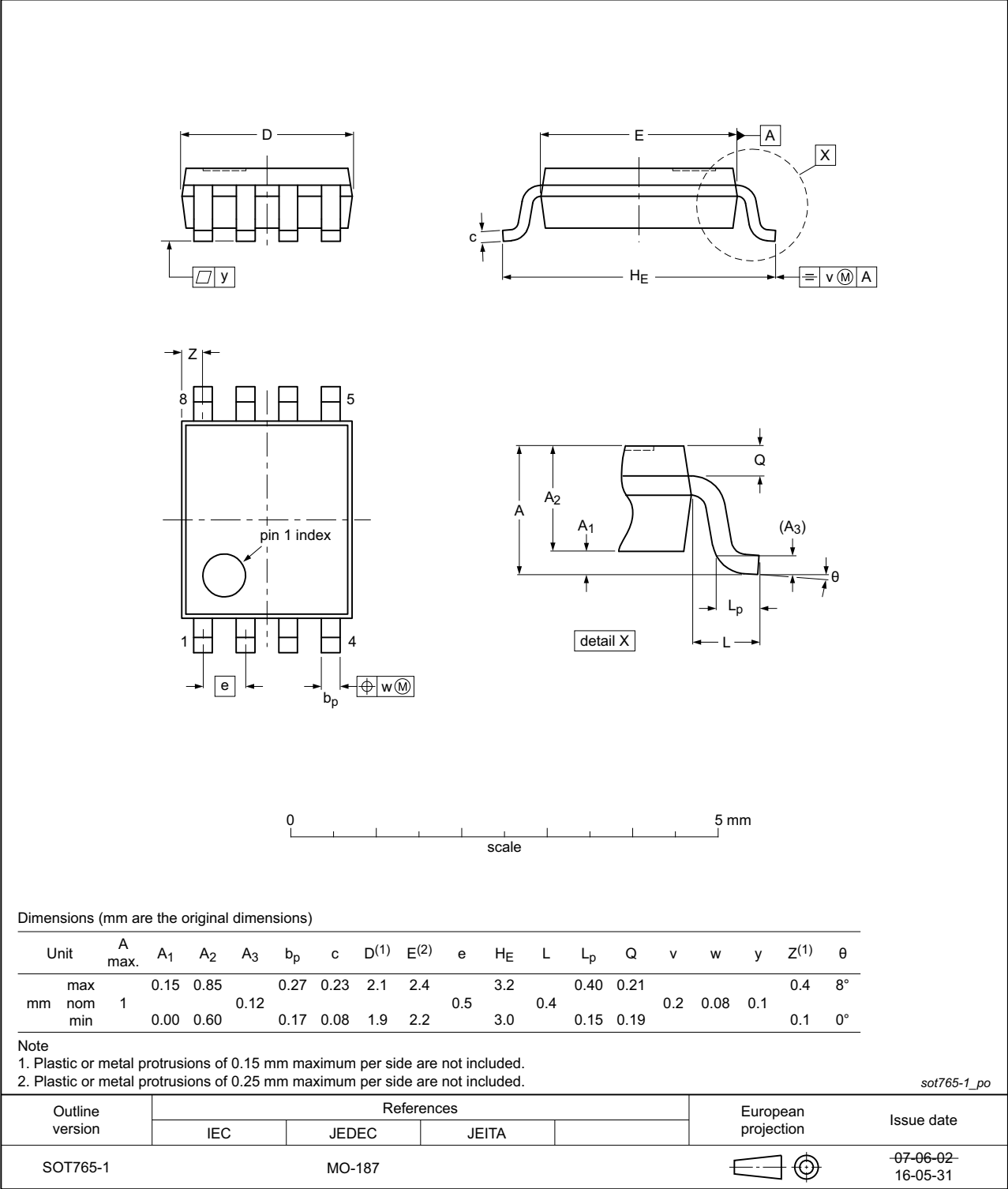Dimensions (mm are the original dimensions)

Unit	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D[1]	E[2]	e	H$_E$	L	L$_p$	Q	v	w	y	Z[1]	θ
	max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm	nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig 8.   Package outline SOT765-1 (VSSOP8)

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14. Abbreviations

Table 11.   Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G240_Q100 v.2	20161214	Product data sheet	-	74LVC2G240_Q100 v.1
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC2G240_Q100 v.1	20141015	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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