# **Quad 2-Input XOR Gate**

# With 5 V–Tolerant Inputs

The MC74LVX86 is an advanced high speed CMOS 2–input Exclusive–OR gate. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed:  $t_{PD} = 5.8 \text{ ns}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5 V (Max)$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

• These Devices are Pb-Free and are RoHS Compliant

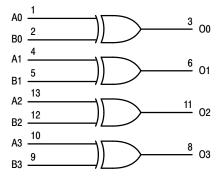


Figure 1. Logic Diagram

### PIN NAMES

Pins	Function
An, Bn	Data Inputs
On	Outputs

### **FUNCTION TABLE**

Inputs		Outputs
An	Bn	On
L	L	L
L	Н	Н
н	L	Н
н	Н	L



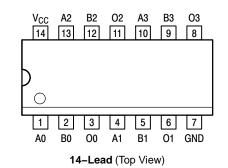
## **ON Semiconductor®**

http://onsemi.com

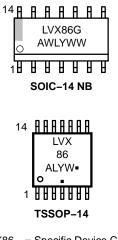


D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G





### MARKING DIAGRAMS



LVX86 = Specific Device Code A = Assembly Location WL, L = Wafer Lot Y = Year WW, W = Work Week G or • = Pb-Free Package

(Note: Microdot may be in either location)

### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	–0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, $V_{CC}$ and GND Pins	±50	mA
PD	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

			V <sub>cc</sub>		T <sub>A</sub> = 25°C	;	T <sub>A</sub> = -40	to 85°C	
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V <sub>OH</sub>	High–Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low–Level Output Voltage $(V_{in} = V_{IH} \text{ or } V_{IL})$	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4m A$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
l <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μΑ
I <sub>CC</sub>	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			2.0		20.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### **AC ELECTRICAL CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns)

					T <sub>A</sub> = 25°C		T <sub>A</sub> = -40	to 85°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Input to Output	V <sub>CC</sub> = 2.7V	$C_L = 15pF$ $C_L = 50pF$		7.5 10.0	14.5 18.0	1.0 1.0	17.5 21.0	ns
		$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		5.8 8.3	9.3 12.8	1.0 1.0	11.0 14.5	
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7V$ $V_{CC} = 3.3 \pm 0.3V$	$C_L = 50 pF$ $C_L = 50 pF$			1.5 1.5		1.5 1.5	ns

 Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

### **CAPACITIVE CHARACTERISTICS**

		T <sub>A</sub> = 25°C		$T_{A} = 25^{\circ}C$ $T_{A} = -4$		T <sub>A</sub> = -40	to 85°C	
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit	
Cin	Input Capacitance		4	10		10	pF	
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)		18				pF	

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per gate). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

		T <sub>A</sub> =	25°C	
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.5	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

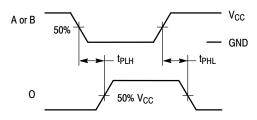
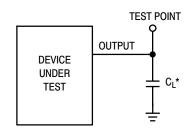


Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance

### Figure 3. Test Circuit

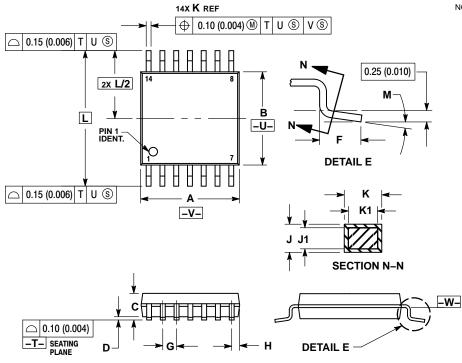
### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74LVX86DR2G	SOIC-14 NB (Pb-Free)	2500 Tape & Reel
MC74LVX86DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### PACKAGE DIMENSIONS

TSSOP-14 CASE 948G **ISSUE B** 

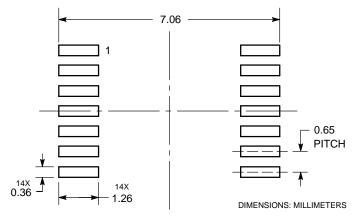


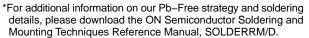
NOTES: 1. DIMENSIONING AND TOLERANCING PER

DIRENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER.
DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
TERERENCE ONLY.
DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.
MILLIMETERS INCHES

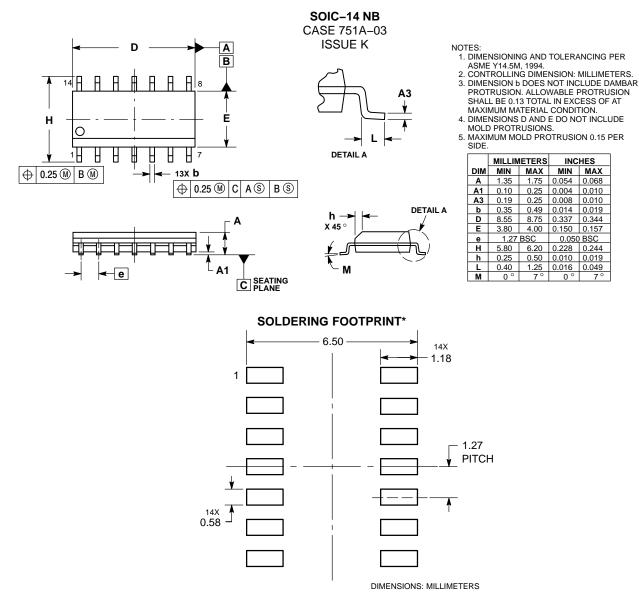
	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BS0		
М	0 °	° 8	0 °	8 °	

**SOLDERING FOOTPRINT\*** 





#### PACKAGE DIMENSIONS



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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