MAX14900E — Octal, High-Speed, Industrial, High-Side Switch

General Description

The MAX14900E is an octal power switch that features per-channel configuration for high-side or push-pull operation. Low propagation delay, high-rate load-switching makes the device suitable for next-generation high-speed PLC systems. Each high-side switch sources 850mA continuous current with a low 165mΩ (max) on-resistance at 500mA at T_A = +125°C. The high-side switches feature 2µs (max) input-to-output propagation delay when driving resistive loads. Long cables can be driven with switching rates of up to 100kHz for PWM/PPO control in push-pull operation. Multiple high-side switches can be connected in parallel to achieve higher drive currents. The device features a wide supply input range of 10V to 36V.

The MAX14900E is configured, monitored, and driven by an SPI and/or parallel interface. In parallel mode, eight logic inputs directly control the outputs and the serial interface can be used for configuration/monitoring. Serial mode utilizes the serial interface for both setting and configuration, and features CRC error detection to ensure robust SPI communication.

Current limiting and per-channel thermal shutdown protect each switch/driver. The device features a global diagnostics output as well as per-channel diagnostics and monitoring through the serial interface.

The MAX14900E is available in a 48-pin (7mm x 7mm) QFN-EP or standard 48-pin TQFN-EP package, and is specified over the -40°C to +125°C temperature range.

Applications

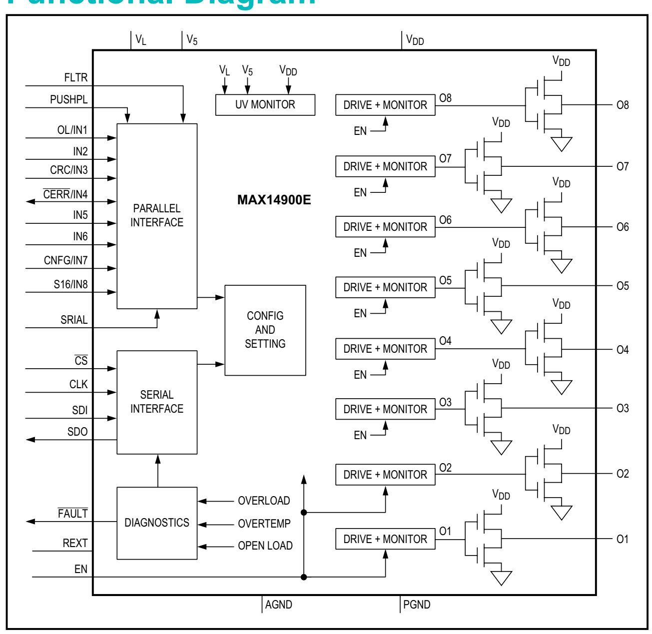
- Programmable Logic Controllers
- High-Density Digital Output Modules
- Motor Controllers
- PWM/PPO Control

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

Benefits and Features

- Low Power for High-Density Modules
  - 3mA (max) Total Supply Current
  - 165mΩ (max) High-Side R_{ON} at +125°C
- Fast Switching Ideal for Accurate, High-Speed Control Systems
  - 2µs Propagation Delays (High-Side Mode)
  - 0.8µs Propagation Delays (Push-Pull Mode)
  - 100kHz (max) Push-Pull Mode Switching Rate
- Extensive Fault Feedback Eases Maintenance and Reduces Installation Time
  - Global and Per-Channel Diagnostics
  - Open Load/Wire Detection
  - Thermal Shutdown Fault Indication
  - Output Logic State Feedback
  - Undervoltage Lockout
- Small Packages with Serial Interface Allows Making High-Density Modules
  - Daisy-Chainable SPI Minimizes Isolation Cost
  - 7mm x 7mm, 48-Pin QFN and TQFN Packages

Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to AGND = PGND.)
V_{DD} .... -0.3V to +40V
O_ .... -0.3V to (V_{DD} + 0.3V)
V_5, V_L, $\overline{FAULT}$, IN_, PUSHPL,
FLTR, SRIAL, CLK, SDI, $\overline{CS}$, EN .... -0.3V to +6V
REXT .... -0.3V to (V_5 + 0.3V)
SDO .... -0.3V to (V_L + 0.3V)
Continuous Reverse Current (O_) 2.0A
Inductive Kickback Current (O_) 1.9A
Continuous Current (Any Other Terminal) .... ±100mA
Continuous Power Dissipation (T_A = +70°C)
(derate 38.5mW/°C above +70°C) 4400mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... Internally Limited
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 18°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DD} = 10V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{DD} Supply Voltage	V_{DD}		10		36	V
V_{DD} Supply Current	I_{DD}	EN = high, O_ in push-pull mode and unloaded		0.7	1.5	mA
		EN = high, O_ in high-side mode and unloaded		0.7	1.5	
V_{DD} Disable Supply Current	I_{DD_DIS}	EN = low		0.7	1.5	mA
V_{DD} Undervoltage-Lockout Threshold	VDD_ UVLO	V_5 = 5V, V_{DD} rising	7.0	7.8	8.5	V
V_{DD} Undervoltage-Lockout Hysteresis	$V_{DD\_}$ UVHYS	V_5 = 5V		2.5		V
V_5 Supply Voltage	V_5		4.5		5.5	V
V_5 Supply Current	I_5	O_ in push-pull or high-side mode, $\overline{CS}$ = high, DC output		0.9	1.5	mA
V_5 Undervoltage-Lockout Threshold	V_{5_UVLO}	V_{DD} = 24V, V_5 rising	3.8	4	4.2	V
V_5 Undervoltage-Lockout Hysteresis	V_{5_UVHYS}	V_{DD} = 24V		0.3		V
V_5 POR Threshold	V_{5_POR}			1.6	2.4	V
V_L Supply Voltage	V_L		2.5		5.5	V
V_L Supply Current	I_L	Logic inputs unconnected		9	40	µA
V_L POR Threshold	V_{L_POR}			1.6	2.4	V

Electrical Characteristics (continued)

(V_{DD} = 10V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER OUTPUTS (O_)							
High-Side Mode On-Resistance	R_{ON_HS}	High-side mode, EN = high, O_ = high, $I_{O\_}$ = 500mA			85	165	mΩ
High-Side Mode Current Limit	I_{LIM_HS}	High-side mode, EN = high, O_ = high		1.4	1.7	2.0	A
High-Side Mode Leakage Current	I_{LKG_HS}	EN = low, $V_{O\_}$ = 0V		-1		+20	µA
Push-Pull Mode On-Resistance	R_{ON_PP}	Push-pull mode, EN = high	$I_{O\_}$ = +50mA, O_ = high		1.6	4	Ω
			$I_{O\_}$ = -50mA, O_ = low		5.2	10	
Push-Pull Current Limit	I_{LIM_PP}	Push-pull mode, EN = high, during blanking time	0V < $V_{O\_}$ < V_{DD} - 3V, O_ = high	200	500		mA
			3V < $V_{O\_}$ < V_{DD}, O_ = low	200	300		
Current-Limit Autoretry Blanking Time	t_{BLANK}	Push-pull mode, EN = high, O_ connected to V_{DD} or PGND			90		µs
Current-Limit Autoretry Off-Time	t_{RETRY}	Push-pull mode, EN = high, O_ connected to V_{DD} or PGND			11		ms
OPEN-LOAD DETECTION (O_)							
Open-Load Pullup Current	I_{OL}	High-side mode, O_ = off, 0V < $V_{O\_}$ < (V_{DD} – 2V), OL detect = on		65	80	110	µA
Open-Load and Status-Detect Threshold	$V_{TOL\_}$	EN = high, OL detect = on, high-side mode, O_ = off		6.3	7	7.7	V
LOGIC INPUTS (IN_, PUSHPL, FLTR, SRIAL, CLK, SDI, $\overline{\text{CS}}$, EN)							
Input Logic-High Voltage	V_{IH}			0.7 x V_L			V
Input Logic-Low Voltage	V_{IL}					0.3 x V_L	V
Input Threshold Hysteresis	V_{ITHYS}				0.1 x V_L		V
Input Pulldown/Pullup Resistor	R_{PULL}	(Note 3)		140	200	270	kΩ
LOGIC OUTPUTS ($\overline{\text{FAULT}}$, $\overline{\text{CERR}}$/IN4, SDO)							
Open-Drain Output Logic-Low Voltage	V_{ODL}	I_{SINK} = 5mA				0.33	V
Open-Drain Output Leakage Current	I_{LKG_OD}	SRIAL = high, output not asserted, V_{OUT} = 5.5V		-1		+1	µA
SDO Output Logic-High Voltage	V_{OH}	I_{SOURCE} = 5mA		V_L - 0.33			V
SDO Output Logic-Low Voltage	V_{OL}	I_{SINK} = 5mA				0.33	V
SDO Pulldown Resistor	R_{SDO}	$\overline{\text{CS}}$ = high		140	200	270	kΩ

Electrical Characteristics (continued)

(V_{DD} = 10V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
High-Side Mode LTH Output Propagation Delay	t_{PDHS_LH}	High-side mode, delay from IN_ transition (parallel mode) or $\overline{CS}$ rising-edge (serial mode) to O_ rising by 0.5V; R_L = 48Ω, C_L = 1nF, t_R/t_F ≤ 20ns, FLTR = low, Figure 1 (Note 4)		0.2	1	µs
High-Side Mode HTL Output Propagation Delay	t_{PDHS_HL}	High-side mode, delay from IN_ transition (parallel mode) or $\overline{CS}$ rising-edge (serial mode) to O_ falling by 0.5V, R_L = 48Ω, C_L = 1nF, t_R/t_F ≤ 20ns, FLTR = low, Figure 1 (Note 4)		0.9	2	µs
Push-Pull Output LTH Propagation Delay	t_{PDPP_LH}	Push-pull mode, delay from IN_ transition (parallel mode) or $\overline{CS}$ rising-edge (serial mode) to O_ settling to within 0.8 x V_{DD}, R_L = 5kΩ, C_L = 1nF, FLTR = low, Figure 2		0.3	0.7	µs
Push-Pull Output HTL Propagation Delay	t_{PDPP_HL}	Push-pull mode, delay from IN_ transition (parallel mode) or $\overline{CS}$ rising-edge (serial mode) to O_ settling to within 0.2 x V_{DD}, R_L = 5kΩ, C_L = 1nF, FLTR = low, Figure 2		0.3	0.8	µs
Output Rise and Fall Time	t_R, t_F	High-side mode, 20% to 80%, R_L = 48Ω, C_L = 1nF, Figure 1		1.5	4	µs
		Push-pull mode, 20% to 80%, R_L = 5kΩ, C_L = 1nF, Figure 2		0.1	0.4	
		Push-pull mode, 20% to 80%, R_L = 240Ω, V_{CC} = 24V, C_L = 1nF, Figure 2		0.1	0.4	
Output Switching Rate	f_O	Push-pull mode, R_L = 5kΩ or I_L = 100mA to ground, C_L = 1nF, SRIAL = low			100	kHz
Channel-to-Channel Skew	t_{PDSK_LH}, t_{PDSK_HL}	Push-pull mode, Figure 2 (Note 5)	-100		+100	ns
CRC Error-Detect Propagation Delay	t_{PDL_CERR}	Error detected on SDI data, from $\overline{CS}$ rising-edge to $\overline{CERR}$/IN4 falling-edge; I_{SOURCE} = 5mA, Figure 3		14.5	30	ns
CRC Error-Clear Propagation Delay	t_{PDH_CERR}	Error cleared, from $\overline{CS}$ rising-edge to $\overline{CERR}$/IN4 rising, I_{SOURCE} = 5mA, Figure 3		17	40	ns
Pulse Length of Rejected Glitch	t_{GL}	FLTR = high	0		80	ns
Admitted Pulse Length		FLTR = high	300			ns
Glitch Filter Propagation Delay Time	t_{PDGF}	FLTR = high		140	300	ns

Electrical Characteristics (continued)

(V_{DD} = 10V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING CHARACTERISTICS (Figure 4)						
CLK Clock Period	t_{CH+CL}		50			ns
CLK Pulse-Width High	t_{CH}		5			ns
CLK Pulse-Width Low	t_{CL}		5			ns
$\overline{CS}$ Fall-to-CLK Rise Time	t_{CSS}	FLTR = low (Note 4)	5			ns
		FLTR = high	300			
SDI Hold Time	t_{DH}		5			ns
SDI Setup Time	t_{DS}		5			ns
Output Data Propagation Delay	t_{DO}	C_L = 10pF. CLK falling-edge to SDO stable			25	ns
SDO Rise and Fall Times	t_{FT}	C_L = 10pF		4		ns
$\overline{CS}$ Hold Time	t_{CSH}	(Note 4)	50			ns
$\overline{CS}$ Pulse-Width High	t_{CSPW}	FLTR = low (Note 4)	50			ns
		FLTR = high	280			
PROTECTION SPECIFICATIONS						
Channel Thermal-Shutdown Threshold	T_{C_SD}	Temperature rising		+170		°C
Thermal-Shutdown Hysteresis	$T_{C\_SD\_HYS}$			15		°C
Global Thermal-Shutdown Threshold	T_{G_SD}	Temperature rising		150		°C
Global Thermal-Shutdown Hysteresis	$T_{G\_SD\_HYS}$			10		°C
ESD Protection	V_{ESD}	O_ pins, Human Body Model (Note 6)		±15		kV
		All other pins, Human Body Model		±2		

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: All logic input pins except $\overline{CS}$ have a pulldown resistor. $\overline{CS}$ has a pullup resistor.
Note 4: Specifications are guaranteed by design; not production tested.
Note 5: Channel-to-channel skew is defined as the difference in propagation delays between channels on the same device with the same polarity.
Note 6: Bypass V_{DD} pins to AGND with a 1μF capacitor as close as possible to the device for high-ESD protection.

Test Circuits/Timing Diagrams

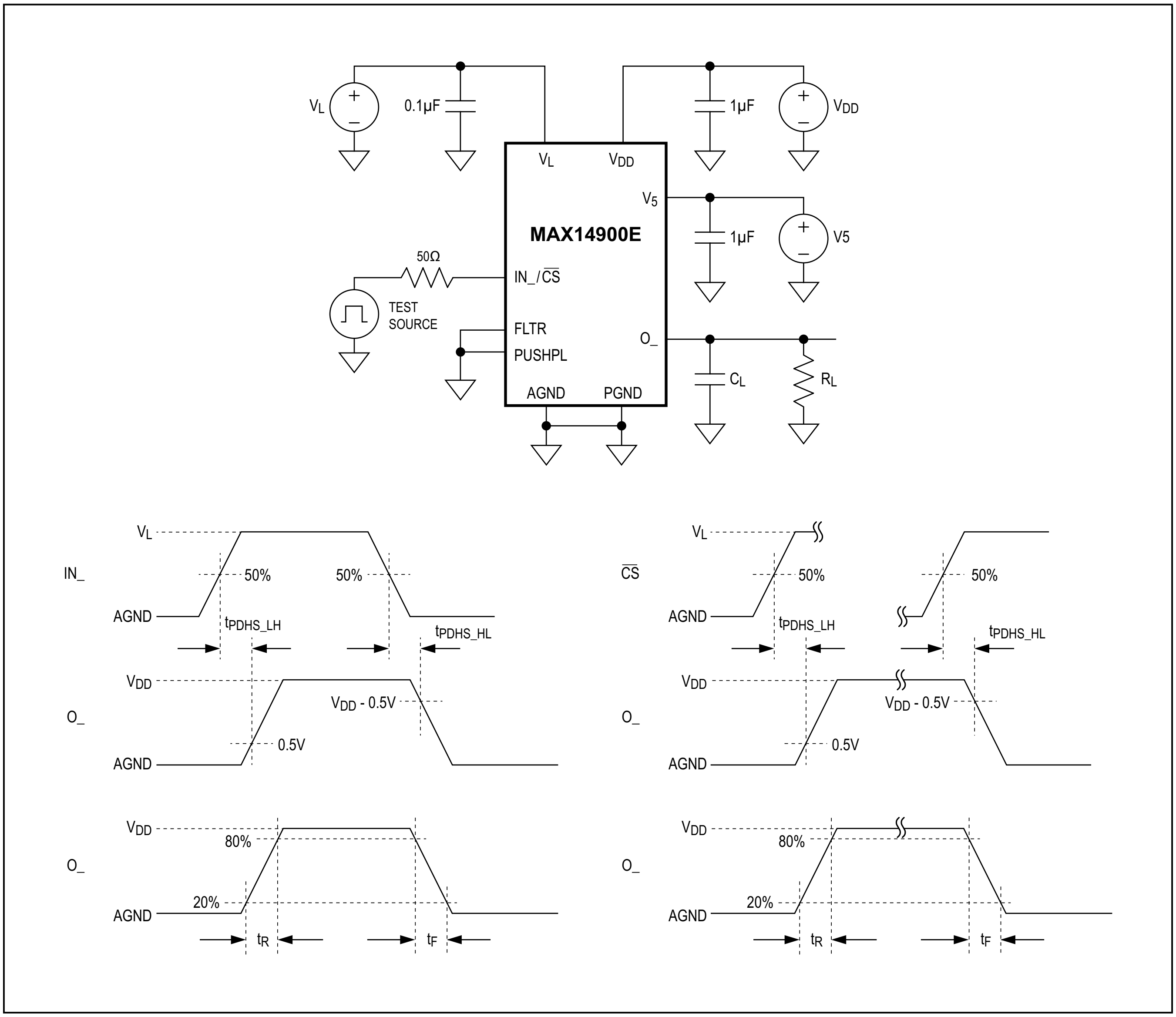


Figure 1. High-Side Mode Timing Characteristics

Test Circuits/Timing Diagrams (continued)

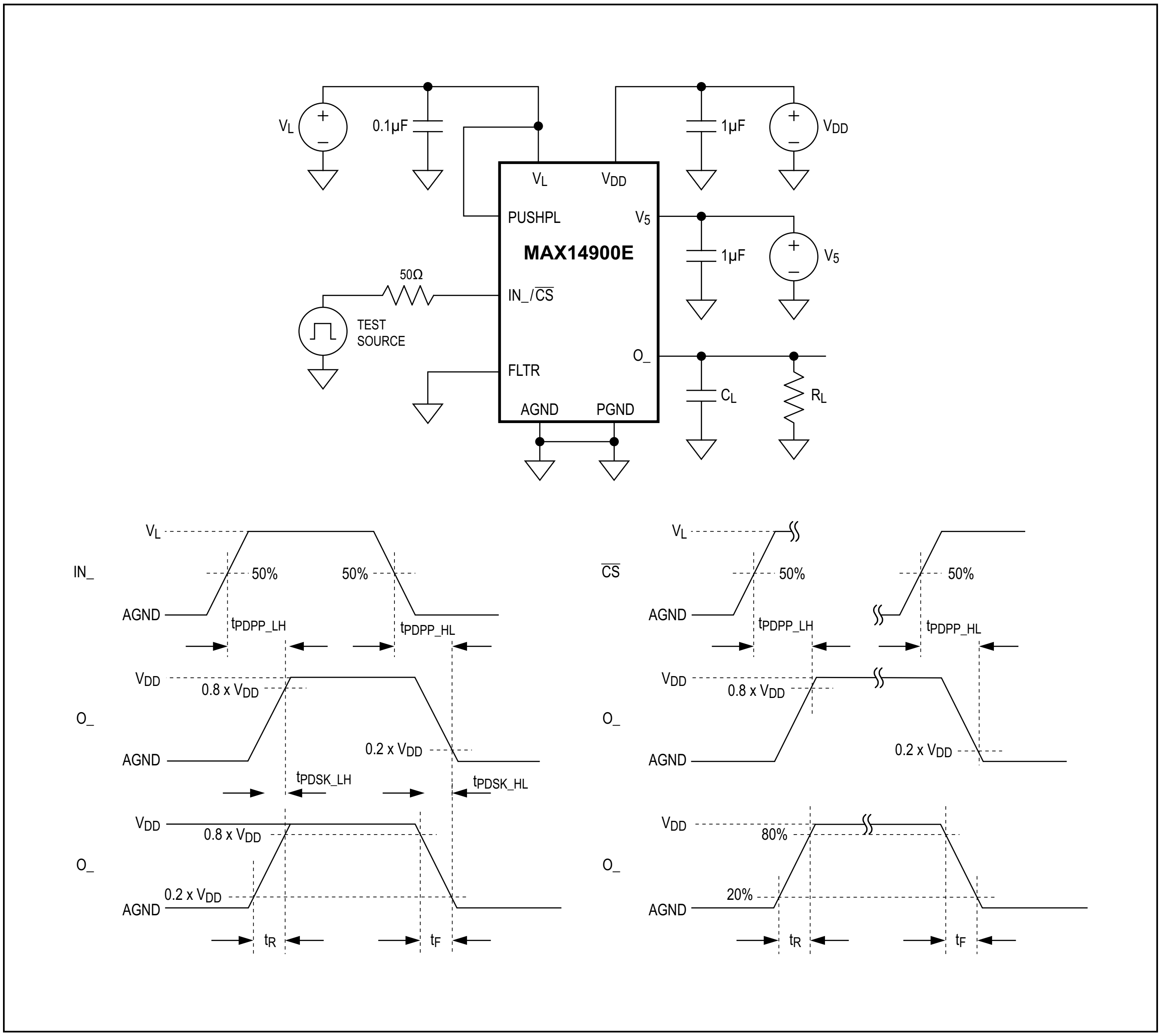


Figure 2. Push-Pull Mode Timing Characteristics

Test Circuits/Timing Diagrams (continued)

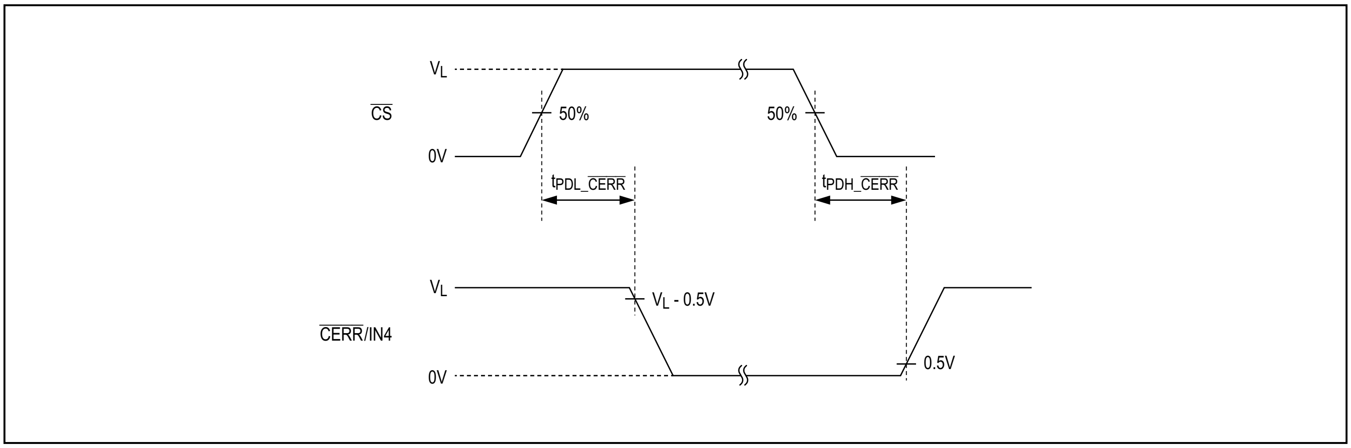


Figure 3. CRC Error Detection Timing

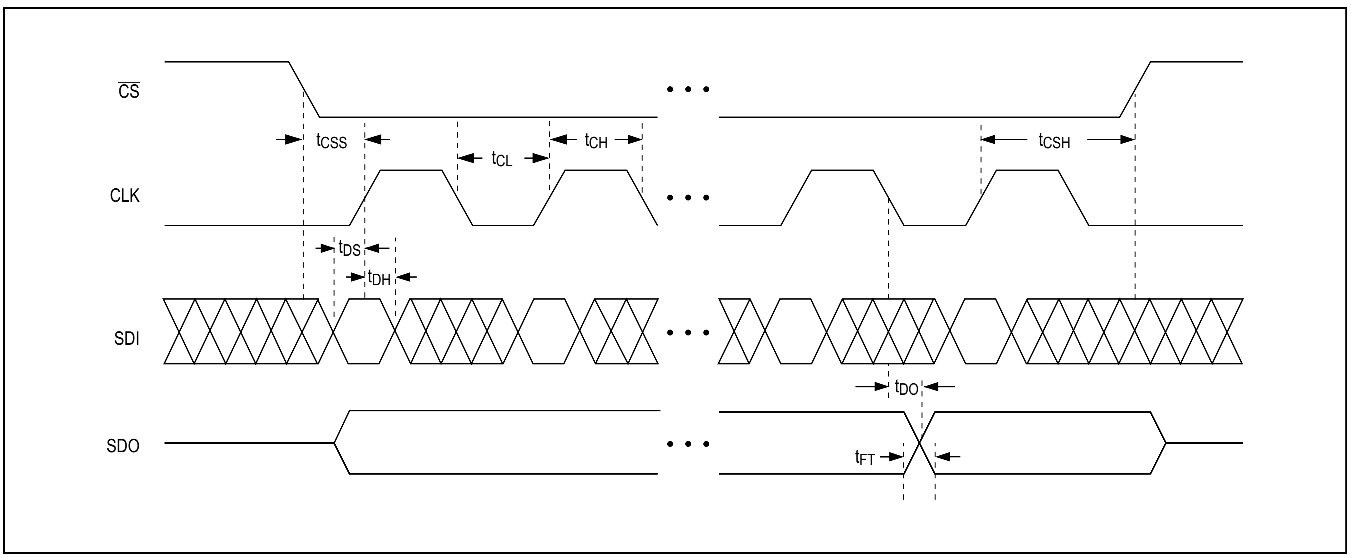
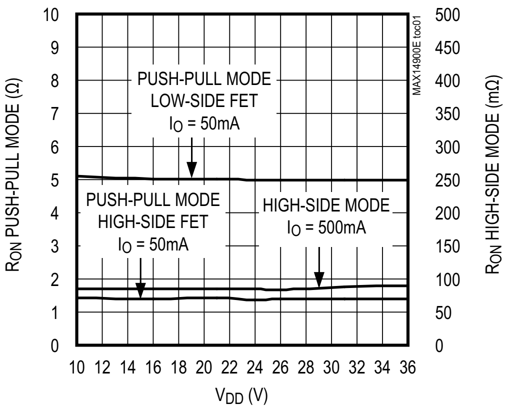


Figure 4. SPI Timing Diagram

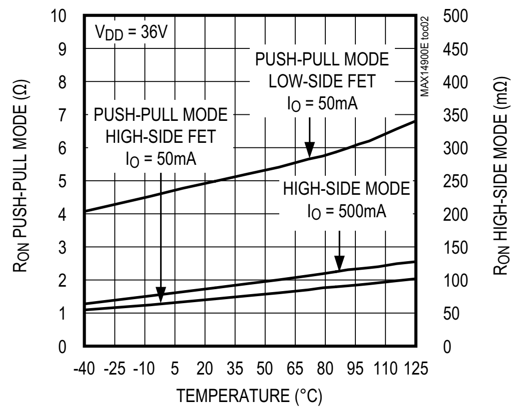
Typical Operating Characteristics

(V_{DD} = +24V, V_5 = V_L = 5.0V, T_A = +25°C, unless otherwise noted.)

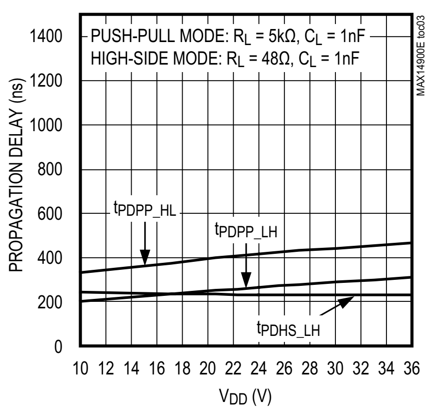
R_{ON} vs. V_{DD}



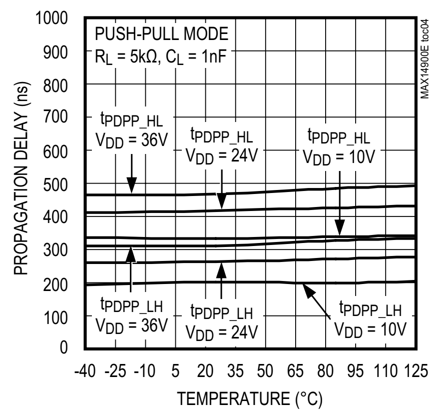
R_{ON} vs. TEMPERATURE



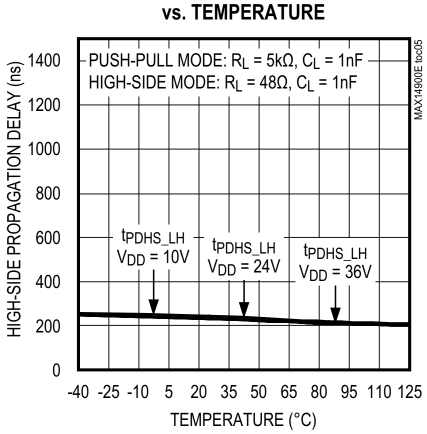
PROPAGATION DELAY vs. V_{DD}



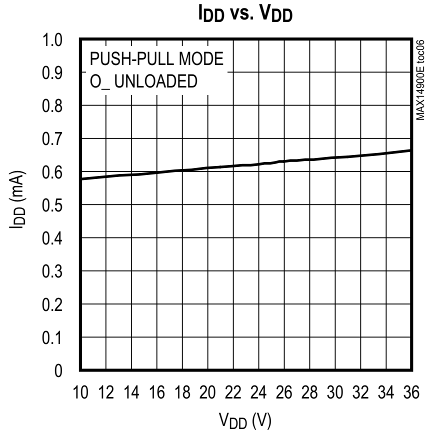
PUSH-PULL PROPAGATION DELAY vs. TEMPERATURE



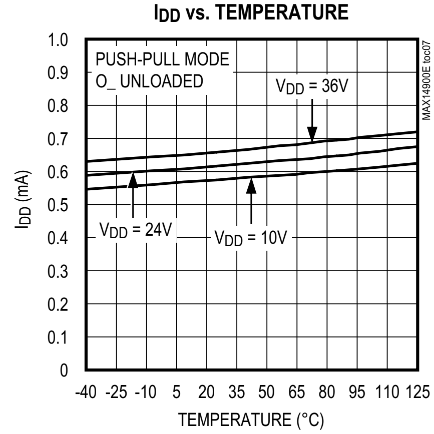
HIGH-SIDE PROPAGATION DELAY vs. TEMPERATURE



I_{DD} vs. V_{DD}

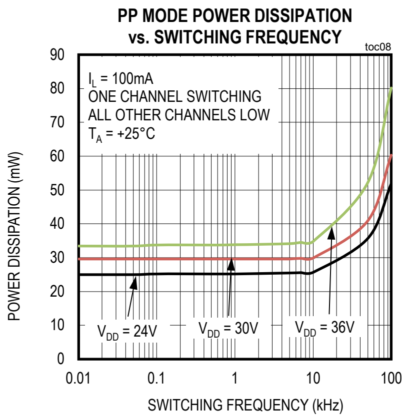


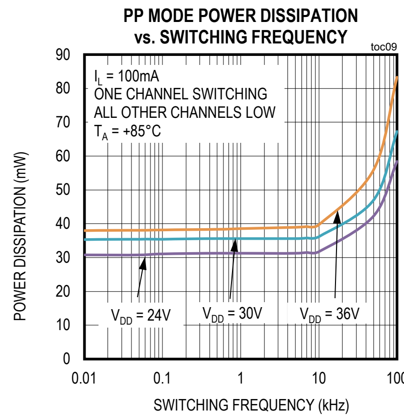
I_{DD} vs. TEMPERATURE

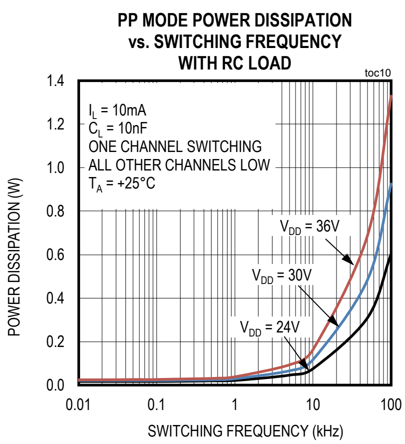


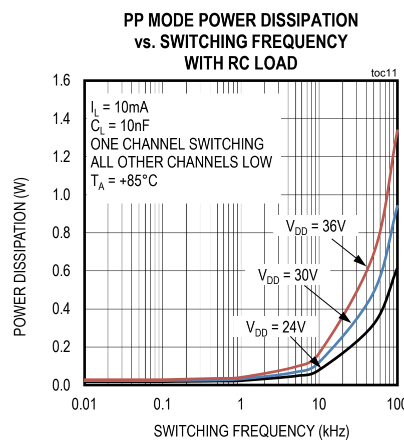
Typical Operating Characteristics (continued)

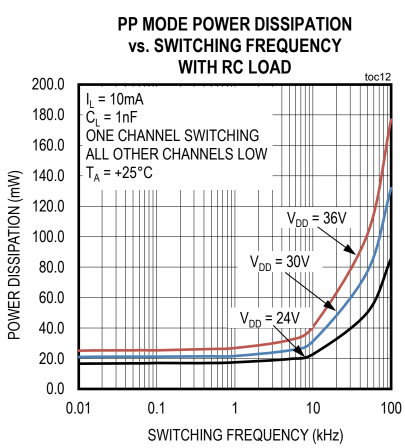
(V_{DD} = +24V, V_5 = V_L = 5.0V, T_A = +25°C, unless otherwise noted.)

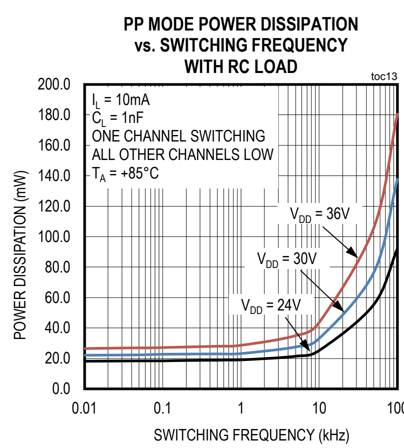




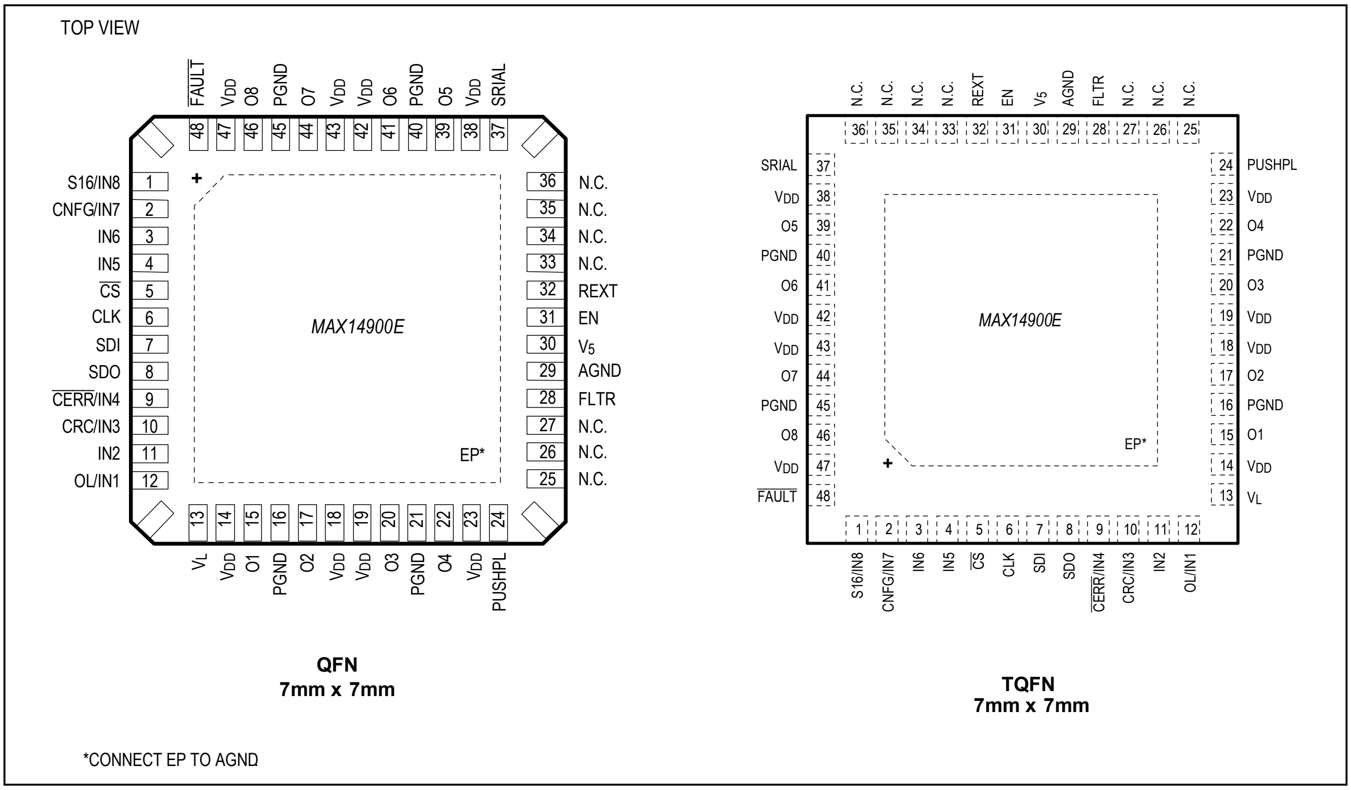








Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	S16/IN8	16-Bit Serial-Select Input/IN8 Input. In serial mode (SRIAL = high), drive S16/IN8 high to select 16-bit serial operation. Drive S16/IN8 low to select 8-bit serial operation. In parallel mode (SRIAL = low), S16/IN8 sets the O8 output on/off in high-side mode or high/low in push-pull mode. S16/IN8 has an internal 200kΩ pulldown resistor.
2	CNFG/IN7	Configure Select Input/IN7 Input. In serial mode (SRIAL = high), drive CNFG/IN7 high to select per-channel configuration over the serial interface. Drive CNFG/IN7 low to select setting the O_ outputs over the serial interface. In parallel mode (SRIAL = low), CNFG/IN7 sets the O7 output on/off in high-side mode or high/low in push-pull mode. CNFG/IN7 has an internal 200kΩ pulldown resistor.
3	IN6	IN6 Input. In parallel mode (SRIAL = low), IN6 sets the O6 output on/off in high-side mode or high/low in push-pull mode. IN6 has an internal 200kΩ pulldown resistor.
4	IN5	IN5 Input. In parallel mode (SRIAL = low), IN5 sets the O5 output on/off in high-side mode or high/low in push-pull mode. IN5 has an internal 200kΩ pulldown resistor.
5	$\overline{CS}$	SPI Chip-Select Input. $\overline{CS}$ is the SPI active-low chip select. $\overline{CS}$ has an internal 200kΩ pullup resistor.
6	CLK	Serial-Clock Input. CLK is the SPI serial-clock input (up to 20MHz) and has an internal 200kΩ pulldown resistor.
7	SDI	Serial-Data Input. SDI is the SPI serial-data input and has an internal 200kΩ pulldown resistor.
8	SDO	Serial-Data Output. SDO is the SPI serial-data output. SDO has an internal 200kΩ pulldown resistor when $\overline{CS}$ is logic-high.

Pin Description (continued)

PIN	NAME	FUNCTION
9	$\overline{\text{CERR}}$/IN4	CRC Error Detection Output/IN4 Input. In serial mode (SRIAL = high) with error checking enabled (CRC/IN3 = high), $\overline{\text{CERR}}$/IN4 is an active-low open-drain output that asserts when a CRC error is detected on SDI data. In parallel mode (SRIAL = low), $\overline{\text{CERR}}$/IN4 sets the O4 output on/off in high-side mode or high/low in push-pull mode. $\overline{\text{CERR}}$/IN4 has an internal 200kΩ pulldown resistor when SRIAL = 0.
10	CRC/IN3	CRC Enable Input/IN3 Input. In serial mode (SRIAL = high), drive CRC/IN3 high to enable CRC generation/error detection on SPI data. In parallel mode (SRIAL = low), CRC/IN3 sets the O3 output on/off in high-side mode or high/low in push-pull mode. CRC/IN3 has an internal 200kΩ pulldown resistor.
11	IN2	IN2 Input. In parallel mode (SRIAL = low), IN2 sets the O2 output on/off in high-side mode or high/low in push-pull mode. IN2 has an internal 200kΩ pulldown resistor.
12	OL/IN1	Open-Load Enable Input/IN1 Input. In serial mode (SRIAL = high), drive OL/IN1 high to enable open-load detection on all eight O_ outputs that are configured in high-side mode, overriding the serial configuration. Drive OL/IN1 low to disable open-load detection unless enabled by the serial interface. In parallel mode (SRIAL = low), OL/IN1 sets the O1 output on/off in high-side mode or high/low in push-pull mode. OL/IN1 has a 200kΩ pulldown resistor that is always connected.
13	V_L	Logic Supply Input. V_L defines the logic levels on all I/O logic interface pins from 2.5V to 5.5V. Bypass V_L to AGND with a 0.1µF ceramic capacitor as close as possible to the device.
14, 18, 19, 23, 38, 42, 43, 47	V_{DD}	Supply Voltage Input. V_{DD} supply is 10V to 36V. Bypass the V_{DD} pins to a ground plane with a 1µF ceramic capacitor. Externally connect all V_{DD} pins and ensure that the maximum trace resistance between each V_{DD} pin is less than 10mΩ.
15	O1	Driver Output 1. May be configured as a high-side switch or push-pull output.
16, 21, 40, 45	PGND	Power Ground. Connect PGND to the ground plane.
17	O2	Driver Output 2. May be configured as a high-side switch or push-pull output.
20	O3	Driver Output 3. May be configured as a high-side switch or push-pull output.
22	O4	Driver Output 4. May be configured as a high-side switch or push-pull output.
24	PUSHPL	Global Push-Pull/High-Side Select Input. In parallel mode (SRIAL = low), drive PUSHPL high to globally configure all O_ outputs to operate in push-pull mode, overriding the serial configuration. Drive PUSHPL low to configure all O_ outputs to operate in high-side mode unless configured as push-pull by the serial interface. PUSHPL has an internal 200kΩ pulldown resistor.
25–27, 33–36	N.C.	No Connection. Not internally connected.
28	FLTR	Glitch Filter Enable Input. Set FLTR high to enable glitch filtering on every logic input except SDI and CLK. FLTR has an internal 200kΩ pulldown resistor.
29	AGND	Analog Ground. Connect AGND to the ground plane.
30	V_5	5V Supply Input. Bypass V_5 to AGND with a 1µF ceramic capacitor as close as possible to the device.
31	EN	Enable Input. Drive EN high to enable normal operation for all O_ outputs. Drive EN low to force all O_ outputs into high-impedance mode. EN has an internal 200kΩ pulldown resistor.
32	REXT	External Resistor Connection. Connect a 56kΩ ±1% resistor from REXT to AGND.

Pin Description (continued)

PIN	NAME	FUNCTION
37	SRIAL	Serial/Parallel Select Input. Drive SRIAL high to set and configure the O_ outputs through the serial interface. Drive SRIAL low to set the O_ outputs through the parallel (IN_) pins. SRIAL does not affect the read back of diagnostics/status information through the serial interface. SRIAL has an internal 200kΩ pulldown resistor.
39	O5	Driver Output 5. May be configured as a high-side switch or push-pull output.
41	O6	Driver Output 6. May be configured as a high-side switch or push-pull output.
44	O7	Driver Output 7. May be configured as a high-side switch or push-pull output.
46	O8	Driver Output 8. May be configured as a high-side switch or push-pull output.
48	$\overline{\text{FAULT}}$	Global Fault Output. $\overline{\text{FAULT}}$ is an open-drain, active-low output that asserts when a fault condition (thermal shutdown, open-load, and/or overload protection) is detected on any O_ output.
—	EP	Exposed Pad. Connect EP to a large ground plane, which is electrically connected to PGND, using a via farm to minimize thermal impedance; not intended as an electrical connection point.

Functional Diagram

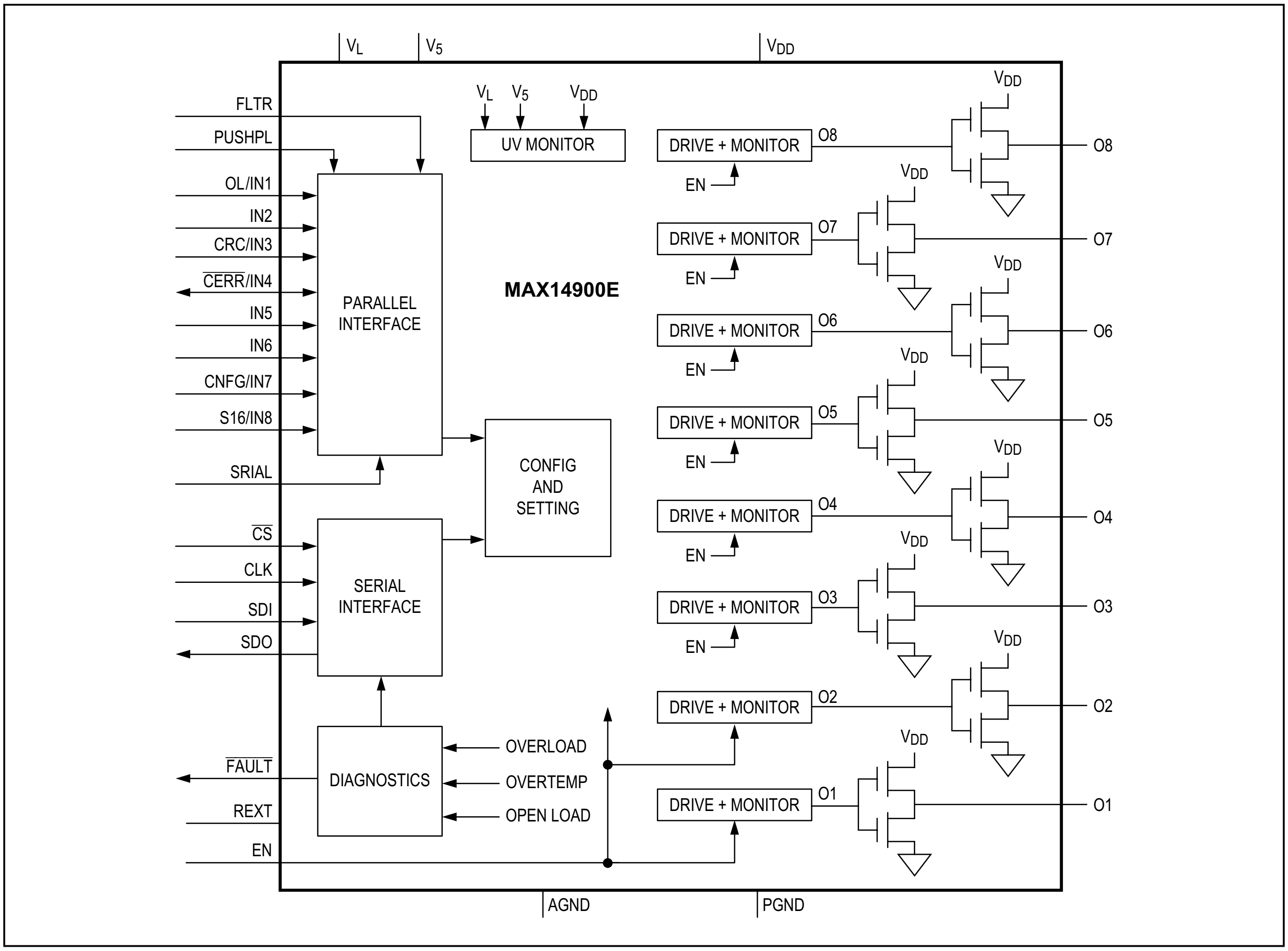


Table 1. Serial/Parallel Operating Modes

OPERATING MODE	SRIAL	S16/IN8	CNFG/ IN7	SDI DATA		SDO DATA	
				SETTING	CONFIG	FAULT	STATUS
Parallel mode with optional SPI configuration, diagnostics, and monitoring	0	X	X	N/A	16-bit	8-bit	8-bit
8-bit serial mode with SPI setting and diagnostics	1	0	0	8-bit	N/A	8-bit	N/A
8-bit serial mode with SPI configuration and diagnostics	1	0	1	N/A	8-bit	8-bit	N/A
16-bit serial mode with SPI setting, configuration, diagnostics, and monitoring	1	1	0	8-bit	8-bit	8-bit	8-bit
16-bit serial mode with SPI configuration, diagnostics, and monitoring	1	1	1	N/A	16-bit	8-bit	8-bit

X = Don't care

Detailed Description

The MAX14900E is an octal low-propagation delay 850mA high-side switch that can be operated as a push-pull driver with high switching-rate capability. Each channel can be configured to operate in high-side or push-pull mode. Push-pull mode drives capacitive loads such as long cables that need to be driven at high switching rates. In high-side mode, each channel switches up to 850mA load current with 165mΩ (max) on-resistance.

The MAX14900E's switches/drivers are configured either individually by a serial SPI interface and/or globally by a parallel interface. In parallel operating mode (SRIAL = low), the IN_ inputs directly control the O_ outputs and the SPI interface configures each channel and reads back diagnostic and state status. In serial operating mode (SRIAL = high), the SPI interface is used to configure and set the state of each channel while the parallel inputs provide optional configuration possibilities.

Current limiting, overload protection, and thermal shutdown circuitry protect each switch/driver. The device features per-channel diagnostic detection that feeds back per-channel thermal shutdown and output state information. In high-side mode, multiple channels can be connected in parallel to achieve higher load currents.

Serial/Parallel Operating Modes

A serial SPI and parallel interface allow configuration, monitoring, and driving of the MAX14900E. The serial interface supports per-channel configuration, setting, and diagnostics/monitoring while the parallel interface allows direct driving of the switches/outputs. Table 1 details how the device utilizes each interface depending on the status of the configuration select inputs.

Table 2. Parallel Driving Truth Table

IN_	O_ STATE	
	PUSH-PULL	HIGH-SIDE
0	Low	Off
1	High	On

Parallel Operating Mode

In parallel operating mode (SRIAL = low), the eight IN_ inputs directly set the O_ switches on/off in high-side mode or high/low in push-pull mode (Table 2). The serial interface can optionally be used to configure each output as a high-side switch or as a push-pull driver and to enable open-load detection for each high-side switch. The serial interface can also be used in parallel mode to read out per-channel fault, open-load detection, and output logic state information.

The outputs can be configured globally for push-pull operation by the PUSHPL input. Global diagnostic fault and open-load information is reported by the $\overline{\text{FAULT}}$ output.

Serial Operating Mode

In serial operating mode (SRIAL = high), the switches/drivers are set, configured, and monitored by the SPI interface. The S16/IN8, CNFG/IN7, CRC/IN3, and OL/IN1 inputs and the $\overline{\text{CERR}}$/IN4 output provide further configuration and monitoring options in serial operating mode. The remaining IN_ inputs are not used. See the *Serial Controller Interface* section for more information.

Configuration

The global configuration inputs affect all eight O_ channels while serial configuration is per channel. See Table 3.

The serial interface can be used to configure each output individually to be in push-pull or high-side mode and to enable open-load detection for that channel if it is in high-side mode. The PUSHPL and OL/IN1 inputs override the per-channel serial configuration when they are set high.

Output Drivers

The drivers can be configured for high-side or push-pull operation. When configured in high-side mode, each driver can safely source 850mA (max) load current continuously. The high-side switches have active current limiting in the range between 1.4A (min) and 2.0A (max).

When a driver is in push-pull mode, the output drives resistive/capacitive loads at high switching rates with load currents up to 100mA to ground. The R_{ON} is 4Ω (max) for the high-side and 10Ω (max) for the low-side drivers in push-pull mode.

Monitoring the Output Logic State

The voltage state of each O_ driver/switch can be read out via SPI. If the voltage on an O_ output is higher than the 7V (typ) threshold, then the corresponding S_ bit is logic 1 in the status byte. If the voltage on an O_ output is below the threshold, then the corresponding S_ bit is logic 0. Status monitoring can be read out via 16-bit serial mode. This is possible on all modes and states of the outputs: on/off/high/low.

Open-Load Detection

When configured in high-side mode, the device can detect when no load is connected to the O_ outputs or when a wire to a load is open circuit. Open-load detection can be globally enabled in serial mode via the OL/IN1 input, or on a per-channel basis via the serial interface in parallel and serial modes. The detection circuitry applies an 80µA current to the load and monitors the O_ voltage. Open-load detection occurs when the outputs are configured in high-side mode and is active while the high-side driver is off.

When an open-load condition is detected on a high-side switch, the corresponding switch's fault bit is set and the global $\overline{\text{FAULT}}$ output is asserted. Turning off a high-side driver that has a large capacitive load and low bleed resistance triggers a temporary detection of an open-load condition and assert $\overline{\text{FAULT}}$ until the O_ voltage decays to below the 7V (typ) threshold.

Table 3. Global Configuration Inputs

INPUT	SRIAL	CONFIGURATION FUNCTION
FLTR	X	Enables anti-glitch filtering on all logic input pins except SDI and CLK 0 = Glitch filtering disabled 1 = Glitch filtering enabled
PUSHPL	X	Configures all O_ outputs as push-pull or high-side 0 = All drivers high-side mode unless configured as push-pull by serial interface 1 = All drivers push-pull mode
EN	X	Enables normal operation of all O_ outputs 0 = All O_ outputs high impedance 1 = Normal operation
OL/IN1	1	Enables global open-load detection in serial mode 0 = Open-load detection disabled unless enabled by serial interface 1 = Open-load detection enabled for all high-side mode switches
CRC/IN3	1	Enables CRC generation and error detection of SPI data 0 = CRC disabled 1 = CRC enabled

X = Don't care

Thermal Shutdown Protection

Thermal overload circuitry constantly monitors each switch/driver and a global thermal shutdown circuit monitors average chip temperature. When a local thermal shutdown condition occurs for one of the drivers, it is disabled while the others continue to operate. When the local temperature falls to below the activation threshold (T_{C_SD} – $T_{C\_SD\_HYS}$), that driver automatically re-enables. A global thermal shutdown does not disable the O_ outputs but prevents any channel from re-enabling itself until the global temperature sensor is below the limit.

The $\overline{\text{FAULT}}$ output is asserted when any thermal shutdown condition occurs. In addition, F_ bits are set for channels that are in thermal shutdown in the SPI SDO data.

Overload and Short-Circuit Protection

The device protects each O_ output against overload and short-circuit conditions while operating in push-pull and high-side mode.

In high-side mode, the device actively limits each channel's output current to 1.7A. As long as no thermal shutdown occurs, this current limiting condition persists continuously.

In push-pull mode, the device limits the load current to 300mA/500mA (typ). Overload faults are detected when an O_ output is in push-pull mode and an overcurrent condition forces the output voltage to above 1V (for O_ = low) or below (V_{DD} - 1V) (for O_ = high) for more than the blanking time 90µs (typ). When the cause of the output voltage level mismatch is removed, the driver resumes normal operation.

POR and UVLO Conditions

The MAX14900E features undervoltage lockout (UVLO) and power-on reset (POR) circuitry on its power supply inputs to ensure that the device is in a known state on power-up or when there is a droop on one of the supplies. If either V_L or V_5 falls to below its POR threshold, the device goes into its reset state and all configuration settings are lost.

When V_{DD} or V_5 is below its UVLO threshold, all O_ outputs are disabled and the 80µA open-load detection current sources are turned off. The device resumes normal operation when the UVLO condition is removed. As long as V_L and V_5 stay above their POR thresholds, the SPI interface remains active and configuration settings are not affected.

In 16-bit serial mode when a UVLO is present, a series of all ones in the serial SDO status/fault read back bits reports this condition.

$\overline{\text{FAULT}}$ Output

The global $\overline{\text{FAULT}}$ output asserts when a fault condition is detected on any O_ output. The types of fault conditions reported by $\overline{\text{FAULT}}$ are thermal shutdown, open-load (if enabled), and overload protection (in push-pull mode only). The global $\overline{\text{FAULT}}$ is not initiated in a UVLO condition.

Thermal shutdown faults are detected when the internal temperature of any driver exceeds the thermal shutdown threshold (T_{C_SD}). The fault is cleared when the temperature falls to below the activation threshold (T_{C_SD} – $T_{C\_SD\_HYS}$).

Open-load faults are detected when the voltage at an O_ output in high-side mode with the HS switch turned off is above the detection threshold of 7V. This happens when the O_ output is not connected to any external load and the 80µA pullup current charges the node. A brief open-load condition can occur after an HS switch is turned off and the load has not discharged capacitance yet.

In push-pull mode, if the voltage level at an O_ output differs from the programmed value for longer than the 90µs (typ) blanking time due to overcurrent, the driver is turned off for the 11ms (typ) retry time. During the retry period, the $\overline{\text{FAULT}}$ output is asserted and the fault bit is set for that driver in the serial data. The fault is cleared after the fault condition is removed at the end of the current retry period (11ms).

Serial Controller Interface

The MAX14900E can be configured, controlled and/or monitored on a per-channel basis via its SPI interface (see Table 1). Daisy-chaining multiple MAX14900E devices is supported to reduce the required number of $\overline{CS}$ and/or isolator pins. Figure 5 shows an example of daisy-chaining two MAX14900E devices. Daisy-chaining operates both with 8-bit and 16-bit serial data: S16/IN8 = X.

The MAX14900E uses SPI mode 0 with CPOL = 0 and CPHA = 0. When the $\overline{CS}$ input transitions low, diagnostics and status information is sampled and stored in the internal SPI shift register and the SDO output becomes active. This data is clocked out of SDO on each falling CLK edge while new SDI data is sampled and stored in the shift register on each rising CLK edge. When $\overline{CS}$ transitions high at the end of the SPI cycle, the current data in the SPI shift register is latched into the MAX14900E and the new configuration and/or setting data changes the driver states. Figure 6 illustrates the sampling of internal signals dependent on $\overline{CS}$ transitions.

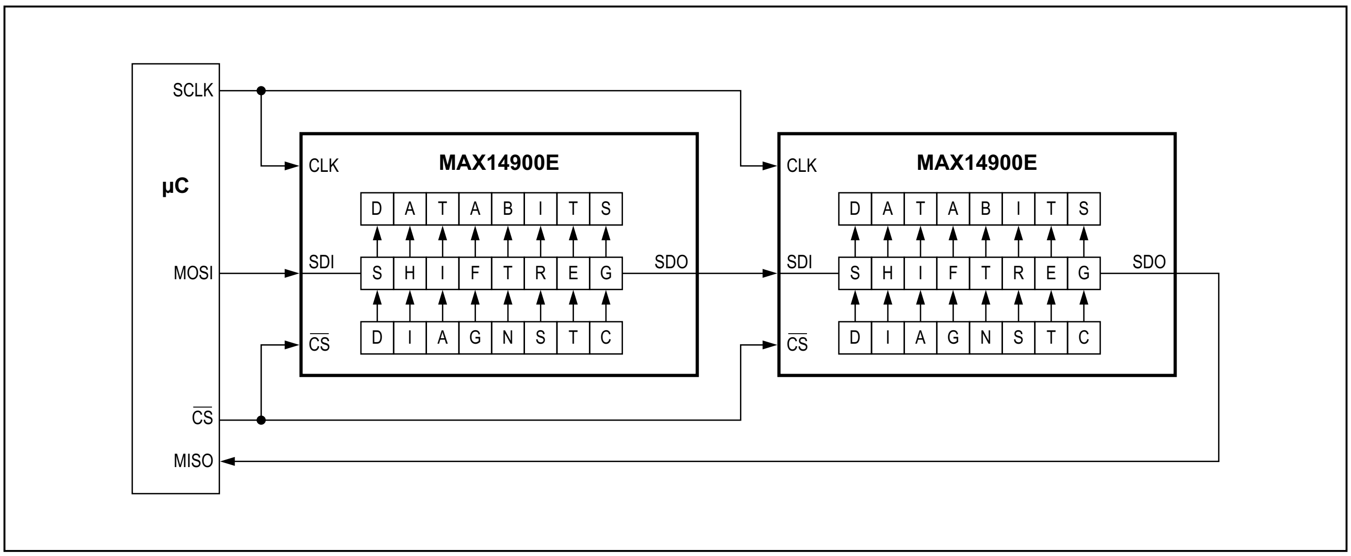


Figure 5. Daisy-Chained MAX14900E Devices with 8-Bit Serial Mode

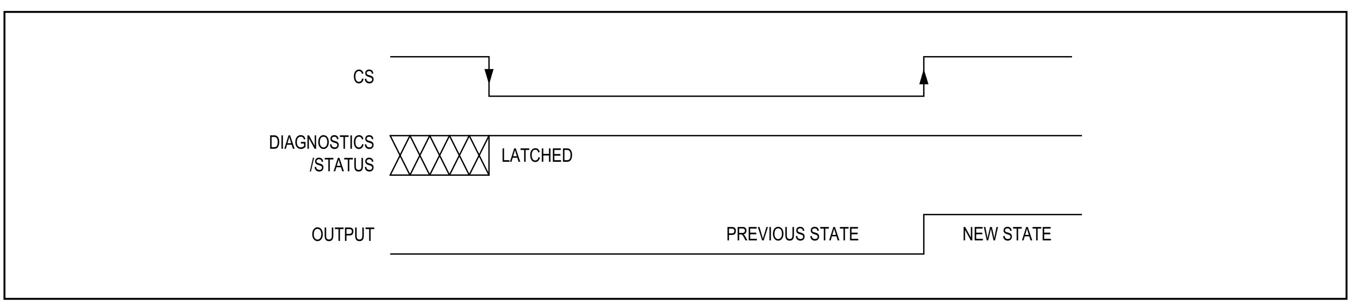


Figure 6. Internal Sampling Events Timing Diagram

8-Bit Serial Mode with Setting and Monitoring

In serial mode with 8-bit setting and 8-bit monitoring (SRIAL = high, S16/IN8 = low, CNFG/IN7 = low), the SPI shift register is 8 bits long (Figure 7). The DO_ bits set the state of the respective O_ output (Table 4). The F_ bits report fault information of the respective O_ output (Table 7).

8-Bit Serial Mode with Configuration and Monitoring

In serial mode with 8-bit configuration and 8-bit monitoring (SRIAL = high, S16/IN8 = low, CNFG/IN7 = high), the SPI shift register is 8 bits long (Figure 8). The C_ bits configure push-pull/high-side mode for the respective O_ output (Table 5). The F_ bits report fault information for the respective O_ output (Table 7).

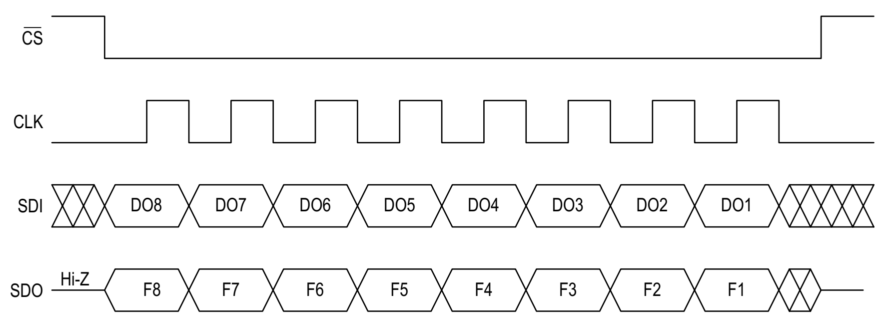


Figure 7. Serial Timing in 8-Bit Setting Serial Mode

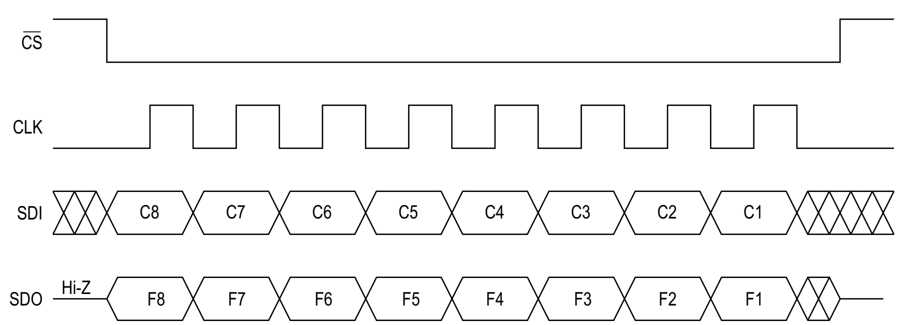


Figure 8. Serial Timing in 8-Bit Configuration Serial Mode

16-Bit Serial Mode with 8-Bit Setting/8-Bit Configuration

In serial mode with 8-bit setting/8-bit configuration and 16-bit monitoring (SRIAL = high, S16/IN8 = high, CNFG/IN7 = low), the SPI shift register is 16 bits long (Figure 9). The DO_ bits set the state of the respective O_ output and the C_ bits configure push-pull/high-side mode (Table 4 and Table 5). The F_ and S_ bits report the status information for each channel (Table 8).

Parallel Mode/16-Bit Serial Mode with 16-Bit Configuration

In parallel and serial mode with 16-bit serial configuration and 16-bit monitoring (SRIAL = low or SRIAL = high, S16/IN8 = high, CNFG/IN7 = high), the SPI shift register is 16 bits long (Figure 10). The C1_ and C0_ bits configure push-pull/high-side mode and open-load detection for each respective channel (Table 6). The F_ and S_ bits report the status information for each channel (Table 8).

Setting, Configuration, and Monitor Bit Definitions

Table 3 to Table 8 define the effects of the setting, configuration, and monitoring bits.

If PUSHPL = high, then all outputs are configured as push-pull mode regardless of C_.

Table 4. Serial Setting Truth Table

DO_	O_ STATE	
	PUSH-PULL OPERATION	HIGH-SIDE OPERATION
0	Low	Off
1	High	On

Table 5. 8-Bit Serial Configuration Truth Table

C_	O_ CONFIGURATION
0	High-side mode
1	Push-pull mode

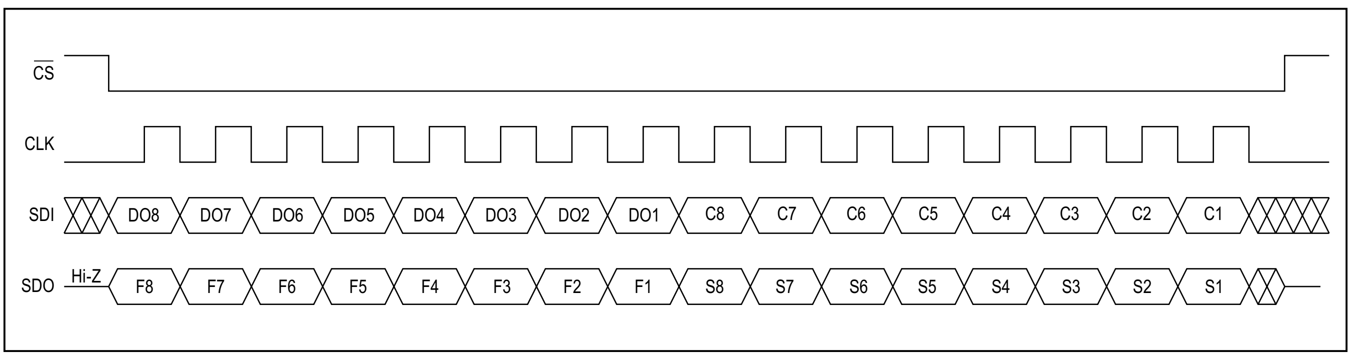


Figure 9. 16-Bit Serial Timing with 8-Bit Setting/8-Bit Configuration

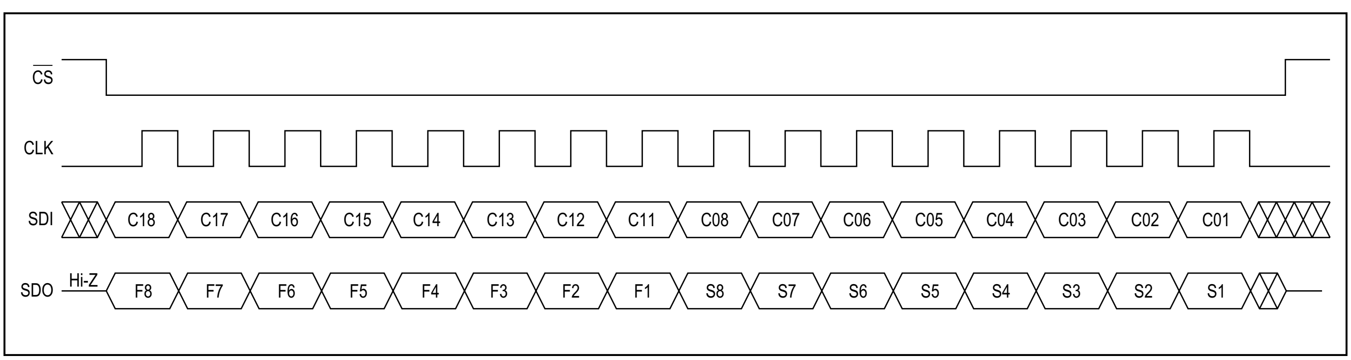


Figure 10. 16-Bit Serial Timing with 16-Bit Configuration

16-Bit Serial Configuration

Open-load detection is only available for outputs configured in high-side mode. If PUSHPL = high, then all outputs are configured as push-pull mode regardless of the C_ bits. In serial modes, if OL/IN1 = high, then all outputs that are configured as high side will have open-load detect on, regardless of the C1_ bits.

8-Bit Serial Diagnostics

If a driver is configured in push-pull mode, then a fault means that an overload or a thermal shutdown is present on that channel. If the driver is configured in high-side mode, then a fault means that an overtemperature condition is detected. If open-load detection is enabled in high-side mode, then the F_ bit is set when either an open-load (only possible with the high-side switch off) or an overtemperature is detected. In a UVLO condition, eight F_ bits are logic one.

16-Bit Serial Diagnostics

Logic-level status (S_bits) detection is only valid when no fault is present. Each S_ bit in normal (no fault) operating condition reports whether or not the O_ voltage is above (= 1) or below (= 0) 7V (typ).

When all F_ and S_ bits are logic one, a UVLO condition is present.

Table 6. 16-Bit Serial Configuration Truth Table

C1_	C0_	O_ CONFIGURATION
0	0	High-side mode, open-load detect off
0	1	Push-pull mode
1	0	High-side mode, open-load detect on
1	1	Push-pull mode

Table 7. 8-Bit Diagnostics Truth Table

F_	O_ CONDITION
0	No fault present
1	Fault (overload, open load, or UVLO) present

Table 8. 16-Bit Serial Diagnostics Truth Table

F_	S_	O_ STATUS
0	0	No fault detected, logic state of O_ is low
0	1	No fault detected, logic state of O_ is high
1	0	Fault detected, logic state not defined
1	1	UVLO detected

CRC Error Checking on Serial Interface

In serial mode (SRIAL = high), CRC error detection can be enabled by setting CRC/IN3 high to minimize incorrect operation due to noise on the SDI/SDO/CLK signals. With CRC error detection enabled, the MAX14900E detects errors on the SDI data that it receives from the controller and it calculates a CRC on the SDO data that it sends to the controller and appends this check byte to the SDO data.

This ensures that both the SPI data sent and received by the MAX14900E has a low likelihood of undetected errors.

The check byte appended to all 8-bit/16-bit SDO data by the MAX14900E contains a 7-bit frame check sequence (FCS). This FCS is based on the CRC generator polynomial $x^7 + x^5 + x^4 + x^2 + x + 1$. The CRC initialization condition is 0x7F. The MAX14900E in turn expects a check byte appended to all 8-/16-bit SDI data that it receives containing a FCS based on the same polynomial (Figure 11).

The controller should calculate the 7 FCS bits (CRI_) on the 8-/16-bit data including the logic 1 in the first position of the check byte. Thus the CRC is calculated on 9 or 17 bits. CRI1 is the LSB of the FCS. The MAX14900E verifies this received CRC. If the MAX14900E detects CRC errors on the received SDI data, then it ignores this data and does not change its configuration and/or output setting. Instead, the $\overline{\text{CERR}}$/IN4 output is asserted and the ERR bit is set in the check byte that it appends to the 8-/16-bit SDO diagnostic/status data that it sends back to the controller during the following serial communication cycle (Figure 12).

ERR is the error feedback bit that is sent back to the controller to signal that a CRC error was detected on the

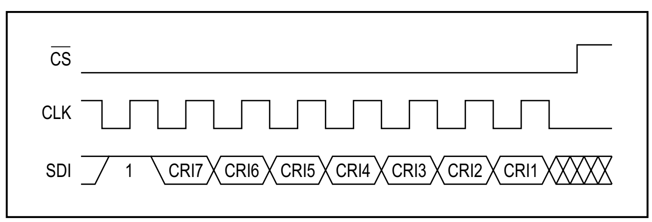


Figure 11. CRC Check Byte Expected From Controller

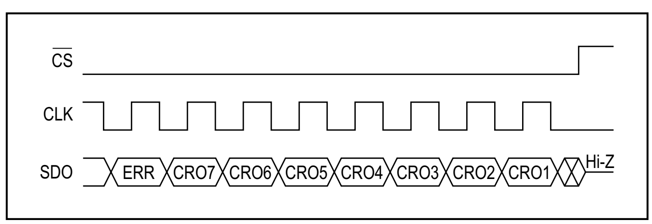


Figure 12. CRC Check Byte Sent by MAX14900E

previous SDI data reception. Note that ERR is delayed by one SPI cycle, i.e., it indicates that a CRC error was detected in the previous SPI data cycle. The $\overline{\text{CERR}}$/IN4 output is immediately set active when a CRC error is detected, allowing the controller to resend the last SDI data or take other action.

The CRO_ bits are the CRC bits that the MAX14900E calculates on the 8-/16-bit diagnostics and/or status data plus the ERR bit i.e., the output FCS is calculated on 9/17 bits. This allows the controller to detect errors on the SDO data received from the MAX14900E.

Applications Information

Driving Inductive Loads

In high-side mode, when the high-side switch turns off, an inductive load will cause the O_ voltage to swing negative in order to continue sourcing the load's inductive current while the inductor field collapses. The internal diodes support turn-off of inductive loads of up to 1.5H and currents of up to 1.9A.

Driving Lamp Loads

Lamp loads are incandescent lamps where the filament resistance is strongly dependent on the filament's temperature. The initial startup current is high because a cold filament has a very low resistance. The MAX14900E will reliably turn on 15W lamps over the operating temperature range.

Driving Capacitive Loads

When charging/discharging purely capacitive loads with a push-pull driver, the driver dissipates power that is proportional to switching frequency. The power can be estimated by $P_D \sim C \times V_{DD}^2 \times f$, where C is the load capacitance, V_{DD} is the supply voltage, and f is the switching frequency. For example, in an application with a 1nF load and 100kHz switching frequency, each driver dissipates 130mW at V_{DD} = 36V. When driving purely capacitive loads consider a maximum capacitance of around 10nF.

Multiple SPI Devices on Shared Bus

The SDO output is high impedance when $\overline{\text{CS}}$ is logic-high to allow connecting multiple devices in parallel on a shared SPI bus with the SDO lines connected together. When SDO is high impedance, an internal 200kΩ pull-down resistor is enabled to pull SDO to GND weakly.

Paralleling of Outputs

In high-side mode, multiple outputs can be connected together in parallel to achieve higher load currents. The total load current should be shared equally between these high-side switches that are operated in parallel. This is achieved by having identical trace resistances for all the PCB tracks from the O_ pins to the common star connection point. This is particularly important, since the on-resistance of each high-side switch is low: 85mΩ (typ).

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Connect all V_{DD} pins to a V_{DD} plane. Ensure that all V_{DD} pins have no more than 10mΩ between them. In this case a 1μF capacitor should be placed to the ground plane as close to the V_{DD} pins as possible. In the case low resistance paths are not possible between the V_{DD} pins, bypass each pin to GND via a 100nF capacitor.

A suppressor/TVS diode should be used between V_{DD} and GND to clamp high-surge transients on the V_{DD} supply input and surges from the O_ outputs. The standoff voltage should be higher than the maximum operating voltage of the equipment while the breakdown voltage should be around 40V.

As long field supply cables can generate large voltage transients on the V_{DD} supply due to large di/dt, it is recommended to add a large capacitor on V_{DD} at the point of field supply entry. Capacitance should be as large as possible, but 47μF electrolytic capacitor is recommended as a minimum.

High ESD Protection

Electrostatic discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly.

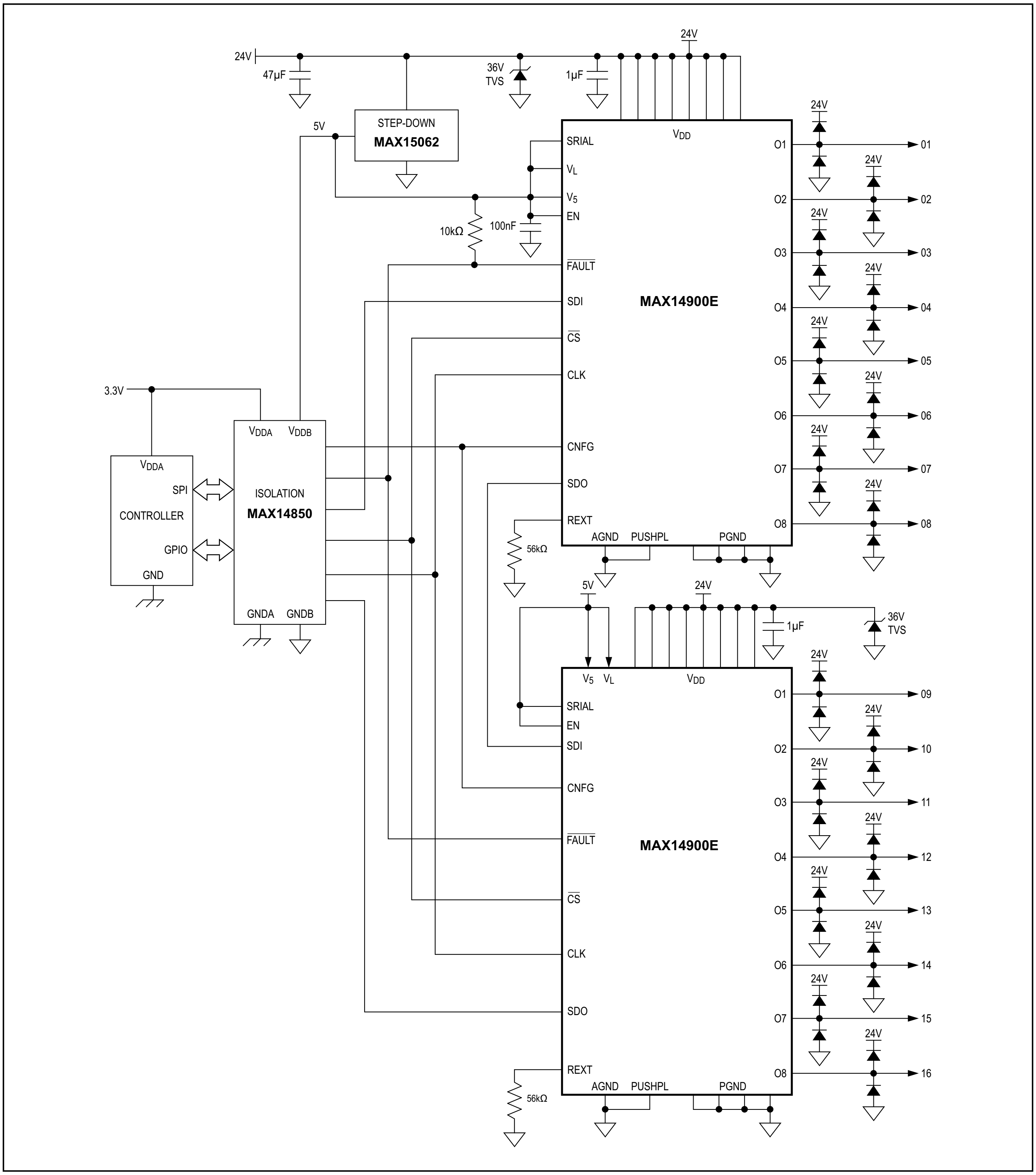
All O_ outputs are further protected against ESD up to ±15kV (HBM) without damage, when the part is operative in the application circuit with a 1μF bypass capacitor on V_{DD} and a suppressor/TVS diode.

In order to achieve even higher ESD levels, connect external diodes from each output to GND and to V_{DD} as described in the *Surge Protection* section.

Surge Protection

The MAX14900E O_ pin is tolerant to ±600V/(42Ω + 0.5μF) 1.2μs/50μs surge testing, when only using a TVS diode on V_{DD} and without protection diodes on the O_ pins. It achieved over ±1.5kV/(42Ω + 0.5μF) IEC61000-4-5 surge testing when using the *Typical Operating Circuit*. The silicon diodes on O_ must have low forward voltage diodes that support the surge currents, like MURA205T3G. A surge-suppressor diode on the V_{DD} supply must have low output impedance at the high surge currents. The SM30TY is suitable for this. Place all diodes and the V_{DD} capacitor as close to the MAX14900E pins as possible.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE (°C)	PIN-PACKAGE
MAX14900EAGM+CKT	-40 to +125	48 QFN-EP**
MAX14900EAGM+TCKT	-40 to +125	48 QFN-EP**
MAX14900EAGM+CKH	-40 to +125	48 TQFN-EP**
MAX14900EAGM+TCKH	-40 to +125	48 TQFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.

T =Tape and reel.

***EP = Exposed pad.*

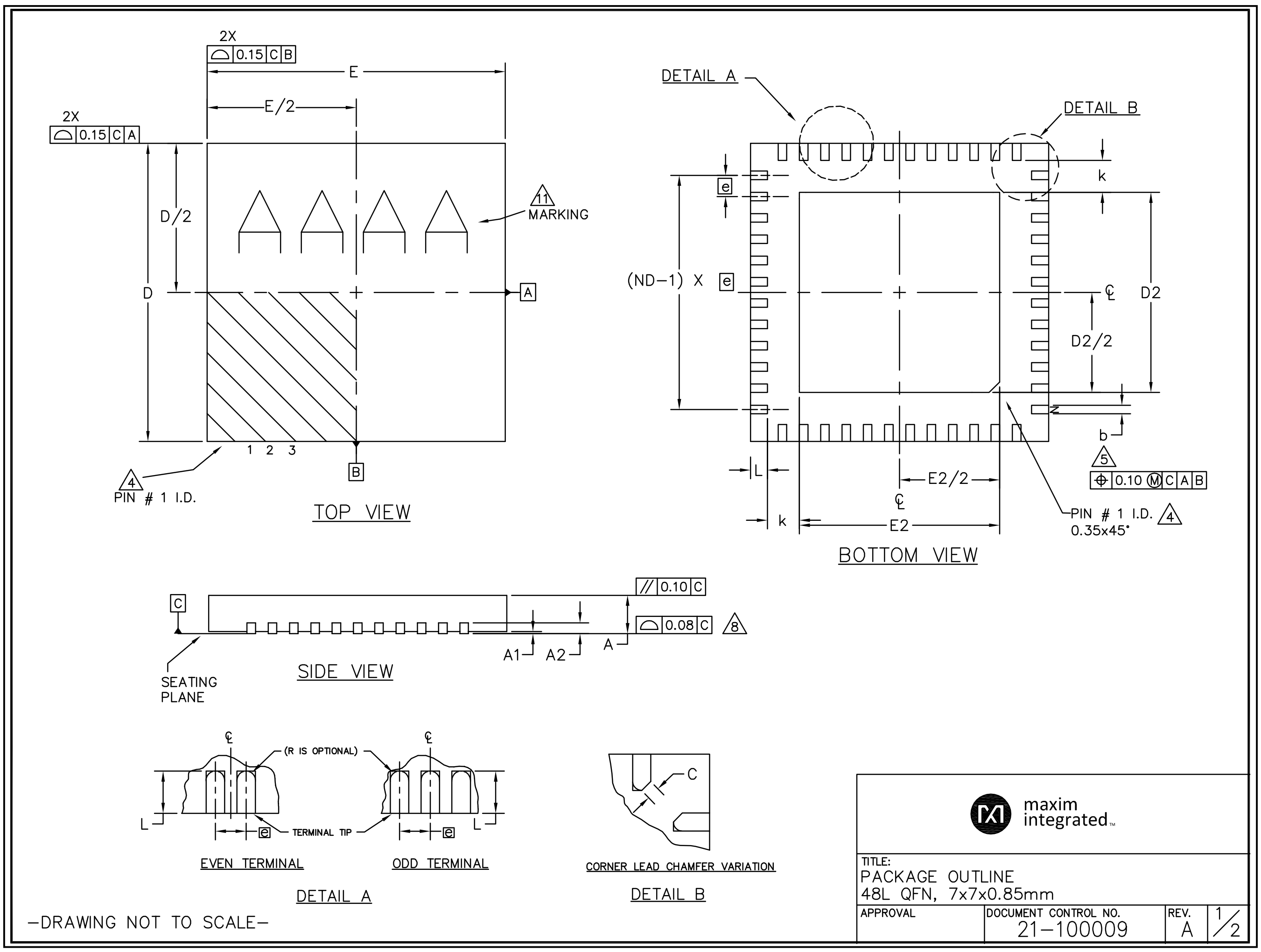
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 QFN	K4877+1	21-100009	90-100003
48 TQFN	T4877+6	21-0144	90-0130



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COMMON DIMENSIONS			
PKG SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.20 REF.		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	5.40	5.50	5.60
E	6.90	7.00	7.10
E2	5.40	5.50	5.60
e	0.50 BSC.		
k	0.25	–	–
L	0.30	0.40	0.50
C	0.115 X 45°		
N	48		
ND	12		
NE	12		
PACKAGE CODE	K4877-1		

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. WARPAGE SHALL NOT EXCEED 0.10 mm.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

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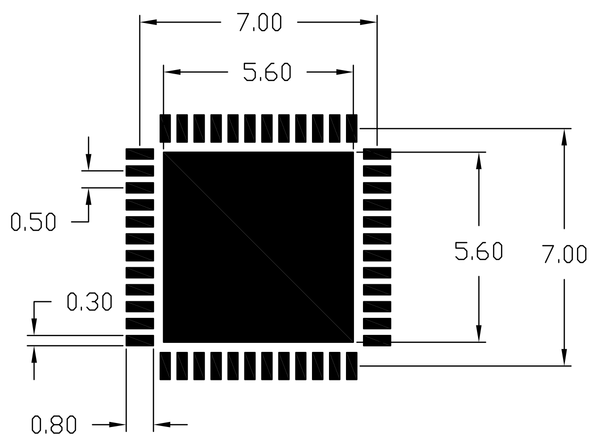
TITLE: PACKAGE OUTLINE 48L QFN, 7x7x0.85mm			
APPROVAL	DOCUMENT CONTROL NO. 21–100009	REV. A	2/2

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



NOTES:
1. REFERENCE PKG. OUTLINE: 21-100009.
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE ONLY.
5. ALL DIMENSIONS IN MM.

-DRAWING NOT TO SCALE-

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This document is subject to change without notice.
Contact technical support at http://www.maximintegrated.com/support for further questions.

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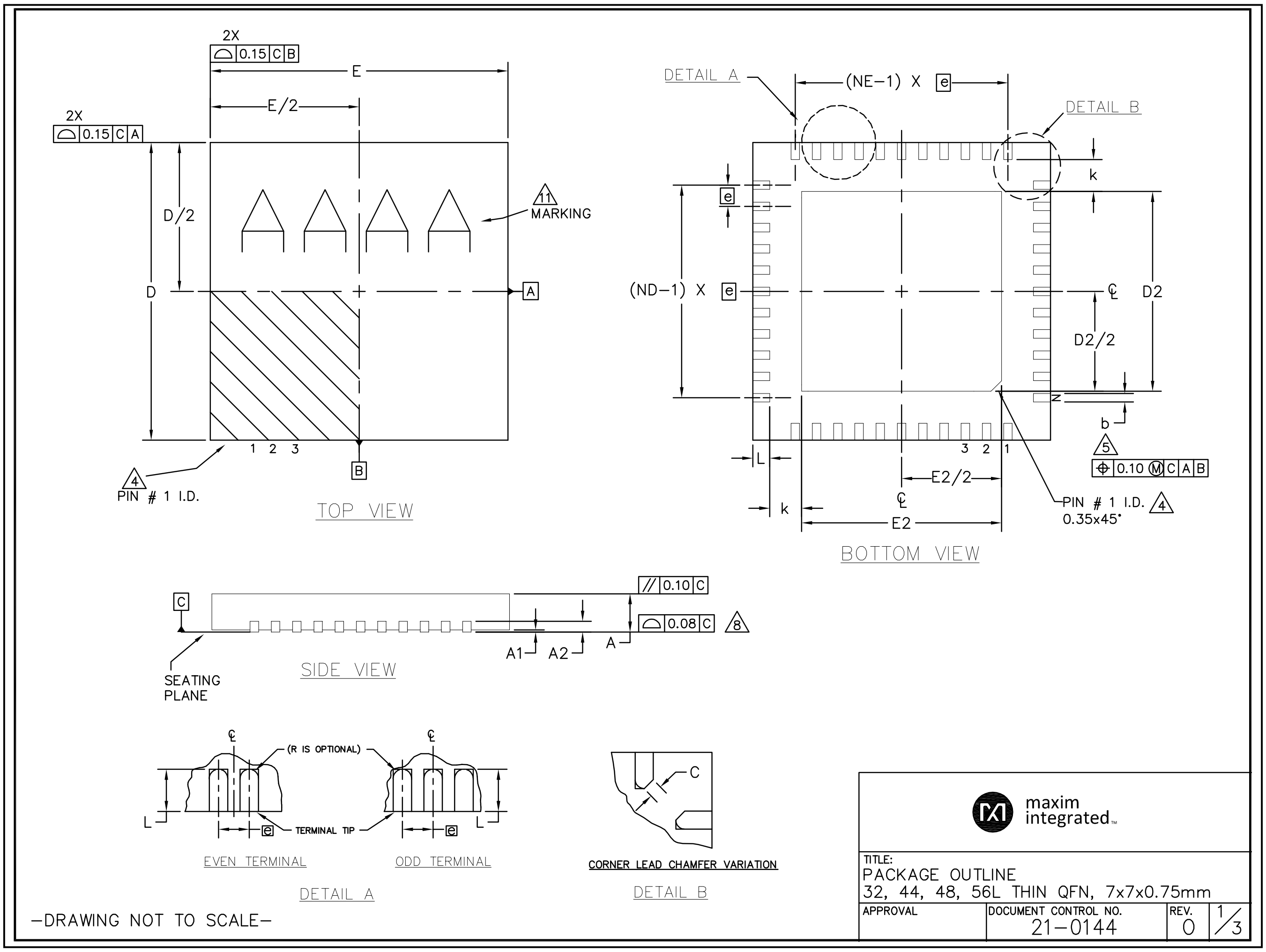
TITLE: PACKAGE LAND PATTERN, [K4877+1] QFN

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	90-100003	A	1/1

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

CORNER LEAD CHAMFER VARIATION

PKG. CODES	C
T4877–3	0.115 X 45°
T4877–4	0.115 X 45°
T4877–4C	0.115 X 45°
T4877–6	0.115 X 45°
T4877–7	0.115 X 45°
T4877–10	0.115 X 45°
T4877M–1	0.115 X 45°
T4877M–6	0.115 X 45°

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2 MIN.	D2 NOM.	D2 MAX.	E2 MIN.	E2 NOM.	E2 MAX.	JEDEC MO220 REV. C
T3277–2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277–3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477–2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD–1
T4477–2C	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD–1
T4477–3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD–1
T4877–3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877–4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877–4C	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877–6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877–7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877–10	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M–1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M–6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN–8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877N–8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877–9C	–	3.92	4.02	4.12	3.92	4.02	4.12	–
T5677–1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677MN–1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677–2	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677–3	–	5.40	5.50	5.60	5.40	5.50	5.60	–

–DRAWING NOT TO SCALE–

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TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.75mm

APPROVAL | DOCUMENT CONTROL NO. 21–0144 | REV. 0 | 2/3

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877–3/–4/–6 & T5677–1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

maxim integrated™

TITLE: PACKAGE OUTLINE 32, 44, 48, 56L THIN QFN, 7x7x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21–0144	REV. 0	3/3

Package Information

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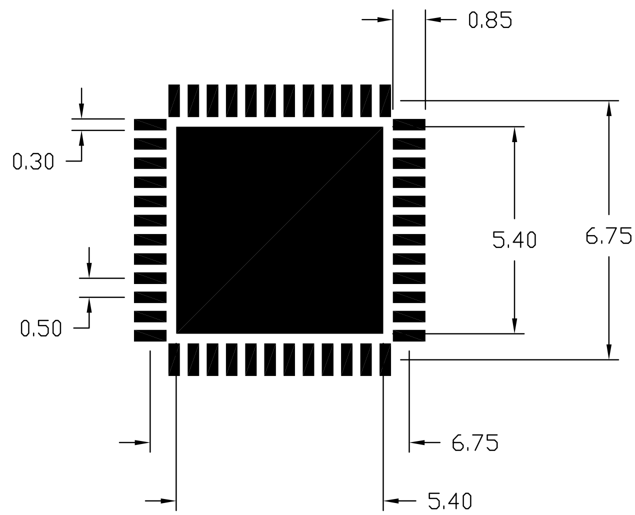

NOTES:
1. REFERENCE PKG. OUTLINE: 21-0144.
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.
5. ALL DIMENSIONS IN MM.

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TITLE: PACKAGE LAND PATTERN, [T4877-4 / T4877+4]			
APPROVAL	DOCUMENT CONTROL NO. 90-0130	REV. B	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—
1	6/14	Added new features	1, 4, 5, 7, 9, 10, 12, 14, 15, 17-21
2	11/14	Changed current limit and added TQFN package option	1–3, 13, 16, 20–23
3	1/15	Updated *General Description*, *Benefits and Features*, *Ordering Information*, and *Package Information* sections	1, 23-30
4	4/15	Updated *Functional Diagram* and *Maximum Power Dissipation* in the *Absolute Maximum Ratings* section, corrected mislabeled axis and symbols in *Typical Operating Characteristics*, and added the *Paralleling of Outputs* section under *Applications Information*	1-2, 4, 10-11, 13, 15-18, 21

