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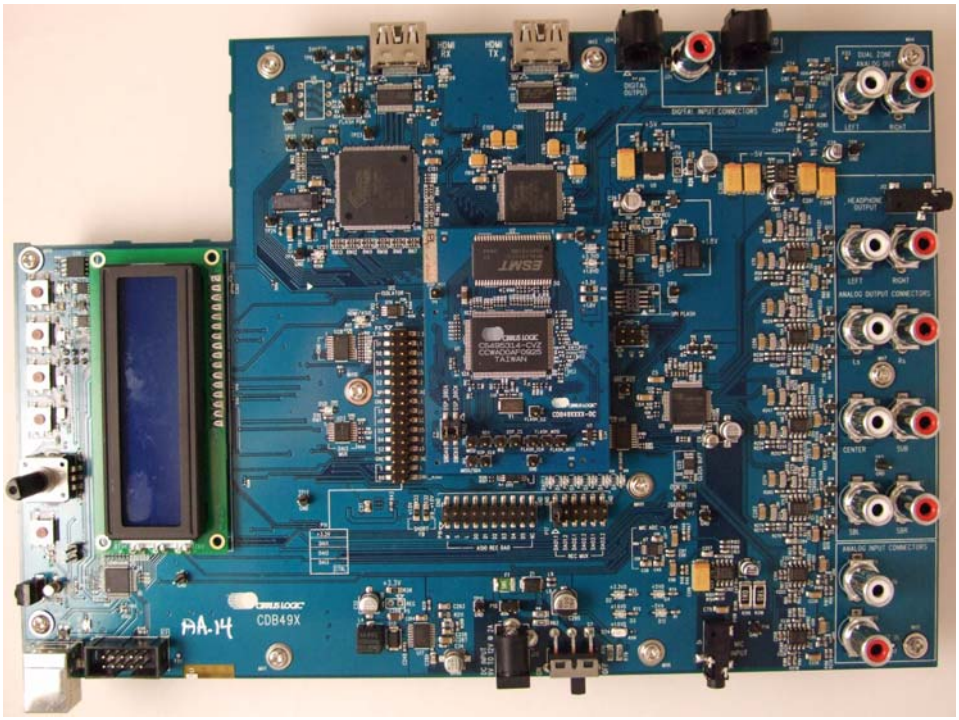
CIRRUS LOGIC®

CK49x
Customer Kit

CK49x–4953xx/ 4970x4

User's Manual



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

DEC 2012
DS898CK7

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

Chapter 1
Customer Kit Contents and Requirements

1.1 CK49x Customer Kit Contents

Table 1-1. CK49x Customer Kit Contents

Customer Kit	Item	Quantity
CK49x-49530[1] CK49x-49531 CK49x-495303[1] CK49x-495313[1] CK49x-497024 CK49x-497014[4]	CDB49x Evaluation Board[2]	**1**
CK49x-49530[1]	DC49530 Daughter Card (128-pin package) with CS495304 DSP	**1**
CK49x-49531	DC49531[3] Daughter Card (128-pin package) with CS495314 DSP	**1**
CK49x-495303[1]	DC49503 Daughter Card (128-pin package) with CS495303 DSP	**1**
CK49x-495313[1]	DC49513 Daughter Card (128-pin package) with CS495313 DSP	**1**
CK49x-497024	DC497024 Daughter Card (128-pin package) with CS497024 DSP	**1**
CK49x-497014[4]	DC497014 Daughter Card (128-pin package) with CS497014 DSP	**1**
CK49x-49530 CK49x-49531 CK49x-495303[1] CK49x-495313[1] CK49x-497024 CK49x-497014[4]	Power Supply: +9V, 2A, 100V - 240V with AC Power Cord	**1**
CK49x-49530 CK49x-49531 CK49x-495303[1] CK49x-495313[1] CK49x-497024 CK49x-497014[4]	USB Cable (USB 2.0)	**1**
CK49x-49530 CK49x-49531[1] CK49x-495303 CK49x-495313[1] CK49x-497024 CK49x-497014[4]	Document Card explaining how to get the latest board software	**1**

1. Not available for ordering.
2. In this manual, the main (large) board is called the "CDB49x Evaluation Board as shown in Figure 1-1." When a daughter card is installed on the CDB49x Evaluation Board as shown in Figure 1-2, the board is then called the "CK49x Evaluation System"
3. DC49531 is being renamed to DC495314.
4. Use the DC497014 daughter card when implementing firmware other than firmware from DTS.

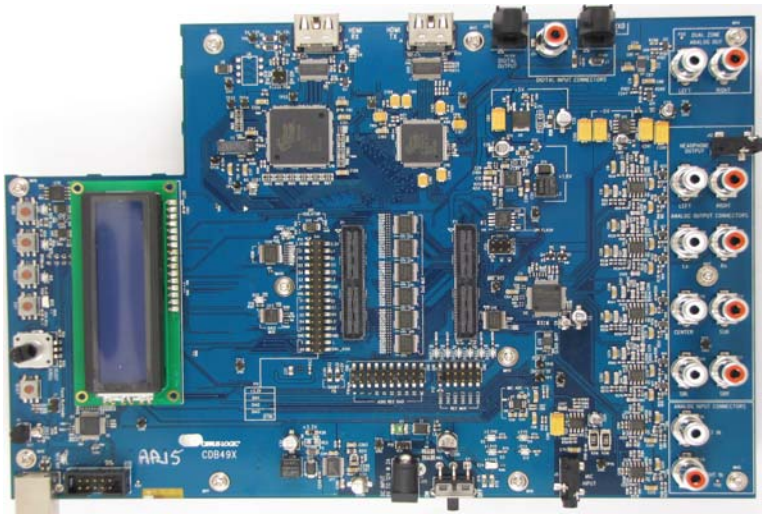


Figure 1-1. CDB49x Evaluation Base Board (without DC4953x Installed)

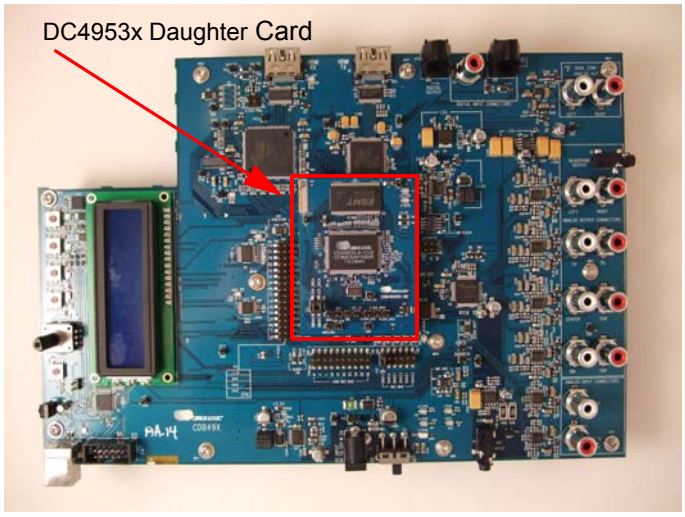


Figure 1-2. CK49x Evaluation System (CDB49x Evaluation Base Board (with DC4953x Installed)

1.2 Requirements

1.2.1 PC Requirements

- Microsoft® Windows XP® Operating System
- USB 2.0 Support

1.2.2 Software Requirements

- Cirrus Board Software Package (available from your local Cirrus Logic representative)

1.2.3 Support Hardware Requirements

- Digital or Analog Audio Source (for example, DVD player, PC with a digital audio card/device)
- Amplified Speakers for audio playback (for example, powered PC speakers, AVR/amp + speakers)

1.2.4 Cabling Requirements

- Digital Audio Inputs – HDMI cables, S/PDIF optical cables, RCA audio cables (Connect to digital audio card, audio analyzer, or DVD player), 20-pin ribbon cable (Play I^2S audio from digital audio card)
- Digital Audio Output – HDMI cables, S/PDIF Optical cable, RCA audio cable (Connect to digital audio card, audio analyzer, or AV), 20-pin ribbon cable (Record I^2S audio from digital audio card)
- Analog Audio Inputs – RCA audio cables (Connect CK49x line-level inputs to analog audio source)
- Analog Audio Outputs – RCA audio cables (Connect CK49x line-level outputs to powered speakers or AVR), 1/8" stereo headphone cable (Connect CK49x line-level output to headphones)

1.3 CK49x System Description

A block diagram of the CDB49x main board is shown in Figure 1-3 and a block diagram of the DC4953x daughter card in Figure 1-4. The sections that follow provide a detailed description of each block.

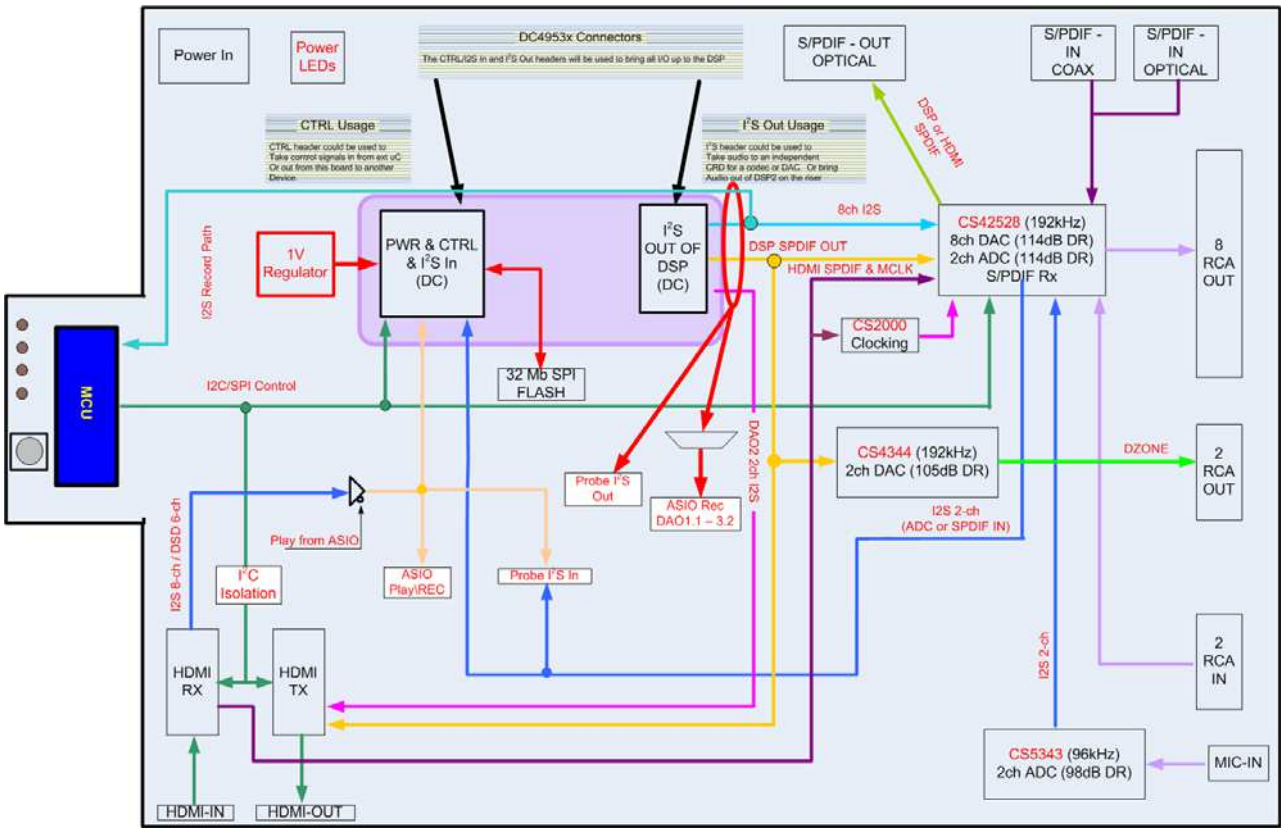


Figure 1-3. CDB49x Main Board Block Diagram

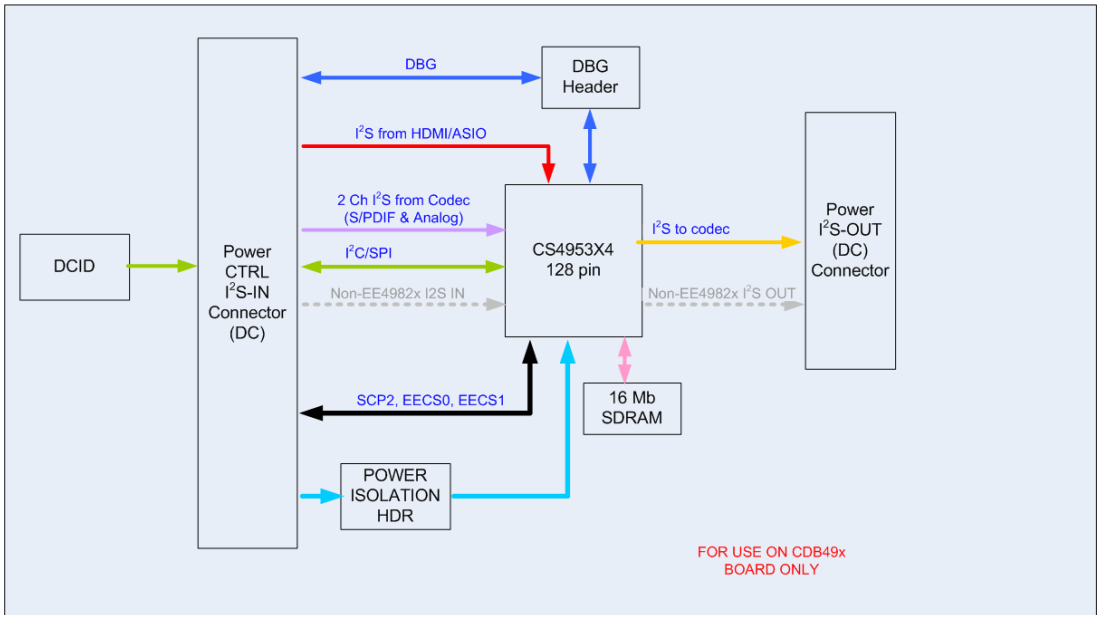


Figure 1-4. DC4953x Daughter Card Block Diagram

1.3.1 Audio Inputs

1.3.1.1 Analog Line-level Inputs

Analog line-level inputs have the following characteristics:

- Connector Type: RCA Female
- Absolute Maximum Signal Level: +12Vp-p
- Full Scale Amplitude: 2V_{RMS}
- Reference Designators: J26,J28, or LEFT-IN, RIGHT-IN

1.3.1.2 HDMI Digital Input

HDMI digital inputs have the following characteristics:

- Connector Type: HDMI Type A Female
- Reference Designators: J4, or HDMI RX

1.3.1.3 Optical Digital Inputs

Optical digital inputs have the following characteristics:

- Connector Type: Fiber Optic RX for Digital Audio, JIS F05 (TOSLINK)
- Reference Designators: J8, or RX0

1.3.1.4 Coaxial Digital Inputs

Coaxial digital inputs have the following characteristics:

- Connector Type: RCA Female
- Maximum Signal Level: 5Vp-p
- Reference Designators: J31, or RX1

1.3.1.5 I^2S Digital Input

Coaxial digital inputs have the following characteristics:

- Connector Type: 0.100" Male Header
- Maximum Signal Level: +3.3V
- Reference Designator: P3

1.3.1.6 Microphone Input

The microphone input has the following characteristics:

- Connector Type: 3.5mm (1/8") Stereo Female
- Absolute Maximum Signal Level: 14.3mVp-p
- Full Scale Amplitude: 6.5mVp-p
- Reference Designator: J5

1.3.2 Audio Outputs

1.3.2.1 Main Analog Line-level Outputs

Analog line-level outputs have the following characteristics:

- Connector Type: RCA Female
- Full Scale Amplitude: 2VRMS
- Reference Designators: J33-J40, or LEFT, RIGHT, Ls, Rs, CENTER, SUB, SBL, SBR

1.3.2.2 Headphone Output

Analog line-level outputs have the following characteristics:

- Connector Type: 3.5mm (1/8") Stereo Female
- Full Scale Amplitude: 2VRMS
- Reference Designators: J12, or HEADPHONE OUT

The headphone output shares the same Op Amp that drives Main LEFT/RIGHT outputs, which means that headphone content will always be the same as Main LEFT/RIGHT. Only one pair of outputs should be connected to a load - either HEADPHONE OUT or J34/J36.

1.3.2.3 Dual Zone Analog Line-level Outputs

Analog line-level outputs have the following characteristics:

- Connector Type: RCA Female
- Max Full Scale Amplitude: 1.23VRMS
- Reference Designators: J1, J10, or LEFT, RIGHT

1.3.2.4 HDMI Digital Output[1]

HDMI digital outputs have the following characteristics:

- Connector Type: HDMI Type A Female
- Reference Designators: J6, or HDMI TX

1.3.2.5 Optical Digital Output

The optical digital output has the following characteristics:

- Connector Type: Fiber Optic TX for Digital Audio, JIS F05 (TOSLINK)
- Reference Designator: J24, or DIGITAL OUTPUT

1.3.2.6 I^2S Digital Output

I^2S digital output has the following characteristics:

- Connector Type: 0.100" Male Header
- Maximum Signal Level: +3.3V
- Reference Designator: P12

1. HDMI Digital Output is not currently supported.

1.3.2.7 I²S Digital Output (DAO Mux Output)

I²S digital output has the following characteristics:

- Connector Type: 0.100" Male Header
- Maximum Signal Level: +3.3V
- Reference Designator: P16

1.3.3 DC Power Input

The DC power input has the following characteristics and is switched by S7:

- Voltage Range: +9VDC TO +12VDC
- Minimum Power: 18W supply (2A @ 9V)
- Connector Type: 2mm Female, positive center pin
- Reference Designator: J25

1.3.4 USB Connector

The control header has the following characteristics:

- Connector Type: USB Standard B Connector
- Reference Designator: J2

This connector is the interface between the CK49x and the PC.

1.3.5 MCU Programming Header

This header is used to program the MCU from a Silicon Labs programming dongle. This is not for customer use, and should be used only by Cirrus FAEs for upgrading the board.

- Connector Type: 0.100" Shrouded Male Header
- Reference Designator: J9

1.3.6 Reset button

The button S6 (located near the USB connector J2) is used to reset the MCU. In stand-alone mode this will re-initialize the entire board and start the stand-alone program over from the beginning.

In USB-control mode, this button will re-initialize the board and force the device to re-enumerate itself on the PC USB interface.

1.3.7 Buttons and Knobs

The buttons S1 - S4 (located near the LCD) are used for controlling the MCU when in stand-alone mode.

The knob S5 is also used for controlling the MCU when in stand-alone mode.

1.3.8 DAO MUX Select Header

The DAO outputs of the DSP are sent to a mux that drives I²S Digital Output header P16. The signals driven to P16 are selected by the Header P17. Only 1 shunt may be installed on header P17 at any time. Using more than 1 shunt will cause multiple buffers to drive their outputs simultaneously and cause contention.

The output buffer currently enabled is indicated by the LEDs D18 - D23.

1.3.9 DAI1 Audio Input Source Multiplexer

The audio input source multiplexer has the following characteristics:

- Source 0 [shunt removed]: HDMI RX I2S Audio
- Source 1 [shunt installed]: I^2S Audio (ASIO I^2S Board)
- Reference Designators: U15, U28

This multiplexer is controlled by pins 1-2 of header P4, and is used to select which audio source feeds the CS495xxx/CS497xxx DAI1 pins when the ASIO I^2S Board is installed. When the on-board sources (HDMI RX) are being used, the ASIO audio data cannot be processed. Likewise, when the ASIO audio data source (ASIO I^2S Board) is selected, the on-board audio inputs are disabled.

1.3.10 DAI2 Audio Input Source Multiplexer

The audio input source multiplexer has the following characteristics:

- Source 0: CS42528 Audio (ADC or S/PDIF)
- Source 1: Bi-Phase Encoded S/PDIF Signal
- Reference Designator: U23

This multiplexer is controlled by GPO1 of the CS42528 (U5), and is used to select which audio sources feed the CS495xxx/CS497xxx DAI2 pins. When the DSD audio from HDMI RX is being used, the CS42528 data cannot be processed. Likewise, when the CS42528 audio is selected, the HDMI RX DSD audio is disabled.

1.3.11 CS495xxx/CS497xxx Audio DSP

The audio DSP (U1 on DSP Daughtercard) is a dual-core processor designed specifically for audio applications. The CK49x allows a designer to evaluate the CS495xxx/CS497xxx DSPs in many different modes of multi-channel input and output. The 128-pin footprint on this board is compatible with any CS495xxx/CS497xxx chip that uses the LQFP128 package.

Audio input data to the DSP can come from any of the following sources:

- CS42528 Line-Level Analog In
- CS42528 Microphone Analog In
- CS42528 Digital S/PDIF In
- HDMI RX
- I^2S Through ASIO I^2S Board (feature not currently supported)

Audio output data from the DSP can be sent to the following destinations:

- CS42528 Line-Level Analog Output
- CS42528 Headphone Analog Output
- CS42528 Digital S/PDIF Out
- HDMI TX
- I^2S Through Header P16

The CS4953xx/CS4970x4 has many applications stored in internal ROM, but a host is still required to configure the application for a particular system. The CK49x allows the PC to act as a host to boot and configure the DSP through the GUI software.

The DSP is booted primarily from external serial Flash (U13 on CDB49x) using the DSP Condenser system for simplified MCU control.

1.3.12 Debug Header

The DC49xxx daughtercard (DSP daughtercard) has a debug port (TP13) intended for factory testing of the DSP. By default, shunts are installed across the header to allow debug from the attached MCU. If the jumpers are removed, it is possible to debug the DSP using an external controller.

1.3.13 CS2000 Clock Synthesizer

The CS2000 (U25) is a high performance clocking device that is used to reduce jitter on recovered clocks through the use of a low-jitter PLL and clean reference clock. The CS2000 is used on this board to reduce the jitter on the MCLK recovered from an HDMI link.

The CS2000 can also be programmed to pass the reference clock (XTAL_OUT from the DSP) directly to the CS42528 audio CODEC and S/PDIF RX.

1.3.14 CS42528 S/PDIF RX

The CS42528 (U5) has an integrated 192 kHz S/PDIF receiver with an input multiplexer. All of the S/PDIF sources on the board (RX0, RX1, DSP, U16) are connected to the CS42528 input multiplexer. The active S/PDIF signal is selected by changing the internal mux through the serial host port of the CS42528. This selection is controlled through the Audio In configuration within DSP Composer (see Chapter 4, "Programming the DSP on the CK49x Evaluation Board" for details).

When S/PDIF audio is being processed, the CS42528 must master MCLK for the system (see Figure 1-6 for details).

1.3.15 CS42528 Audio CODEC

The CS42528 (U5) is a high-performance, multi-channel audio CODEC capable of supporting sample rates up to 192 kHz on its 2 ADCs and 8 DACs. This device is used for main-channel analog-to-digital and digital-to-analog conversions on the CK49x.

All analog inputs (J5, J26, J28) and 8 of the analog outputs (J33 - J40) are connected to the CS42528. The microphone input (J5) uses an external ADC (U7) to feed the dedicated ADC input of the CS42528. When the microphone is in use, a special TDM format is used to deliver the digitized microphone audio to the DSP via the SAI data output of the CS42528.

When analog audio is being processed, the 24.576 MHz crystal for the CS495xxx/CS497xxx must master MCLK for the system (see 'Audio Clocking on page 1-10 for details).

1.3.16 CS4344 DAC

The CS4344 (U3) is a high-performance, 2-channel DAC capable of converting audio data with sample rates up to 192 kHz. This device is used for the dual-zone digital-to-analog conversions on the CK49x.

Analog outputs (J1, J10) are connected to the CS4344. The dual-zone DAC is connected to the DAO2 port of the CS495xxx/CS497xxx to allow up to 10 channels of simultaneous analog output.

1.3.17 HDMI Recevier (RX)

The Silicon Image™ Si9135 HDMI Rx (U16) is used for the HDMI input on the CK49x. It can provide up to 4 lines of I^2S data which can support PCM, legacy compressed audio (DD, DTS), and new HD audio streams.

Because the Si9135 responds to all I^2C addresses, a bus isolator (U14) has been used to prevent the HDMI Rx from responding to serial communication intended for other devices on the CK49x.

1.3.18 HDMI Transmitter (TX)

The Silicon Image Si9134 HDMI Tx (U19) is used for the HDMI output on the CK49x.

Note: The HDMI Tx function is currently not supported on the CK49x.

Because the Si9134 responds to all I^2C addresses, a bus isolator (U14) has been used to prevent the HDMI Tx from responding to serial communication intended for other devices on the CK49x.

1.3.19 Memory

The CDB49x is assembled with a 32-Mbit serial Flash (U13).

The CS495xxx/CS497xxx can use external SDRAM (U15 on DC4953x) to implement features such as large multi-channel audio delays. A 16 Mbit SDRAM (200 MHz) is connected to the 150 MHz memory bus of the CS495xxx/CS497xxx.

1.3.20 Audio Clocking

Clocking architecture is one of the most important aspects of an audio system. The input and output clock domains of the DSP must be synchronous when delivering audio data in an isochronous fashion (constant bit-rate delivery), even if the input/output domains operate at different frequencies (e.g. 48 kHz input/96 kHz output). Systems utilizing I^2S delivery of S/PDIF input, ADC input, or other digital audio input use isochronous delivery.

The requirements are slightly more complicated for systems using "bursty" delivery on the input side of the DSP, but the CK49x is designed to emulate isochronous systems.

The CK49x can operate in three different clocking modes. Each of these modes is explained in the following sections.

1.3.20.1 Clock and Data Flow for ADC Input

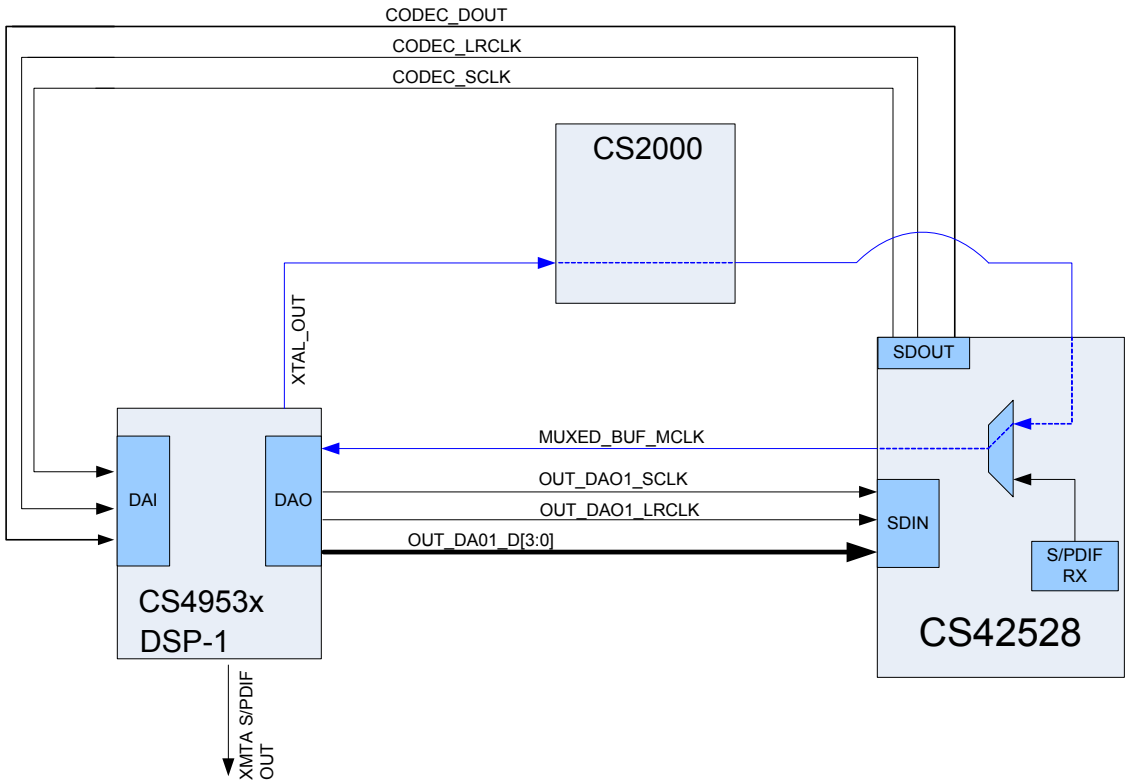


Figure 1-5. CS495xxx/CS497xxx ADC Clocking

The ADC clocking architecture is used when the ADCs are used as the only audio input (i.e. S/PDIF is disabled, and the audio input source multiplexer (U23) is used to select CODEC audio sources. Figure 1-5 illustrates this clocking configuration.

XTAL_OUT from the CS495xxx/CS497xxx is MCLK for the system via the CS2000 and CS42528 clocking mux, and the codec masters the input clocks (MUXED_SCLK/MUXED_LRCLK) of the CS495xxx/CS497xxx. The system routing of the clocks was simplified by using the CS42528 to drive MCLK to the system, but the internal clock multiplexer of the CS42528 is forced to the OMCK setting to pass XTAL_OUT.

The CS495xxx/CS497xxx always masters its output clocks (OUT_DAO1_SCLK/OUT_DAO1_LRCLK).

Table 1-2. ADC Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_BUF_MCLK	CS495xxx/CS497xxx	CS42528	24.576 MHz
CODEC_SCLK	MUXED_BUF_MCLK	CS42528	64*Input Fs (default)
CODEC_LRCLK	MUXED_BUF_MCLK	CS42528	Input Fs
OUT_DAO1_SCLK	MUXED_BUF_MCLK	CS495xxx/CS497xxx	64*Output Fs (default)
OUT_DAO1_LRCLK	MUXED_BUF_MCLK	CS495xxx/CS497xxx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the CS42528's RMCK pin. The CS42528 provides the recovered clock from the S/PDIF input unless it loses signal lock, in which case the CS42528 passes the DSP clock (XTAL_OUT) that it receives on the OMCK pin via the CS2000.

1.3.20.2 Clock and Data Flow for S/PDIF Input

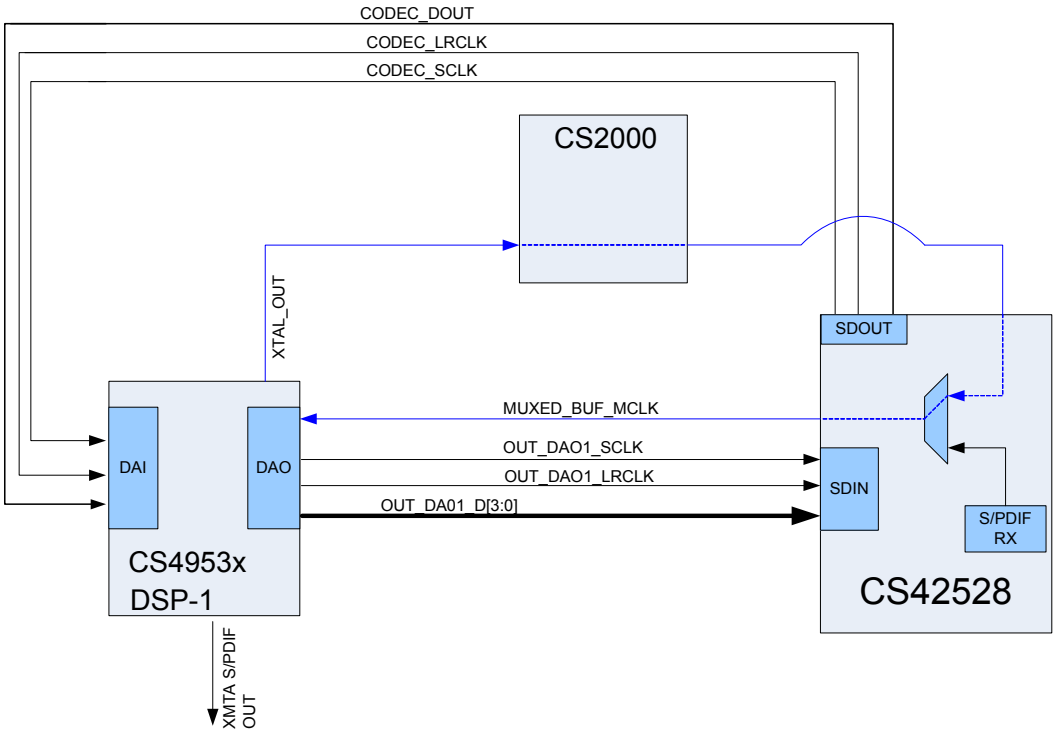


Figure 1-6. CS495xxx/CS497xxx S/PDIF Clocking

The S/PDIF clocking architecture is used when any S/PDIF RX is used as an audio source. That is, any S/PDIF RX is selected, and the audio input source multiplexer (U23) is used to select CODEC audio sources. Figure 1-6 illustrates this clocking configuration.

MCLK recovered from the incoming S/PDIF stream must be MCLK for the system, and the codec masters the input clocks (CODEC_SCLK/CODEC_LRCLK) of the CS495xxx/CS497xxx. In this configuration the internal multiplexer of the CS42528 routes the recovered MCLK to MUXED_MCLK.

The CS495xxx/CS497xxx always masters its output clocks (OUT_DAO1_SCLK/OUT_DAO1_LRCLK).

Table 1-3. S/PDIF Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_MCLK	CS42528	CS42528	512*S/PDIF Fs (e.g. 24.576 MHz for 48 kHz),
CODEC_SCLK	MUXED_MCLK	CS42528	64*Input Fs (default)
CODEC_LRCLK	MUXED_MCLK	CS42528	Input Fs
OUT_DAO1_SCLK	MUXED_MCLK	CS495xxx/CS497xxx	64*Output Fs (default)
OUT_DAO1_LRCLK	MUXED_MCLK	CS495xxx/CS497xxx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the CS42528's RMCK pin. The CS42528

provides the recovered clock from the S/PDIF input unless it loses signal lock, in which case the CS42528 passes the DSP clock (XTAL_OUT) that it receives on the OMCK pin.

1.3.20.3 Clock and Data Flow for HDMI or ASIO Input Data Delivery

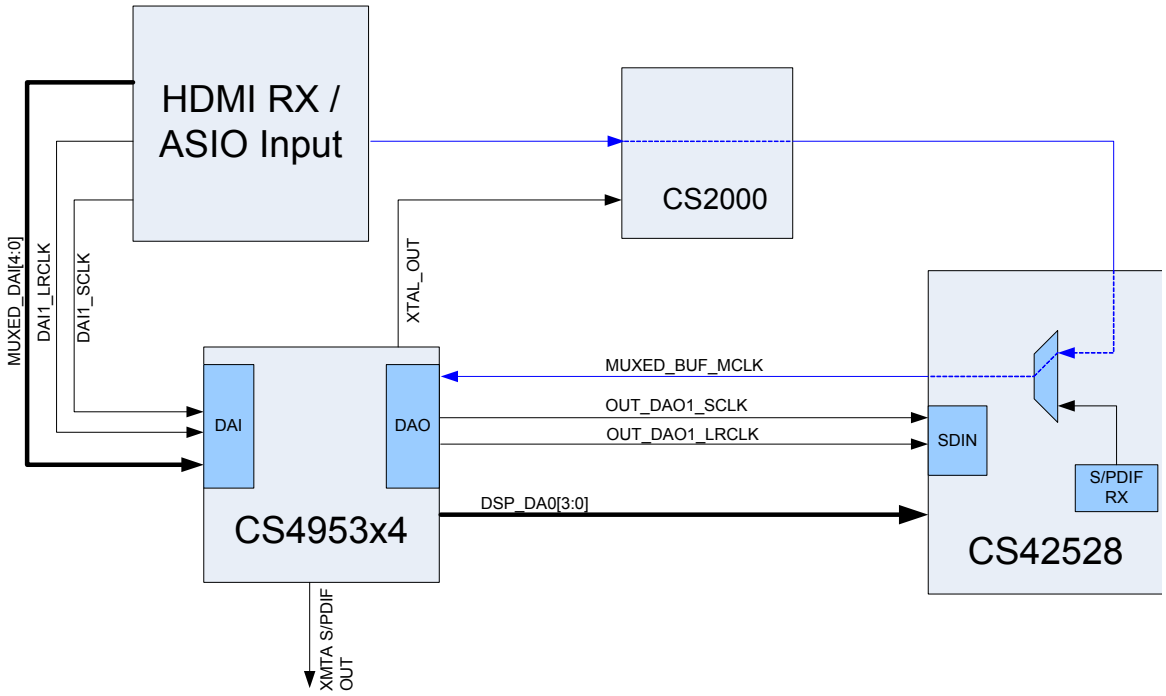


Figure 1-7. HDMI Clocking

When the HDMI or ASIO source is selected, that device masters the system MCLK, and the input clocks (MUXED_SCLK/MUXED_LRCLK) of the CS495xxx/CS497xxx.

The CS495xxx/CS497xxx always masters its output clocks (OUT_DAO1_SCLK/OUT_DAO1_LRCLK).

Table 1-4. HDMI Clocking

Clock Name	Clock Master Source	Clock Driver	Clock Frequency
MUXED_MCLK	HDMI/ASIO Source	HDMI/ASIO Source	256*S/PDIF Fs (e.g. 12.288 MHz for 48 kHz)
DAI1_SCLK	MUXED_MCLK	HDMI/ASIO Source	64*Input Fs (default)
DAI1_LRCLK	MUXED_MCLK	HDMI/ASIO Source	Input Fs
OUT_DAO1_SCLK	MUXED_MCLK	CS495xxx/CS497xxx	64*Output Fs (default)
OUT_DAO1_LRCLK	MUXED_MCLK	CS495xxx/CS497xxx	1*Input Fs (default)

Note: MUXED_MCLK is the clock signal that is driven by the HDMI source.

1.4 DS898CK4Other Useful Information

1.4.1 Web Sites

- Cirrus Logic main web site: www.cirrus.com

1.4.2 DSP Information

The following information can be obtained from your Cirrus Logic representative.

- *CS495xxx/CS497xxx Data Sheet*
- *CS495xxx/CS497xxx System Designer's Guide*
- AN288, *CS495xxx/CS497xxx Firmware User's Manual*

1.4.3 Board Information

- The following information can be obtained from your local Cirrus Logic representative.
- Schematics
- BOM
- Artwork and PCB stack up

1.4.4 Audio CODEC Information

The following information can be obtained from your local Cirrus Logic representative.

- *CS42528 Data Sheet*
- *CS42528 Errata*

1.4.5 DSP Software Utility Information

The following information can be obtained from your local Cirrus representative.

- *DSP Composer™ User's Manual*
- *DSP Composer™ Primitive Elements Reference*

The documents listed above are updated periodically and may be more up-to-date than the information in this document. Check the Cirrus Logic web site for the latest updates.

Chapter 2
Introduction to CK49x Evaluation System

2.1 Introducing the CK49x Evaluation System

The CK49x Evaluation System is composed of the CDB49x base board and the DC4953x daughter card where the C24953x4 DSP is installed. The CK49x Evaluation System provides a practical platform for emulating a typical multi-channel audio system application. The on-board MCU provides a USB control port used to interface the host PC to the CK49x Evaluation System, and convert GUI commands into the serial control protocol required for configuring the CS4953x4 DSP, CS42528 and CS2000 audio ICs, and the HDMI interface chips. Figure 2-1 shows the CK49x Evaluation System when controlled by the user's PC. Figure 2-2 shows the CK49x Evaluation System operating in Standalone mode. Standalone mode is described in detail in Chapter 5.

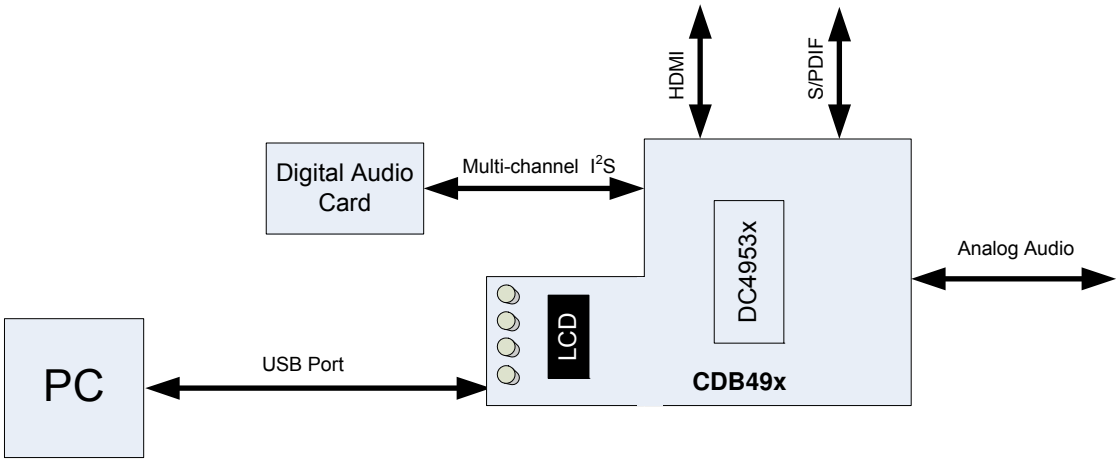


Figure 2-1. CK49x Evaluation System Block Diagram Using PC Control

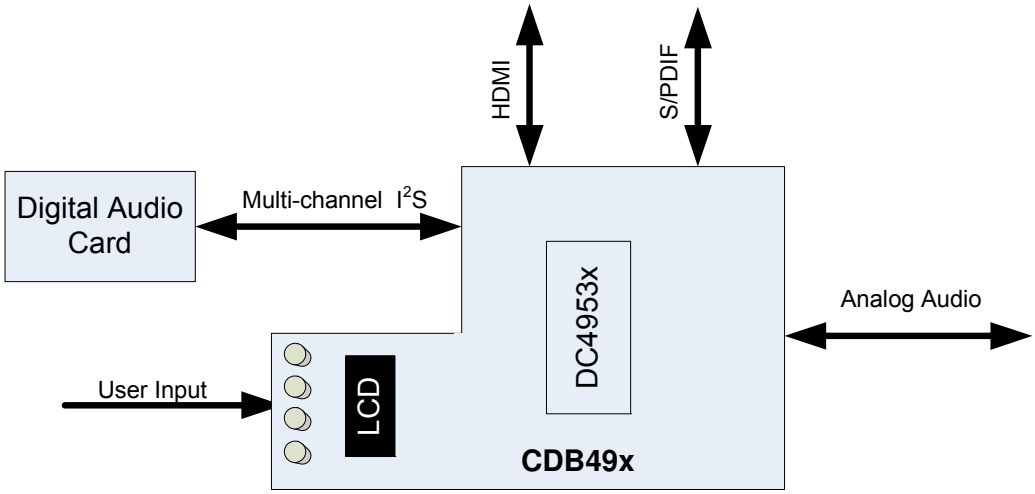


Figure 2-2. CK49x System Block Diagram in Standalone Mode

This document will concentrate on the features and basic operation of the CK49x board. Detailed information regarding the operation and programming of the CS4953x4 DSP is covered by the CS4953xx *Data Sheet*, the *CS4970x4/CS4953x4 System Designer's Guide* and the application note AN288. See Section 1.4 "DS898CK4Other Useful Information" on page 1-14 for more details.

The CK49x is a convenient and easy-to-operate evaluation platform. It has been designed to demonstrate the majority of the DSP functions on a 9" x 6.5" base board. These features include:

- PC control of the DSP using the DSP Composer™ graphical user interface
- Serial control of audio devices on CK49x Evaluation System via I²C™ or SPI™ protocols
- Digital audio input of PCM or compressed data via optical or coaxial S/PDIF
- Digital audio input of PCM or compressed data via HDMI
- 2-channel analog audio input via the CS42528 audio codec
- 8-channel analog output through the CS42528 audio codec
- Digital audio output of PCM data via optical S/PDIF
- Digital audio output of PCM or compressed data via HDMI (feature not currently supported)
- Multi-channel digital audio input via P11 header (feature not currently supported)
- Separate input and output clocking domains to allow 1FS-to-2FS audio processing on the DSP
- DSP Memory expansion through external 16-Mbit SDRAM
- Fast boot –master boot of custom applications from 32 Mbit serial SPI Flash device.
- Microphone input with integrated amplifier for Intelligent Room Calibration (IRC) evaluation
- Supports all members of the CS495xxx/CS4970x4 family in the 128-pin LQFP package.

Note: Not all features of the DSP are exercised on the CK49x. Evaluation System

2.2 Identifying Components on the CK49x Evaluation System

2.2.1 CDB49x Main Board Components

Figure 2-3 shows the top side of the CDB49x Main Board. The accompanying legend identifies the main components of the board. Section 2.2.1.1 contains the legend for the reference points called out in red in Figure 2-3.

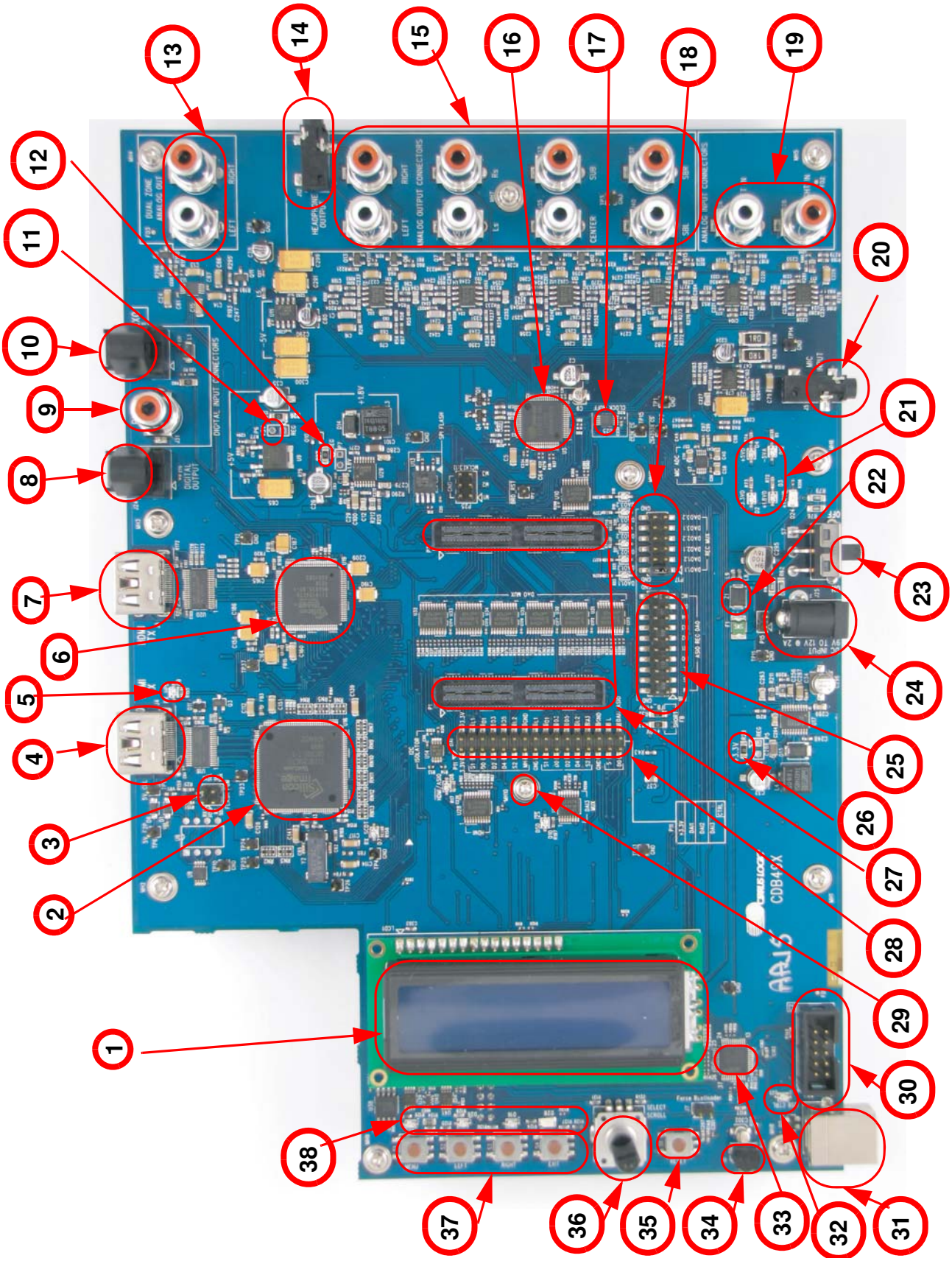


Figure 2-3. CDB49x Main Board Top View

2.2.1.1 CDB49x Main Board Components

The circled numbers found in Figure 2-3 refer to the CDB49x Main Board components in the following list:

1. LCD
2. HDMI Receiver (Rx)
3. Extended Display Identification Data (EDID) Programming Header
4. HDMI Input Connector
5. Hot Plug Indicator
6. HDMI Transmitter (Tx)
7. HDMI Output Connector
8. S/PDIF Optical Tx
9. S/PDIF Coax Rx
10. S/PDIF Optical Rx
11. +5V Header
12. +1.8V Header
13. Dual Zone Analog Outputs
14. Headphone Output
15. Main Analog Line-Level Outputs (Left/Right; Left Surround/Right Surround; Center/Subwoofer; Surround Back Left/Surround Back Right)
16. Cirrus Logic CS42528 CODEC
17. Cirrus Logic CS2000 Clock Generator and Clock Multiplier/Jitter-Reduced Clock Frequency Synthesizer
18. DAO Selection
19. Analog Line-Level Input
20. Mic Input
21. Power Indicator LEDs (4)
22. Slave Boot Control
23. Power Switch
24. +9V Power Connector
25. DAO Mux Header
26. +3.3V Header
27. Daughter Card Connectors (2)
28. DAI 1, 2, and 3 Header
29. DSD/I^2S Mux LED
30. MCU Programming Header (C2 Header)
31. USB Connector
32. USB Active LED
33. 8051 MCU