LT1578/LT1578-2.5

1.5A, 200kHz Step-Down Switching Regulator

FEATURES

- **1.5A Switch Current**
- **High Efficiency—Low Loss 0.2Ω Switch**
- **Constant 200kHz Switching Frequency**
- **4V to 15V Input VoltageRange**
- **Minimum Output: 1.21V**
- Low Supply Current: 1.9mA
- Low Shutdown Current: 20µA
- Easily Synchronizable Up to 400kHz
- Cycle-by-Cycle Current Limit
- Reduced EMI Generation
- Low Thermal Resistance SO-8 Package
- Uses Small Low Value Inductors

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Battery Chargers
- Distributed Power Systems

DESCRIPTION

The LT®1578 is a 200kHz monolithic buck mode switching regulator. A 1.5A switch is included on the die along with all the necessary oscillator, control and logic circuitry. The topology is current mode for fast transient response and good loop stability. The LT1578 is a modified version of the LT1507 that has been optimized for noise sensitive applications. It will operate over a 4V to 15V input range.

In addition, the reference voltage has been lowered to allow the device to produce output voltages down to 1.2V. Quiescent current has been reduced by a factor of two. Switch on resistance has been reduced by 30%. Switch transition times have been slowed to reduce EMI generation. The oscillator frequency has been reduced to 200kHz to maintain high efficiency over a wide output current range.

The pinout has been changed to improve PC layout by allowing the high current, high frequency switching circuitry to be easily isolated from low current, noise sensitive control circuitry. The new SO-8 package includes a fused ground lead that significantly reduces the thermal resistance of the device to extend the ambient operating temperature range. Standard surface mount external parts can be used including the inductor and capacitors.

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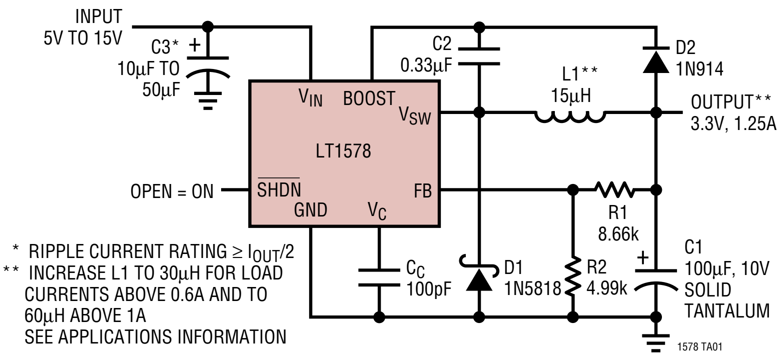
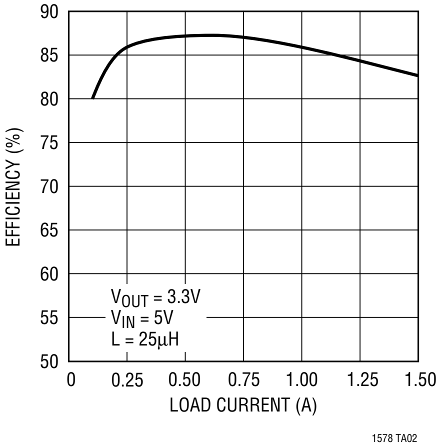
TYPICAL APPLICATION

3.3V Buck Converter



* RIPPLE CURRENT RATING ≥ $I_{OUT}/2$
** INCREASE L1 TO 30µH FOR LOAD CURRENTS ABOVE 0.6A AND TO 60µH ABOVE 1A
SEE APPLICATIONS INFORMATION

Efficiency vs Load Current

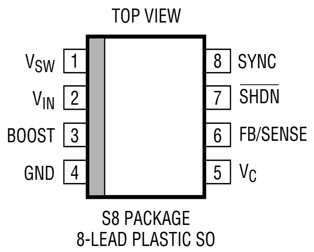


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage	16V
BOOST Pin Above Input Voltage	10V
$\overline{\text{SHDN}}$ Pin Voltage	7V
SENSE Pin Voltage	4V
FB Pin Voltage (Adjustable Part)	3.5V
FB Pin Current (Adjustable Part)	1mA
SYNC Pin Voltage	7V
Operating Junction Temperature Range	
LT1578C	0°C to 125° C
LT1578I	−40°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



θ_{JA} = 80°C/W WITH FUSED GROUND PIN CONNECTED TO GROUND PLANE OR LARGE LANDS

ORDER PART NUMBER	
LT1578CS8 LT1578IS8 LT1578CS8-2.5 LT1578IS8-2.5	
S8 PART MARKING	
1578	157825
1578I	578I25

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 5V, V_C = 1.5V, Boost = V_{IN} + 5V, switch open, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Voltage			1.195	1.21	1.225	V
	All Conditions	●	1.18		1.24	V
Sense Voltage (Fixed 2.5)			2.46	2.5	2.54	V
	All Conditions	●	2.44		2.56	V
Sense Pin Resistance			5.7	9.5	13.7	kΩ
Reference Voltage Line Regulation	4.3V ≤ V_{IN} ≤ 15V	●		0.01	0.03	%/V
Feedback Input Bias Current		●		0.5	2	µA
Error Amplifier Voltage Gain (Notes 2, 10)			200	400		
Error Amplifier Transconductance (Note 10)	ΔI (V_C) = ±10µA		800	1050	1300	µMho
		●	400		1700	µMho
V_C Pin to Switch Current Transconductance				1.5		A/V
Error Amplifier Source Current	V_{FB} = 1.1V	●	40	110	190	µA
Error Amplifier Sink Current	V_{FB} = 1.4V	●	50	130	200	µA
V_C Pin Switching Threshold	Duty Cycle = 0			0.8		V
V_C Pin High Clamp				2.1		V
Switch Current Limit	V_C Open, V_{FB} = 1.1V, DC ≤ 50%	●	1.5	2	3.5	A
Slope Compensation (Note 8)	DC = 80%			0.3		A
Switch On Resistance (Note 7)	I_{SW} = 1.5A			0.2	0.35	Ω
		●			0.45	Ω
Maximum Switch Duty Cycle	V_{FB} = 1.1V		90	94		%
		●	86	94		%
Minimum Switch Duty Cycle (Note 9)				8		%
Switch Frequency	V_C Set to Give 50% Duty Cycle		180	200	220	kHz
		●	160		240	kHz
Switch Frequency Line Regulation	4.3V ≤ V_{IN} ≤ 15V	●		0	0.15	%/V
Frequency Shifting Threshold on FB Pin	Δf = 10kHz	●	0.4	0.74	1.0	V
Minimum Input Voltage (Note 3)		●		4.0	4.3	V
Minimum Boost Voltage (Note 4)	I_{SW} ≤ 1.5A	●		2.3	3.0	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_J = 25°C$. $V_{IN} = 5V$, $V_C = 1.5V$, Boost = $V_{IN} + 5V$, switch open, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Current (Note 5)	$I_{SW} = 0.5A$ $I_{SW} = 1.5A$	● ●		9 27	18 50	mA mA
V_{IN} Supply Current (Note 6)		●		1.9	2.7	mA
Shutdown Supply Current	$V_{\overline{SHDN}} = 0V$, $V_{IN} \le 15V$, $V_{SW} = 0V$, V_C Open	 ●		20	50 75	µA µA
Lockout Threshold	V_C Open	●	2.34	2.42	2.50	V
Shutdown Thresholds	V_C Open Device Shutting Down Device Starting Up	● ●	0.13 0.25	0.37 0.45	0.60 0.7	V V
Synchronization Threshold				1.5	2.2	V
Synchronizing Range			250		400	kHz
SYNC Pin Input Resistance				40		kΩ

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Gain is measured with a V_C swing equal to 200mV above the switching threshold level to 200mV below the upper clamp level.

Note 3: Minimum input voltage is not measured directly, but is guaranteed by other tests. It is defined as the voltage where internal bias lines are still regulated so that the reference voltage and oscillator frequency remain constant. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 5: Boost current is the current flowing into the boost pin with the pin held 5V above input voltage. It flows only during switch on time.

Note 6: Input supply current is the bias current drawn by the input pin with switching disabled.

Note 7: Switch on resistance is calculated by dividing V_{IN} to V_{SW} voltage by the forced current (1.5A). See Typical Performance Characteristics for the graph of switch voltage at other currents.

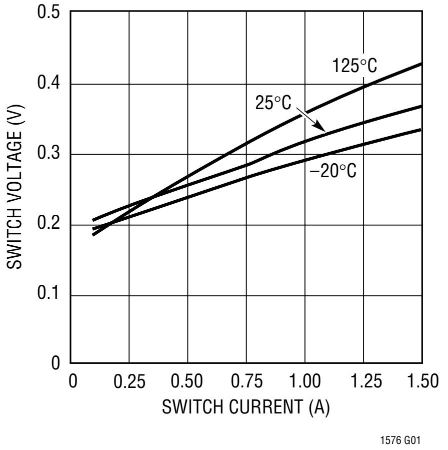
Note 8: Slope compensation is the current subtracted from the switch current limit at 80% duty cycle. See Maximum Output Load Current in the Applications Information section for further details.

Note 9: Minimum on-time is 400ns typical. For a 200kHz operating frequency this means the minimum duty cycle is 8%. In frequency foldback mode, the effective duty cycle will be less than 8%.

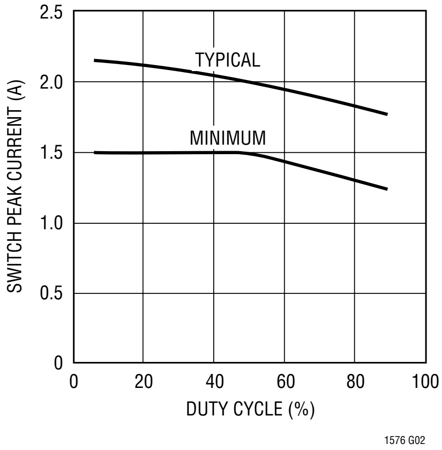
Note 10: Transconductance and voltage gain refer to the internal amplifier exclusive of the voltage divider. To calculate gain and transconductance referred to the sense pin on the fixed voltage parts, divide values shown by the ratio 2.5/1.21.

TYPICAL PERFORMANCE CHARACTERISTICS

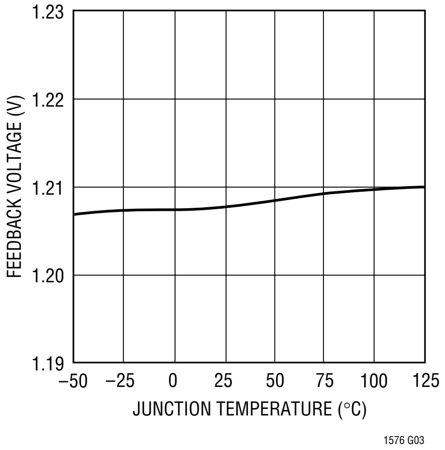
Switch Voltage Drop



Switch Peak Current Limit

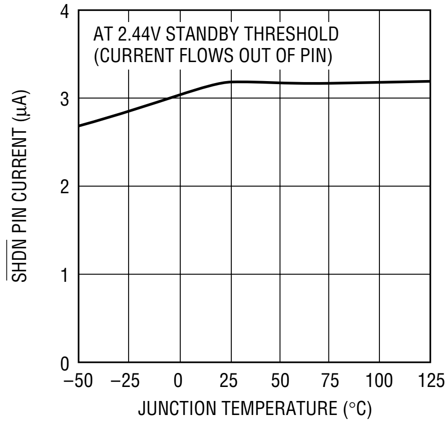


Feedback Pin Voltage



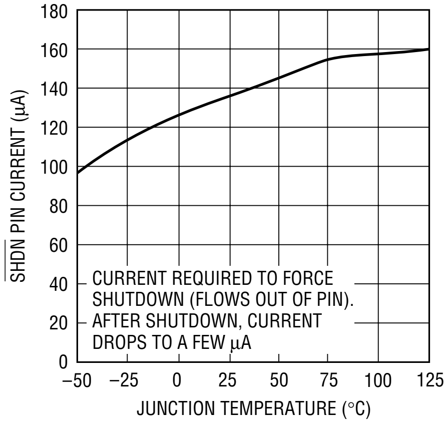
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Pin Bias Current ($V_{\overline{SHDN}}$ = Lockout Threshold)



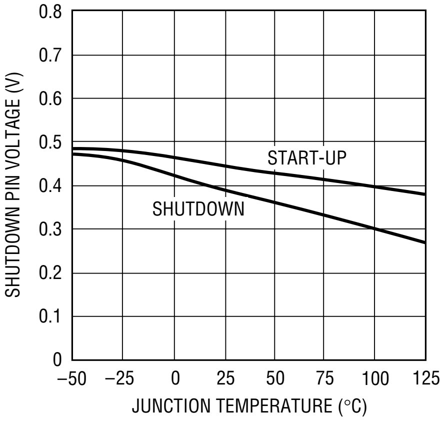
1576 G04

Shutdown Pin Bias Current ($V_{\overline{SHDN}}$ = Shutdown Threshold)



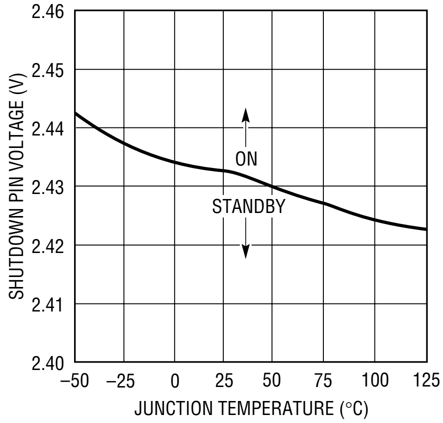
1576 G05

Shutdown Thresholds



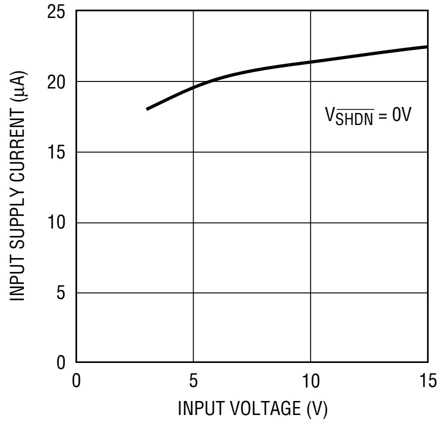
1576 G06

Standby Thresholds



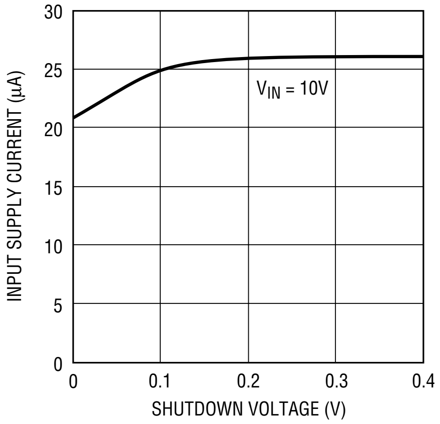
1576 G07

Shutdown Supply Current



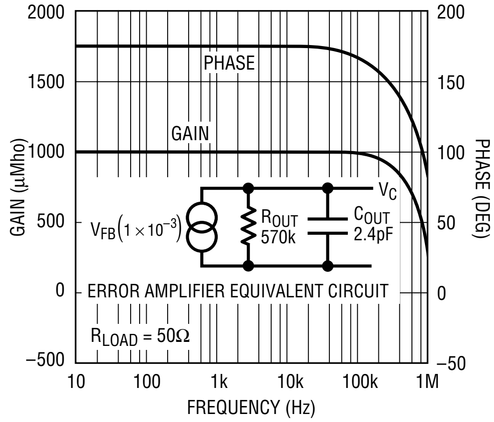
1576 G08

Shutdown Supply Current



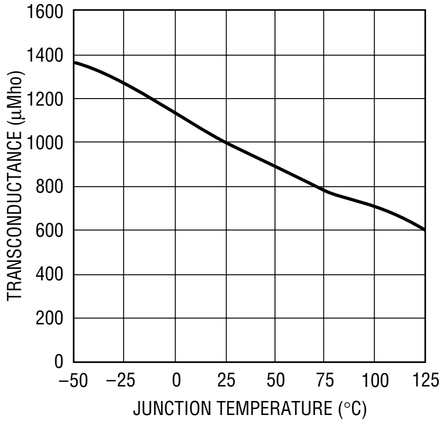
1576 G010

Error Amplifier Transconductance



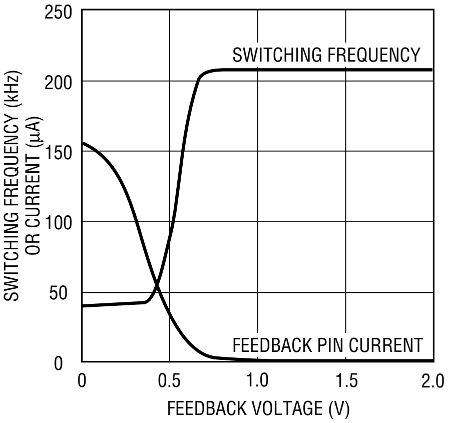
1576 G09

Error Amplifier Transconductance



1576 G11

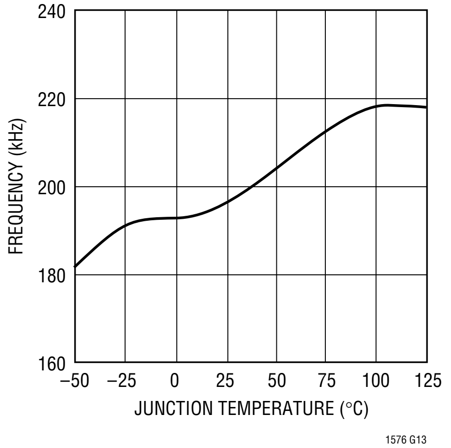
Frequency Foldback



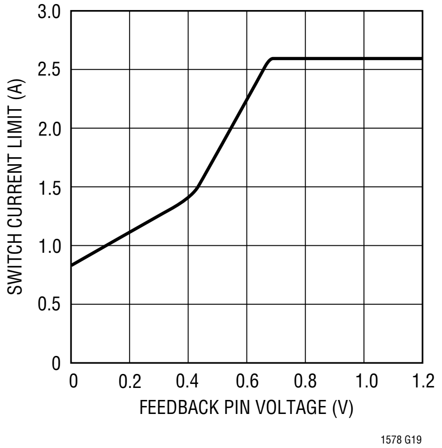
1576 G12

TYPICAL PERFORMANCE CHARACTERISTICS

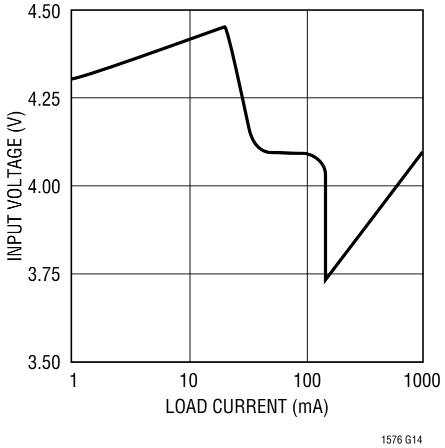
Switching Frequency



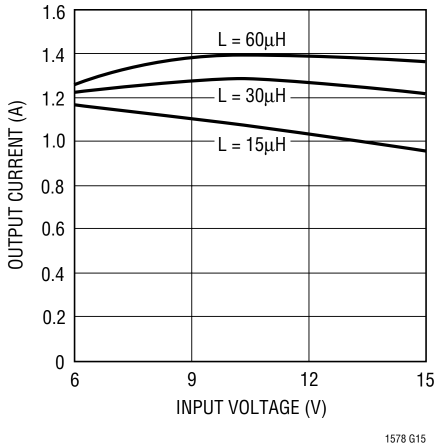
Switch Current Limit Foldback



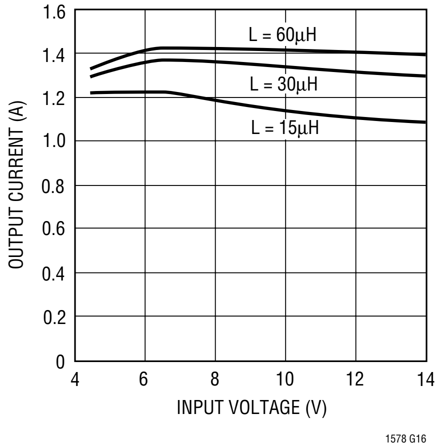
Minimum Input Voltage to Start with 3.3V Output



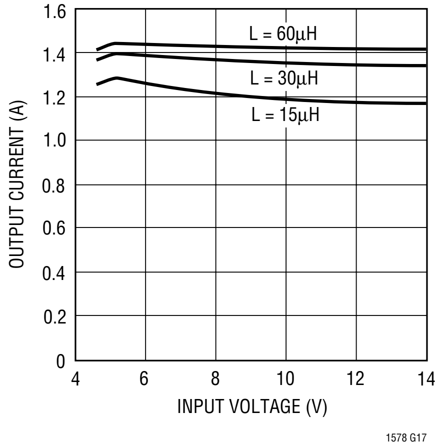
Maximum Output Current at V_{OUT} = 5V



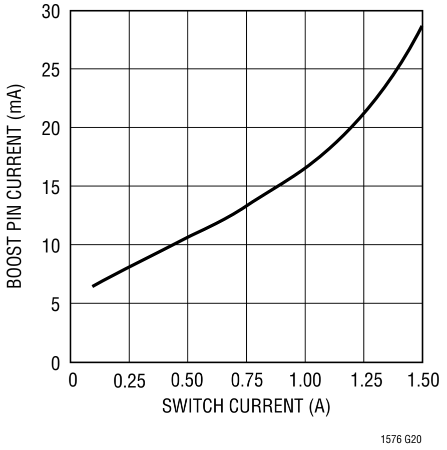
Maximum Output Current at V_{OUT} = 3.3V



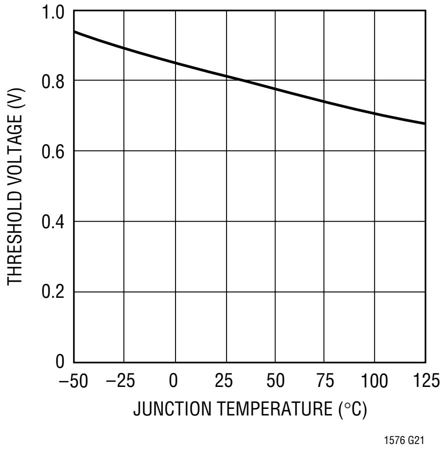
Maximum Output Current at V_{OUT} = 2.5V



BOOST Pin Current



V_C Pin Shutdown Threshold



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Metglas is a registered trademark of AlliedSignal, Inc.

PIN FUNCTIONS

V_{SW} (Pin 1): The switch pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the switch pin negative during switch off time. Negative voltage is clamped with the external catch diode. Maximum negative switch voltage allowed is –0.8V.

V_{IN} (Pin 2): This is the collector of the on-chip power NPN switch. This pin powers the internal circuitry and internal regulator. At NPN switch on and off, high dI/dt edges occur through this pin. Keep the external bypass and catch diode close to this pin. Trace inductance in this path will create a voltage spike at switch off, adding to the V_{CE} voltage across the internal NPN.

BOOST (Pin 3): The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional boost voltage allows the switch to saturate with its voltage drop approximating that of a 0.2Ω FET structure. Efficiency improves from 75% for conventional bipolar designs to >88% for the LT1578.

GND (Pin 4): The GND pin connection needs consideration for two reasons. First, it acts as the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND pin of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pin and the load ground point. Keep the ground path short between the GND pin and the load and use a ground plane when possible. The second consideration is EMI caused by GND pin current spikes. Internal capacitance between the V_{SW} pin and the GND pin creates very narrow (<10ns) current spikes in the GND pin. If the GND pin is connected to system ground with a long metal trace, this trace may radiate EMI. Keep the path between the input bypass and the GND pin short. The GND pin of the SO-8 package is directly attached to the internal tab. This pin should be attached to a large copper area to improve thermal resistance.

V_C (Pin 5): The V_C pin is the output of the error amplifier and the input to the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 1V for very light loads and 2V at maximum load. It can be driven to ground to shut off the regulator, but if driven high, current must be limited to 4mA.

FB/SENSE (Pin 6): The feedback pin is used to set output voltage using an external voltage divider that generates 1.21V at the pin with the desired output voltage. The fixed voltage (2.5V) parts have the divider included on the chip and the FB pin is used as a sense pin, connected directly to the 2.5V output. Three additional functions are performed by the FB pin. When the pin voltage drops below 0.7V, the switch current limit and the switching frequency are reduced and the external sync function is disabled. See Feedback Pin Function section in Applications Information for details.

$\overline{\text{SHDN}}$ (Pin 7): The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. Actually, this pin has two separate thresholds, one at 2.42V to disable switching, and a second at 0.4V to force complete micropower shutdown. The 2.42V threshold functions as an accurate undervoltage lockout (UVLO). This can be used to prevent the regulator from operating until the input voltage has reached a predetermined level.

SYNC (Pin 8): The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. The synchronizing range is equal to *initial* operating frequency, up to 400kHz. When not used, this pin should be grounded. See Synchronizing section in Applications Information for details.

BLOCK DIAGRAM

The LT1578 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the R_S flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing the switch to saturate. This boosted voltage is generated with an external capacitor and diode. Two comparators are connected to the shutdown pin. One has a 2.42V threshold for undervoltage lockout and the second has a 0.4V threshold for complete shutdown.

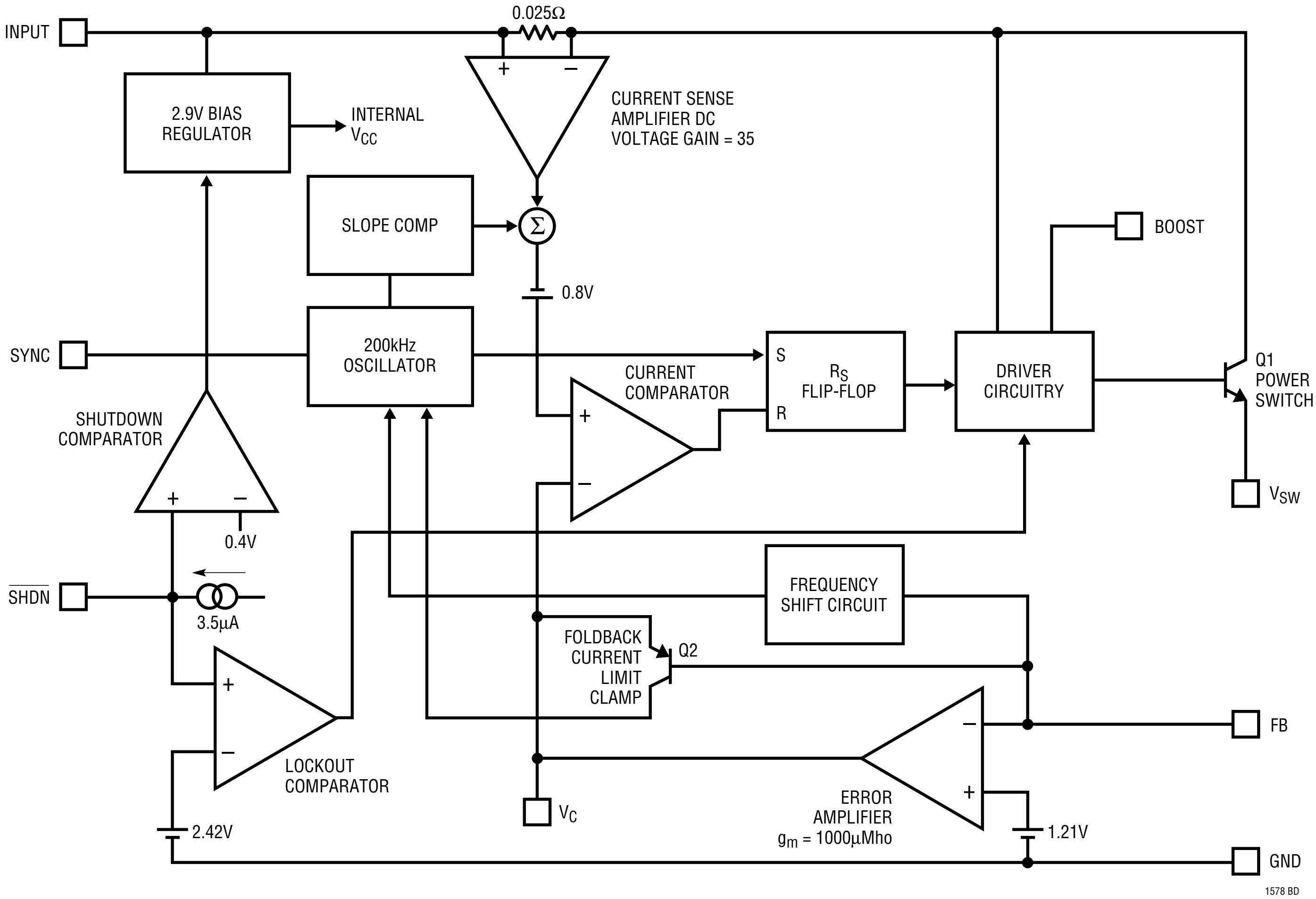
INPUT
0.025Ω
+
−
2.9V BIAS REGULATOR
INTERNAL V_{CC}
CURRENT SENSE AMPLIFIER DC VOLTAGE GAIN = 35
SLOPE COMP
Σ
BOOST
0.8V
SYNC
200kHz OSCILLATOR
S
R_S FLIP-FLOP
R
CURRENT COMPARATOR
DRIVER CIRCUITRY
Q1 POWER SWITCH
SHUTDOWN COMPARATOR
V_{SW}
0.4V
SHDN
3.5µA
FREQUENCY SHIFT CIRCUIT
FOLDBACK CURRENT LIMIT CLAMP
Q2
FB
LOCKOUT COMPARATOR
ERROR AMPLIFIER g_m = 1000µMho
V_C
2.42V
1.21V
GND
1578 BD

Figure 1. Block Diagram

APPLICATIONS INFORMATION

FEEDBACK PIN FUNCTIONS

The feedback (FB) pin on the LT1578 is used to set output voltage and provide several overload protection features. The first part of this section deals with selecting resistors to set output voltage and the remaining part talks about foldback frequency and current limiting created by the FB pin. Please read both parts before committing to a final design. The fixed 2.5V LT1578-2.5 has internal divider resistors and the FB pin, renamed SENSE, is connected directly to the 2.5V output.

The suggested value for the output divider resistor (see Figure 2) from FB to ground (R2) is 5k or less, and a formula for R1 is shown below. The output voltage error caused by ignoring the input bias current on the FB pin is less than 0.25% with R2 = 5k. Please read the following if divider resistors are increased above the suggested values.

$$R1 = \frac{R2\left(V_{OUT} - 1.21\right)}{1.21}$$

More Than Just Voltage Feedback

The feedback pin is used for more than just output voltage sensing. It also reduces switching frequency and current limit when output voltage is very low (see the Frequency Foldback graph in Typical Performance Characteristics). This is done to control power dissipation in both the IC and the external diode and inductor during short-circuit conditions. A shorted output requires the switching regulator to operate at very low duty cycles, and the average current through the diode and inductor is equal to the short-circuit current limit of the switch (typically 2A for the LT1578, folding back to less than 0.77A). Minimum switch on time limitations would prevent the switcher from attaining a sufficiently low duty cycle if switching frequency were maintained at 200kHz, so frequency is reduced by about 5:1 when the feedback pin voltage drops below 0.7V (see Frequency Foldback graph). This does not affect operation with normal load conditions; one simply sees a gear shift in switching frequency during start-up as the output voltage rises.

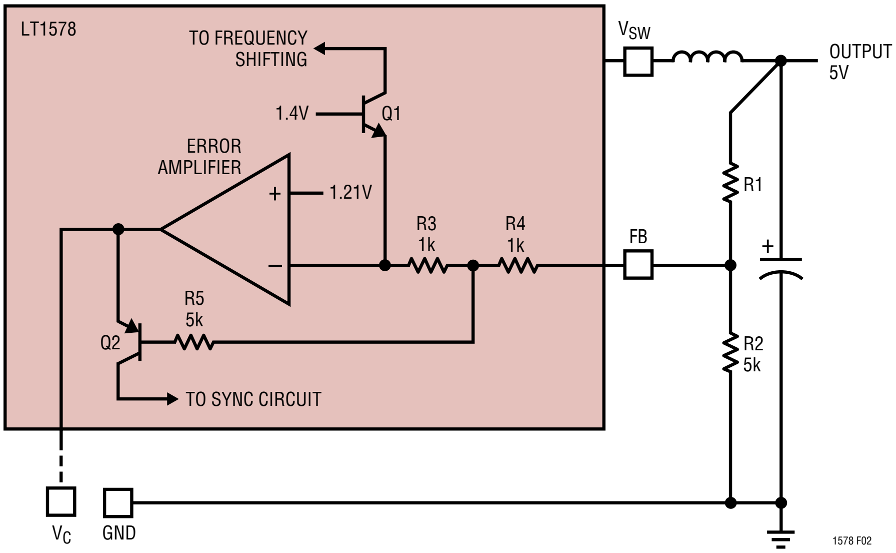

Figure 2. Frequency and Current Limit Foldback

APPLICATIONS INFORMATION

In addition to lower switching frequency, the LT1578 also operates at lower switch current limit when the feedback pin voltage drops below 0.7V. Q2 in Figure 2 performs this function by clamping the V_C pin to a voltage less than its normal 2.1V upper clamp level. This *foldback current limit* greatly reduces power dissipation in the IC, diode and inductor during short-circuit conditions. External synchronization is also disabled to prevent interference with foldback operation. Again, it is nearly transparent to the user under normal load conditions. The only loads that may be affected are current sources, such as lamps and motors, that maintain high load current with output voltage less than 50% of final value. In these rare situations the feedback pin can be clamped above 0.7V to defeat foldback current limit. *Caution:* clamping the feedback pin means that frequency shifting will also be defeated, so a combination of high input voltage and dead shorted output may cause the LT1578 to lose control of current limit.

The internal circuitry which forces reduced switching frequency also causes current to flow out of the feedback pin when output voltage is low. The equivalent circuitry is shown in Figure 2. Q1 is completely off during normal operation. If the FB pin falls below 0.7V, Q1 begins to conduct current and reduces frequency at the rate of approximately 1kHz/µA. To ensure adequate frequency foldback (under worst-case short-circuit conditions), the external divider Thevinin resistance must be low enough to pull 35µA out of the FB pin with 0.5V on the pin ($R_{DIV} \leq$ 14.3k). *The net result is that reductions in frequency and current limit are affected by output voltage divider impedance. Although divider impedance is not critical, caution should be used if resistors are increased beyond the suggested values and short-circuit conditions will occur with high input voltage*. High frequency pickup will increase and the protection accorded by frequency and current foldback will decrease.

MAXIMUM OUTPUT LOAD CURRENT

Maximum load current for a buck converter is limited by the maximum switch current rating (I_P) of the LT1578. This current rating is 1.5A up to 50% duty cycle (DC), decreasing to 1.3A at 80% duty cycle. This is shown graphically in Typical Performance Characteristics and as shown in the formula below:

$$I_P = 1.5\text{A for DC} \leq 50\%$$
$$I_P = 1.67 - 0.18\,(\text{DC}) - 0.32(\text{DC})^2 \text{ for } 50\% < \text{DC} < 90\%$$

DC = Duty cycle = V_{OUT}/V_{IN}

Example: with $V_{OUT} = 5V$, $V_{IN} = 8V$; DC = 5/8 = 0.625, and;

$$I_{SW(MAX)} = 1.67 - 0.18\,(0.625) - 0.32(0.625)^2 = 1.43\text{A}$$

Current rating decreases with duty cycle because the LT1578 has internal slope compensation to prevent current mode subharmonic switching. For more details, read Application Note 19. The LT1578 is a little unusual in this regard because it has nonlinear slope compensation which gives better compensation with less reduction in current limit.

Maximum load current would be equal to maximum switch current *for an infinitely large inductor*, but with finite inductor size, maximum load current is reduced by one-half peak-to-peak inductor current. The following formula assumes continuous mode operation, implying that the term on the right is less than one-half of I_P.

$$\begin{array}{l} I_{OUT(MAX)} = \\ \text{Continuous Mode} \end{array} \quad I_P - \frac{\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}{2\left(L\right)\left(f\right)\left(V_{IN}\right)}$$

For the conditions above and L = 15µH,

$$I_{OUT(MAX)} = 1.43 - \frac{\left(5\right)\left(8-5\right)}{2\left(15 \bullet 10^{-6}\right)\left(200 \bullet 10^{3}\right)\left(8\right)}$$
$$= 1.43 - 0.31 = 1.12\text{A}$$

At $V_{IN} = 15V$, duty cycle is 33%, so I_P is just equal to a fixed 1.5A, and $I_{OUT(MAX)}$ is equal to:

$$1.5 - \frac{\left(5\right)\left(15-5\right)}{2\left(15 \bullet 10^{-6}\right)\left(200 \bullet 10^{3}\right)\left(15\right)}$$
$$= 1.5 - 0.56 = 0.94\text{A}$$

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Note that there is less load current available at the higher input voltage because inductor ripple current increases. This is not always the case. Certain combinations of inductor value and input voltage range may yield lower available load current at the lowest input voltage due to reduced peak switch current at high duty cycles. If load current is close to the maximum available, please check maximum available current at both input voltage extremes. To calculate actual peak switch current with a given set of conditions, use:

$$I_{SW(PEAK)} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2(L)(f)\left(V_{IN}\right)}$$

For lighter loads where discontinuous operation can be used, maximum load current is equal to:

$$I_{OUT(MAX)} = \text{Discontinuous mode} \quad \frac{\left(I_P\right)^2(f)(L)\left(V_{IN}\right)}{2\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}$$

Example: with L = 5μH, V_{OUT} = 5V, and $V_{IN(MAX)}$ = 15V,

$$I_{OUT(MAX)} = \frac{(1.5)^2\left(200 \bullet 10^3\right)\left(5 \bullet 10^{-6}\right)(15)}{2(5)(15-5)} = 0.34A$$

The main reason for using such a tiny inductor is that it is physically very small, but keep in mind that peak-to-peak inductor current will be very high. This will increase output ripple voltage. If the output capacitor has to be made larger to reduce ripple voltage, the overall circuit could actually wind up larger.

CHOOSING THE INDUCTOR AND OUTPUT CAPACITOR

For most applications the output inductor will fall in the range of 15μH to 60μH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the LT1578 switch, which has a 1.5A limit. Higher values also reduce output ripple voltage, and reduce core loss. Graphs in the Typical Performance Characteristics section show maximum output load current versus inductor size and input voltage.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation, and of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Choose a value in microhenries from the graphs of maximum load current and core loss. Choosing a small inductor may result in discontinuous mode operation at lighter loads, but the LT1578 is designed to work well in either mode. Keep in mind that lower core loss means higher cost, at least for closed core geometries like toroids.

   Assume that the average inductor current is equal to load current and decide whether or not the inductor must withstand continuous fault conditions. If maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Dead shorts will actually be more gentle on the inductor because the LT1578 has foldback current limiting.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall somewhere in between. The following formula assumes continuous mode of operation, but it errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

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$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2\left(f\right)\left(L\right)\left(V_{IN}\right)}$$

V_{IN} = Maximum input voltage
f = Switching frequency, 200kHz

3. Decide if the design can tolerate an "open" core geometry like a rod or barrel, with high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. One would not want an open core next to a magnetic storage media, for instance! This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.
4. Start shopping for an inductor (see representative surface mount units in Table 1) which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating), and fault current (if the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts). Keep in mind that all good things like high efficiency, low profile, and high temperature operation will increase cost, sometimes dramatically. Get a quote on the cheapest unit first to calibrate yourself on price, then ask for what you really want.
5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology's applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Table 1

VENDOR/ PART NO.	VALUE (μH)	DC (Amps)	CORE TYPE	SERIES RESISTANCE(Ω)	CORE MATERIAL	HEIGHT (mm)
Coiltronics						
CTX15-2	15	1.7	Tor	0.059	KMμ	6.0
CTX33-2	33	1.4	Tor	0.106	KMμ	6.0
CTX68-4	68	1.2	Tor	0.158	KMμ	6.4
CTX15-1P	15	1.4	Tor	0.087	52	4.2
CTX33-2P	33	1.3	Tor	0.126	52	6.0
CTX68-4P	68	1.1	Tor	0.238	52	6.4
Sumida						
CDRH74-150	15	1.47	SC	0.081	Fer	4.5
CDH115-330	33	1.68	SC	0.082	Fer	5.2
CDRH125-680	68	1.5	SC	0.12	Fer	6
CDH74-330	33	1.45	SC	0.17	Fer	5.2
Coilcraft						
DO3308P-153	15	2	SC	0.12	Fer	3
DO3316P-333	33	2	SC	0.1	Fer	5.21
DO3316P-683	68	1.4	SC	0.18	Fer	5.21
Pulse						
PE-53602	35	1.4	Tor	0.166	Fer	9.1
PE-53604	73	1.3	Tor	0.290	Fer	9.1
PE-53632	22	2.7	Tor	0.063	Fer	9.1
PE-53633	40	2.7	Tor	0.085	Fer	10
Gowanda						
SMP3316-152K	15	3.5	SC	0.041	Fer	6
SMP3316-332K	33	2.3	SC	0.092	Fer	6
SMP3316-682K	68	1.7	SC	0.178	Fer	6

Tor = Toroid
SC = Semi-closed geometry
Fer = Ferrite core material
52 = Type 52 powdered iron core material
KMμ = Kool Mμ

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Output Capacitor

The output capacitor is normally chosen by its Effective Series Resistance (ESR), because this is what determines output ripple voltage. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT1578 applications is 0.05Ω to 0.2Ω. A typical output capacitor is an AVX type TPS, 100µF at 10V, with a guaranteed ESR less than 0.1Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR, and output ripple voltage will be terrible. Table 2 shows some typical solid tantalum surface mount capacitors.

Table 2. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E Case Size	ESR (Max., Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
C Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true, and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Unlike the input capacitor, RMS ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular with a typical value of 200mA$_{RMS}$. The formula to calculate this is:

Output Capacitor Ripple Current (RMS):

$$I_{RIPPLE(RMS)} = \frac{0.29\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}{\left(L\right)\left(f\right)\left(V_{IN}\right)}$$

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor's ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before their ESR provides any damping. They are appropriate for input bypassing because of their high ripple current ratings and tolerance of turn-on surges.

OUTPUT RIPPLE VOLTAGE

Figure 3 shows a typical output ripple voltage waveform for the LT1578. Ripple voltage is determined by the high frequency impedance of the output capacitor, and ripple current through the inductor. Peak-to-peak ripple current through the inductor into the output capacitor is:

$$I_{P\text{-}P} = \frac{\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)}{\left(V_{IN}\right)\left(L\right)\left(f\right)}$$

For high frequency switchers, the sum of ripple current slew rates may also be relevant and can be calculated from:

$$\Sigma\frac{dI}{dt} = \frac{V_{IN}}{L}$$

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Peak-to-peak output ripple voltage is the sum of a *triwave* created by peak-to-peak ripple current times ESR, and a *square* wave created by parasitic inductance (ESL) and ripple current slew rate. Capacitive reactance is assumed to be small compared to ESR or ESL.

$$V_{RIPPLE} = \left(I_{P\text{-}P}\right)\left(ESR\right) + \left(ESL\right)\Sigma\frac{dI}{dt}$$

Example: with $V_{IN} = 10V$, $V_{OUT} = 5V$, $L = 30\mu H$, $ESR = 0.1\Omega$, ESL = 10nH:

$$I_{P\text{-}P} = \frac{\left(5\right)\left(10-5\right)}{\left(10\right)\left(30 \bullet 10^{-6}\right)\left(200 \bullet 10^{3}\right)} = 0.42A$$

$$\Sigma\frac{dI}{dt} = \frac{10}{30 \bullet 10^{-6}} = 0.33 \bullet 10^{6}$$

$$V_{RIPPLE} = \left(0.42A\right)\left(0.1\right) + \left(10 \bullet 10^{-9}\right)\left(0.33 \bullet 10^{6}\right)$$

$$= 0.042 + 0.003 = 45mV_{P\text{-}P}$$

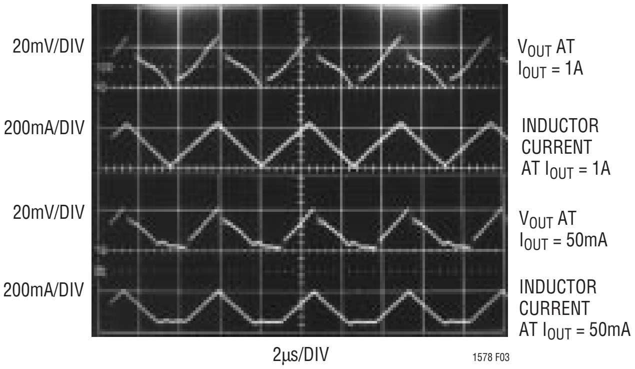

Figure 3. LT1578 Ripple Voltage Waveform

CATCH DIODE

The suggested catch diode (D1) is a 1N5818 Schottky, or its Motorola equivalent, MBR130. It is rated at 1A average forward current and 30V reverse voltage. Typical forward voltage is 0.42V at 1A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator input voltage. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}$$

This formula will not yield values higher than 1A with maximum load current of 1.25A unless the ratio of input to output voltage exceeds 5:1. The only reason to consider a larger diode is the worst-case condition of a high input voltage and *overloaded* (not shorted) output. Under short-circuit conditions, foldback current limit will reduce diode current to less than 1A, but if the output is overloaded and does not fall to less than 1/3 of nominal output voltage, foldback will not take effect. With the overloaded condition, output current will increase to a typical value of 1.8A, determined by peak switch current limit of 2A. With V_{IN} = 15V, V_{OUT} = 4V (5V overloaded) and I_{OUT} = 1.8A:

$$I_{D(AVG)} = \frac{1.8\left(15-4\right)}{15} = 1.32A$$

This is safe for short periods of time, but it would be prudent to check with the diode manufacturer if continuous operation under these conditions must be tolerated.

BOOST PIN CONSIDERATIONS

For most applications, the boost components are a 0.33µF capacitor and a 1N914 or 1N4148 diode. The anode is connected to the regulated output voltage and this generates a voltage across the boost capacitor nearly identical to the regulated output. In certain applications, the anode may instead be connected to the unregulated input voltage. This could be necessary if the regulated output voltage is very low (< 3V) or if the input voltage is less than 6V. Efficiency is not affected by the capacitor value, but the capacitor should have an ESR of less than 1Ω to ensure that it can be recharged fully under the worst-case condition of minimum input voltage. Almost any type of film or ceramic capacitor will work fine.

WARNING! Peak voltage on the BOOST pin is the sum of unregulated input voltage plus the voltage across the

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boost capacitor. This normally means that peak BOOST pin voltage is equal to input voltage plus output voltage, but *when the boost diode is connected to the regulator input, peak BOOST pin voltage is equal to twice the input voltage. Be sure that BOOST pin voltage does not exceed its maximum rating*.

For nearly all applications, a 0.33µF boost capacitor works just fine, but for the curious, more details are provided here. The size of the boost capacitor is determined by switch drive current requirements. During switch on time, drain current on the capacitor is approximately $I_{OUT}/50$. At peak load current of 1.25A, this gives a total drain of 25mA. Capacitor ripple voltage is equal to the product of on time and drain current divided by capacitor value; $\Delta V = (t_{ON})(25mA/C)$. To keep capacitor ripple voltage to less than 0.5V (a slightly arbitrary number) at the worst-case condition of $t_{ON} = 4.7\mu s$, the capacitor needs to be 0.24µF. Boost capacitor ripple voltage is not a critical parameter, but if the minimum voltage across the capacitor drops to less than 3V, the power switch may not saturate fully and efficiency will drop. An *approximate* formula for absolute minimum capacitor value is:

$$C_{MIN} = \frac{\left(I_{OUT}/50\right)\left(V_{OUT}/V_{IN}\right)}{\left(f\right)\left(V_{OUT} - 3V\right)}$$

f = Switching frequency
V_{OUT} = Regulated output voltage
V_{IN} = Minimum input voltage

This formula can yield capacitor values substantially less than 0.24µF, but it should be used with caution since it does not take into account secondary factors such as capacitor series resistance, capacitance shift with temperature and output overload.

SHUTDOWN FUNCTION AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT1578. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. It is particularly useful for input supplies with foldback current limiting. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit and latch under low source voltage

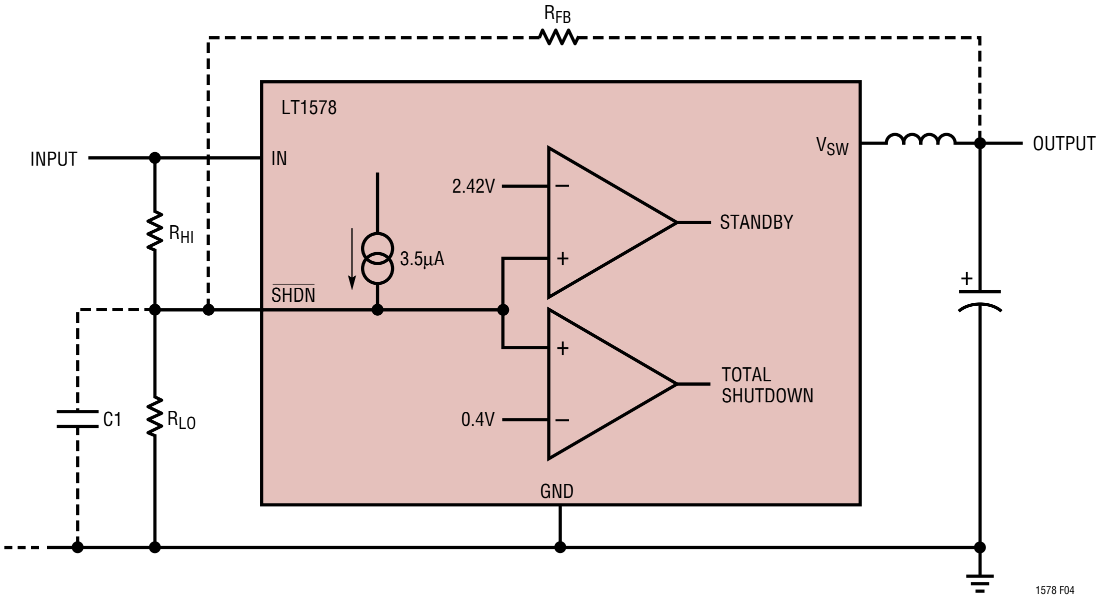

Figure 4. Undervoltage Lockout

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conditions. UVLO helps prevent the regulator from operating at source voltages where these problems might occur.

Threshold voltage for lockout is about 2.42V. A 3.5µA bias current flows *out* of the pin at threshold. This internally generated current is used to force a default high state on the shutdown pin if the pin is left open. When low shutdown current is not an issue, the error due to this current can be minimized by making R_{LO} 10k or less. If shutdown current is an issue, R_{LO} can be raised to 100k, but the error due to initial bias current and changes with temperature should be considered.

$$R_{LO} = 10k \text{ to } 100k \left(25k \text{ suggested}\right)$$

$$R_{HI} = \frac{R_{LO}\left(V_{IN} - 2.42V\right)}{2.42V - R_{LO}\left(3.5\mu A\right)}$$

V_{IN} = Minimum input voltage

Keep the connections from the resistors to the shutdown pin short and make sure that interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the shutdown pin should be bypassed with a 1000pF capacitor to prevent coupling problems from the switch node. If hysteresis is desired in the undervoltage lockout point, a resistor R_{FB} can be added to the output node. Resistor values can be calculated from:

$$R_{HI} = \frac{R_{LO}\left[V_{IN} - 2.42\left(\Delta V / V_{OUT} + 1\right) + \Delta V\right]}{2.42 - R_{LO}\left(3.5\mu A\right)}$$

$$R_{FB} = \left(R_{HI}\right)\left(V_{OUT} / \Delta V\right)$$

25k suggested for R_{LO}

V_{IN} = Input voltage at which switching stops as input voltage descends to trip level

ΔV = Hysteresis in input voltage level

Example: output voltage is 5V, switching is to stop if input voltage drops below 12V and should not restart unless input rises back to 13.5V. ΔV is therefore 1.5V and V_{IN} = 12V. Let R_{LO} = 25k.

$$R_{HI} = \frac{25k\left[12 - 2.42\left(1.5/5 + 1\right) + 1.5\right]}{2.42 - 25k\left(3.5\mu A\right)}$$

$$= \frac{25k\left(10.35\right)}{2.33} = 111k$$

$$R_{FB} = 111k\left(5/1.5\right) = 370k$$

SWITCH NODE CONSIDERATIONS

For maximum efficiency, switch rise and fall times are made as short as possible. To prevent radiated EMI and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping catch diode, switch pin, and input bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin and BOOST pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling. A suggested layout for the critical components is shown in Figure 5. Note that the feedback resistors and compensation components are kept as far as possible from the switch node. Also note that the high current ground path of the catch diode and input capacitor are kept very short and separate from the analog ground line.

The high speed switching current path is shown schematically in Figure 6. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, catch diode, and input capacitor is the only one containing nanosecond rise and fall times. If you follow this path on the PC layout, you will see that it is irreducibly short. If you move the diode or input capacitor away from the LT1578, get your resumé in order. The other paths contain only some combination of DC and 200kHz triwave, so are much less critical.

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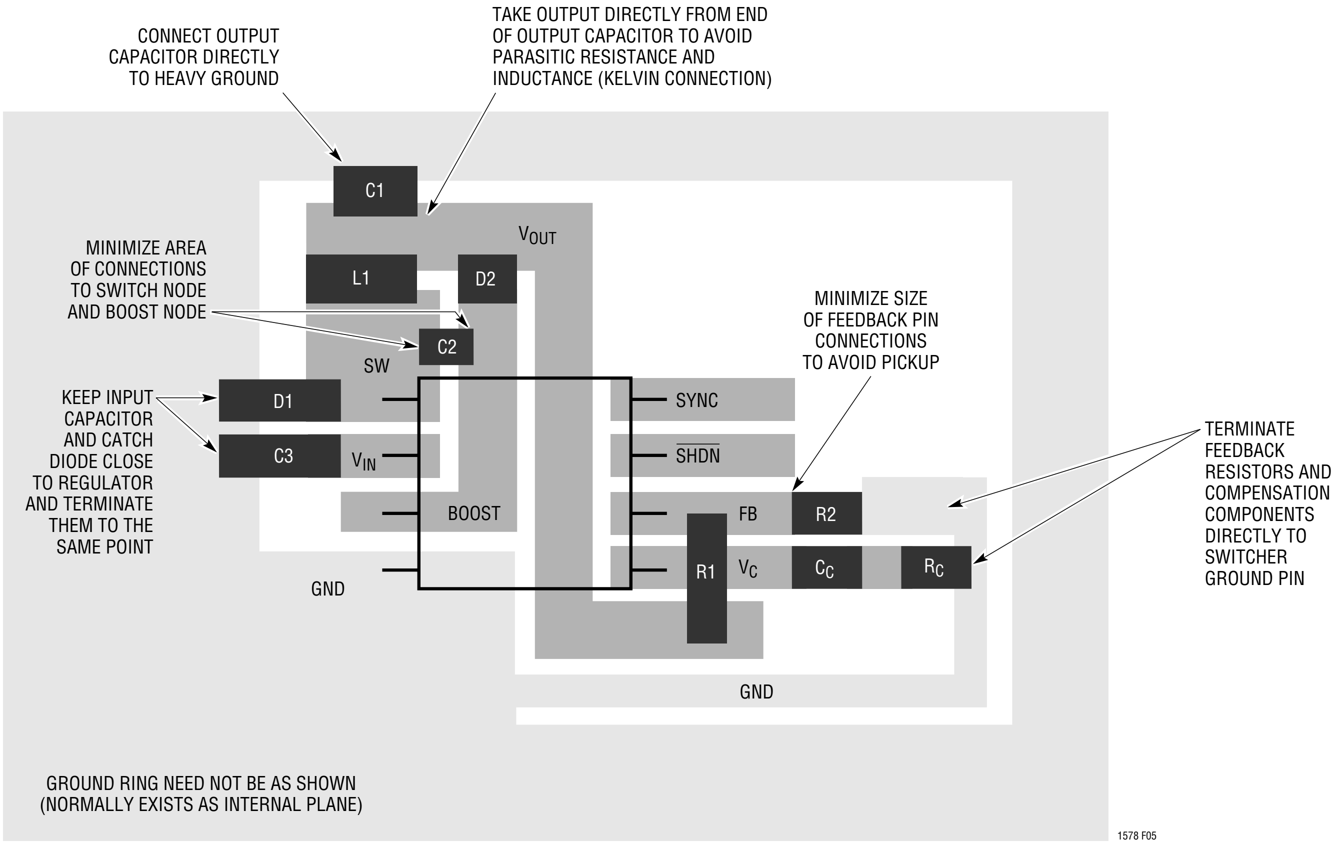
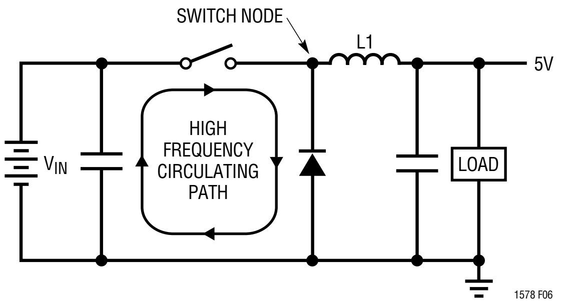


CONNECT OUTPUT CAPACITOR DIRECTLY TO HEAVY GROUND
TAKE OUTPUT DIRECTLY FROM END OF OUTPUT CAPACITOR TO AVOID PARASITIC RESISTANCE AND INDUCTANCE (KELVIN CONNECTION)
C1
V_{OUT}
MINIMIZE AREA OF CONNECTIONS TO SWITCH NODE AND BOOST NODE
L1
D2
C2
SW
MINIMIZE SIZE OF FEEDBACK PIN CONNECTIONS TO AVOID PICKUP
KEEP INPUT CAPACITOR AND CATCH DIODE CLOSE TO REGULATOR AND TERMINATE THEM TO THE SAME POINT
D1
C3
V_{IN}
SYNC
$\overline{SHDN}$
BOOST
FB
R2
TERMINATE FEEDBACK RESISTORS AND COMPENSATION COMPONENTS DIRECTLY TO SWITCHER GROUND PIN
R1
V_C
C_C
R_C
GND
GND
GROUND RING NEED NOT BE AS SHOWN (NORMALLY EXISTS AS INTERNAL PLANE)
1578 F05

Figure 5. Suggested Layout for LT1578



SWITCH NODE
L1
5V
V_{IN}
HIGH FREQUENCY CIRCULATING PATH
LOAD
1578 F06

Figure 6. High Speed Switching Path

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PARASITIC RESONANCE

Resonance or "ringing" may sometimes be seen on the switch node (see Figure 7). Very high frequency ringing following the switch voltage rise time is caused by switch/diode/input capacitance lead inductance and diode capacitance. Schottky diodes have very high "Q" junction capacitance that can ring for many cycles when excited at high frequency. If total lead length for the input capacitor, diode and switch path is 1 inch, the inductance will be approximately 25nH. At switch off, this will produce a spike across the NPN output device in addition to the input voltage. At higher currents this spike can be in the order of 10V to 20V or higher with a poor layout, potentially exceeding the absolute max switch voltage. The path around switch, catch diode and input capacitor must be kept as short as possible to ensure reliable operation. When looking at this, a >100MHz oscilloscope must be used, and waveforms should be observed on the leads of the package. This switch off spike will also cause the SW node to go below ground. The LT1578 has special circuitry inside which mitigates this problem, but negative voltages over 1V lasting longer than 10ns should be avoided. Note that 100MHz oscilloscopes are barely fast enough to see the details of the falling edge overshoot in Figure 7.

A second, much lower frequency ringing is seen during switch off time if load current is low enough to allow the inductor current to fall to zero during part of the switch off time (see Figure 8). Switch and diode capacitance resonate with the inductor to form damped ringing at 1MHz to 10 MHz. This ringing is not harmful to the regulator and it has not been shown to contribute significantly to EMI. Any attempt to damp it with an RC snubber will slightly degrade efficiency.

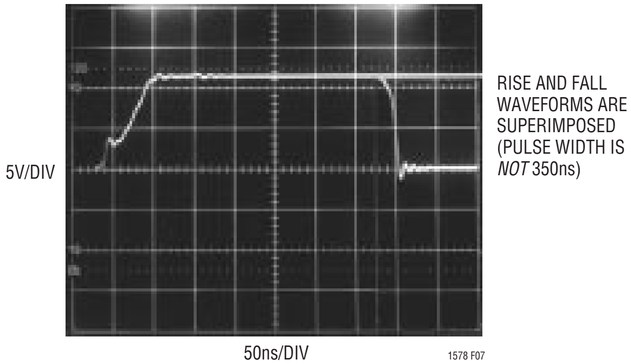

Figure 7. Switch Node Response

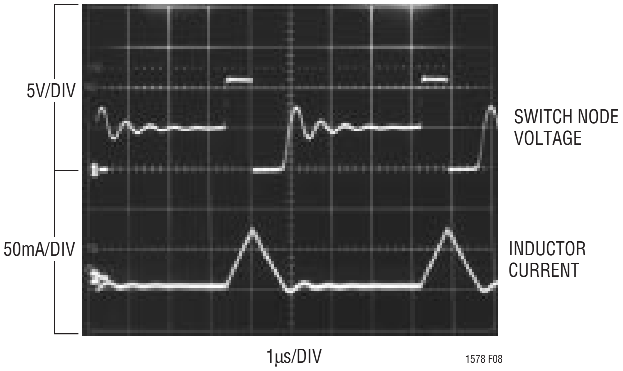

Figure 8. Discontinuous Mode Ringing

INPUT BYPASSING AND VOLTAGE RANGE

Input Bypass Capacitor

Step-down converters draw current from the input supply in pulses. The average height of these pulses is equal to load current, and the duty cycle is equal to V_{OUT}/V_{IN}. Rise and fall times of the current are very fast. A local bypass capacitor across the input supply is necessary to ensure proper operation of the regulator and minimize the ripple current fed back into the input supply. *The capacitor also forces switching current to flow in a tight local loop, minimizing EMI.*

Do not cheat on the ripple current rating of the input bypass capacitor, but also do not be overly concerned with the value in microfarads. The input capacitor is intended to absorb all the switching current ripple, which can have an RMS value as high as one half of the load current. Ripple current ratings on the capacitor must be observed to ensure reliable operation. In many cases it is necessary to parallel two capacitors to obtain the required ripple rating. Both capacitors must be of the same value and manufacturer to guarantee power sharing. The actual value of the capacitor in microfarads is not particularly important

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because at 200kHz, any value above 15μF is essentially resistive. RMS ripple current rating is the critical parameter. Actual RMS current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)/V_{IN}^{2}}$$

The term inside the radical has a maximum value of 0.5 when input voltage is twice output, and stays near 0.5 for a relatively wide range of input voltages. It is common practice therefore to simply use the worst-case value and assume that RMS ripple current is one half of load current. At maximum output current of 1.5A for the LT1578, the input bypass capacitor should be rated at 0.75A ripple current. Note however, that there are many secondary considerations in choosing the final ripple current rating. These include ambient temperature, average versus peak load current, equipment operating schedule, and required product lifetime. For more details, see Application Notes 19 and 46, and Design Note 95.

Input Capacitor Type

Some caution must be used when selecting the type of capacitor used at the input to regulators. Aluminum electrolytics are lowest cost, but are physically large to achieve adequate ripple current rating, and size constraints (especially height) may preclude their use. Ceramic capacitors are now available in larger values, and their high ripple current and voltage rating make them ideal for input bypassing. Cost is fairly high and footprint may also be somewhat large. Solid tantalum capacitors would be a good choice, except that they have a history of occasional spectacular failures when they are subjected to large current surges during power-up. The capacitors can short and then burn with a brilliant white light and lots of nasty smoke. This phenomenon occurs in only a small percentage of units, but it has led some OEMs to forbid their use in high surge applications. The input bypass capacitors of regulators can see these high surges when a battery or high capacitance source is connected. Several manufacturers have developed a line of solid tantalum capacitors specially tested for surge capability (AVX TPS series for instance, see Table 3), but even these units may fail if the input voltage surge approaches the maximum voltage rating of the capacitor. AVX recommends derating capacitor voltage by 2:1 for high surge applications. The highest voltage rating is 50V, so 25V may be a practical input voltage upper limit when using solid tantalum capacitors for input bypassing.

Larger capacitors may be necessary when the input voltage is very close to the minimum specified on the data sheet. Small voltage dips during switch on time are not normally a problem, but at very low input voltage they may cause erratic operation because the input voltage drops below the minimum specification. Problems can also occur if the input-to-output voltage differential is near minimum. The amplitude of these dips is normally a function of capacitor ESR and ESL because the capacitive reactance is small compared to these terms. ESR tends to be the dominate term and is inversely related to physical capacitor size within a given capacitor type.

SYNCHRONIZING

The SYNC pin is used to synchronize the internal oscillator to an external signal. The SYNC input must pass from a logic level low, through the maximum synchronization threshold with a duty cycle between 10% and 90%. The input can be driven directly from a logic level output. The synchronizing range is equal to *initial* operating frequency up to 400kHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (250kHz), not the typical operating frequency of 200kHz. Caution should be used when synchronizing above 280kHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

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At power-up, when V_C is being clamped by the FB pin (see Figure 2, Q2), the sync function is disabled. This allows the frequency foldback to operate in the shorted output condition. During normal operation, switching frequency is controlled by the internal oscillator until the FB pin reaches 0.7V, after which the SYNC pin becomes operational. If no synchronization is required, this pin should be connected to ground.

THERMAL CALCULATIONS

Power dissipation in the LT1578 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}(I_{OUT})^2(V_{OUT})}{V_{IN}} + 60\text{ns}(I_{OUT})(V_{IN})(f)$$

Boost current loss:

$$P_{BOOST} = \frac{V_{OUT}^2(I_{OUT}/50)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}\left(0.55 \bullet 10^{-3}\right) + V_{OUT}\left(1.6 \bullet 10^{-3}\right) + \frac{\left(V_{OUT}^2\right)(0.004)}{V_{IN}}$$

R_{SW} = Switch resistance ($\approx 0.2\Omega$)
60ns = Equivalent switch current/voltage overlap time
f = Switch frequency
Example: with V_{IN} = 10V, V_{OUT} = 5V and I_{OUT} = 1A:

$$P_{SW} = \frac{(0.2)(1)^2(5)}{10} + \left(60 \bullet 10^{-9}\right)(1)(10)\left(200 \bullet 10^3\right)$$
$$= 0.1 + 0.12 = 0.22W$$

$$P_{BOOST} = \frac{(5)^2(1/50)}{10} = 0.05W$$

$$P_Q = 10\left(0.55 \bullet 10^{-3}\right) + 5\left(1.6 \bullet 10^{-3}\right) + \frac{(5)^2(0.004)}{10}$$
$$= 0.02W$$

Total power dissipation is 0.22 + 0.05 + 0.02 = 0.29W.

Thermal resistance for LT1578 package is influenced by the presence of internal or backside planes. With a full plane under the SO package, thermal resistance will be about 80°C/W. No plane will increase resistance to about 120°C/W. To calculate die temperature, add in worst-case ambient temperature:

$T_J = T_A + \theta_{JA}\ (P_{TOT})$

With the SO-8 package (θ_{JA} = 80°C/W), at an ambient temperature of 50°C,

$T_J = 50 + 80\ (0.29) = 73.2°C$

Die temperature is highest at low input voltage, so use lowest continuous input operating voltage for thermal calculations.

FREQUENCY COMPENSATION

Loop frequency compensation of switching regulators can be a rather complicated problem because the reactive components used to achieve high efficiency also introduce multiple poles into the feedback loop. The inductor and output capacitor on a conventional step-down converter actually form a resonant tank circuit that can exhibit peaking and a rapid 180° phase shift at the resonant frequency. By contrast, the LT1578 uses a "current mode" architecture to help alleviate the phase shift created by the inductor. The basic connections are shown in Figure 9. Figure 10 shows a Bode plot of the phase and gain of the power section of the LT1578, measured from the V_C pin to

APPLICATIONS INFORMATION

the output. Gain is set by the 1.5A/V transconductance of the LT1578 power section and the effective complex impedance from output to ground. Gain rolls off smoothly above the 160Hz pole frequency set by the 100µF output capacitor. Phase drop is limited to about 85°. Phase recovers and gain levels off at the zero frequency (≈16kHz) set by capacitor ESR (0.1Ω).

Error amplifier transconductance phase and gain are shown in Figure 11. The error amplifier can be modeled as a transconductance of 1000µMho, with an output impedance of 570kΩ in parallel with 2.4pF. In all practical applications, the compensation network from the V_C pin to ground has a much lower impedance than the output impedance of the amplifier at frequencies above 200Hz. This means that the error amplifier characteristics themselves do not contribute excess phase shift to the loop, and the phase/gain characteristics of the error amplifier section are completely controlled by the external compensation network.

In Figure 12, full loop phase/gain characteristics are shown with a compensation capacitor of 100pF, giving the error amplifier a pole at 2.8kHz, with phase rolling off to 90° and staying there. The overall loop has a gain of 66dB at low frequency, rolling off to unity-gain at 58kHz. The phase plot shows a two-pole characteristic until the ESR of the output capacitor brings it back to single pole above 16kHz. Phase margin is about 77° at unity-gain.

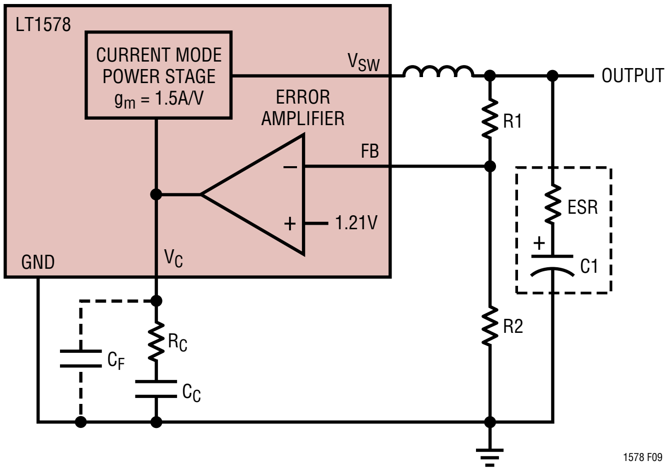

Figure 9. Model for Loop Response

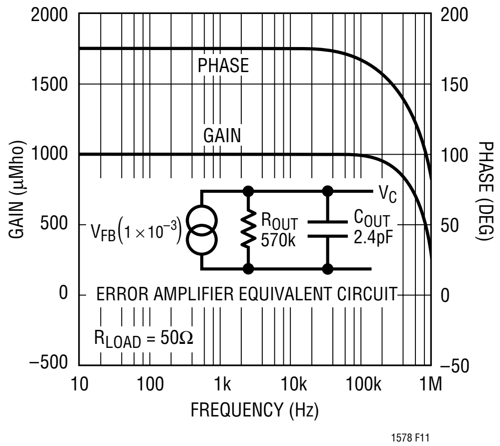

Figure 11. Error Amplifier Gain and Phase

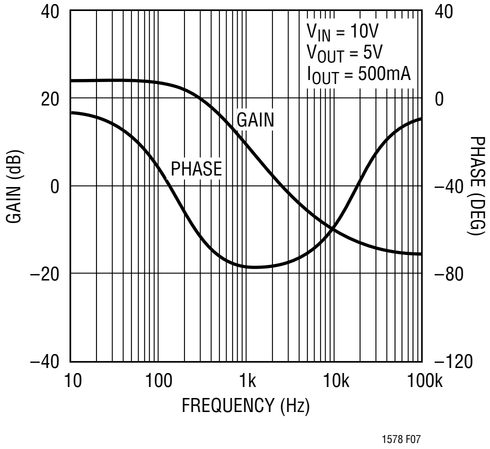

Figure 10. Response from V_C Pin to Output

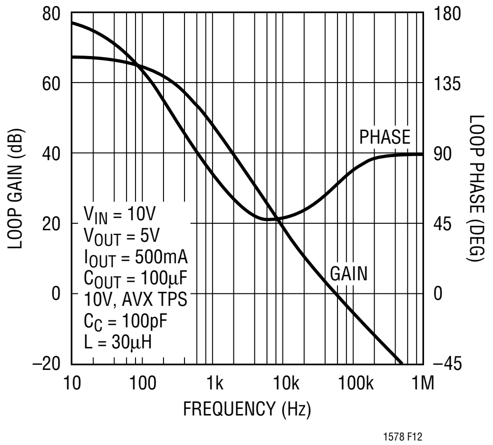

Figure 12. Overall Loop Characteristics

APPLICATIONS INFORMATION

Analog experts will note that around 7kHz, phase dips close to the zero phase margin line. This is typical of switching regulators, especially those that operate over a wide range of loads. This region of low phase is not a problem as long as it does not occur near unity-gain. In practice, the variability of output capacitor ESR tends to dominate all other effects with respect to loop response. Variations in ESR *will* cause unity-gain to move around, but at the same time phase moves with it so that adequate phase margin is maintained over a very wide range of ESR (≥ ±3:1).

What About a Resistor in the Compensation Network?

It is common practice in switching regulator design to add a "zero" to the error amplifier compensation to increase loop phase margin. This zero is created in the external network in the form of a resistor (R_C) in series with the compensation capacitor. Increasing the size of this resistor generally creates better and better loop stability, but there are two limitations on its value. First, the combination of output capacitor ESR and a large value for R_C may cause loop gain to stop rolling off altogether, creating a gain margin problem. An approximate formula for R_C where gain margin falls to zero is:

$$R_C(\text{Loop Gain} = 1) = \frac{V_{OUT}}{(G_{MP})(G_{MA})(ESR)(1.21)}$$

G_{MP} = Transconductance of power stage = 1.5A/V
G_{MA} = Error amplifier transconductance = $1(10^{-3})$
ESR = Output capacitor ESR
1.21 = Reference voltage

With V_{OUT} = 5V and ESR = 0.1Ω, a value of 27.5k for R_C would yield zero gain margin, so this represents an upper limit. There is a second limitation however which has nothing to do with theoretical small signal dynamics. This resistor sets high frequency gain of the error amplifier, including the gain at the switching frequency. If the switching frequency gain is high enough, an excessive amout of output ripple voltage will appear at the V_C pin resulting in improper operation of the regulator. In a marginal case, *subharmonic* switching occurs, as evidenced by alternating pulse widths seen at the switch node. In more severe cases, the regulator squeals or hisses audibly even though the output voltage is still roughly correct. None of this will show on a Bode plot since this is an amplitude insensitive measurement. *Tests have shown that if ripple voltage on the V_C is held to less than 100mV_{P-P}, the LT1578 will generally be well behaved*. The formula below will give an estimate of V_C ripple voltage when R_C is added to the loop, assuming that R_C is large compared to the reactance of C_C at 200kHz.

$$V_{C(RIPPLE)} = \frac{(R_C)(G_{MA})(V_{IN} - V_{OUT})(ESR)(1.21)}{(V_{IN})(L)(f)}$$

G_{MA} = Error amplifier transconductance (1000μMho)

If a series compensation resistor of 15k gave the best overall loop response, with adequate gain margin, the resulting V_C pin ripple voltage with V_{IN} = 10V, V_{OUT} = 5V, ESR = 0.1Ω, L = 30μH, would be:

$$V_{C(RIPPLE)} = \frac{(15k)(1 \bullet 10^{-3})(10 - 5)(0.1)(1.21)}{(10)(30 \bullet 10^{-6})(200 \bullet 10^{3})} = 0.151V$$

This ripple voltage is high enough to possibly create subharmonic switching. In most situations a compromise value (<10k in this case) for the resistor gives acceptable phase margin and no subharmonic problems. In other cases, the resistor may have to be larger to get acceptable phase response, and some means must be used to control ripple voltage at the V_C pin. The suggested way to do this is to add a capacitor (C_F) in parallel with the R_C/C_C network on the V_C pin. The pole frequency for this capacitor is typically set at one-fifth of the switching frequency so that it provides significant attenuation of the switching ripple, but does not add unacceptable phase shift at the loop unity-gain frequency. With R_C = 15k,

$$C_F = \frac{5}{(2\pi)(f)(R_C)} = \frac{5}{2\pi(200 \bullet 10^{3})(15k)} = 265pF$$

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How Do I Test Loop Stability?

The "standard" compensation for LT1578 is a 100pF capacitor for C_C, with $R_C = 0$. While this compensation will work for most applications, the "optimum" value for loop compensation components depends, to various extents, on parameters which are not well controlled. These include *inductor value* (±30% due to production tolerance, load current and ripple current variations), *output capacitance* (±20% to ±50% due to production tolerance, temperature, aging and changes at the load), *output capacitor ESR* (±200% due to production tolerance, temperature and aging), and finally, *DC input voltage and output load current* . This makes it important for the designer to check out the final design to ensure that it is "robust" and tolerant of all these variations.

One way to check switching regulator loop stability is by pulse loading the regulator output while observing the transient response at the output, using the circuit shown in Figure 13. The regulator loop is "hit" with a small transient AC load current at a relatively low frequency, 50Hz to 1kHz. This causes the output to jump a few millivolts, then settle back to the original value, as shown in Figure 14. A well behaved loop will settle back cleanly, whereas a loop with poor phase or gain margin will "ring" as it settles. The *number* of rings indicates the degree of stability, and the *frequency* of the ringing shows the approximate unity-gain frequency of the loop. *Amplitude* of the signal is not particularly important, as long as the amplitude is not so high that the loop behaves nonlinearly.

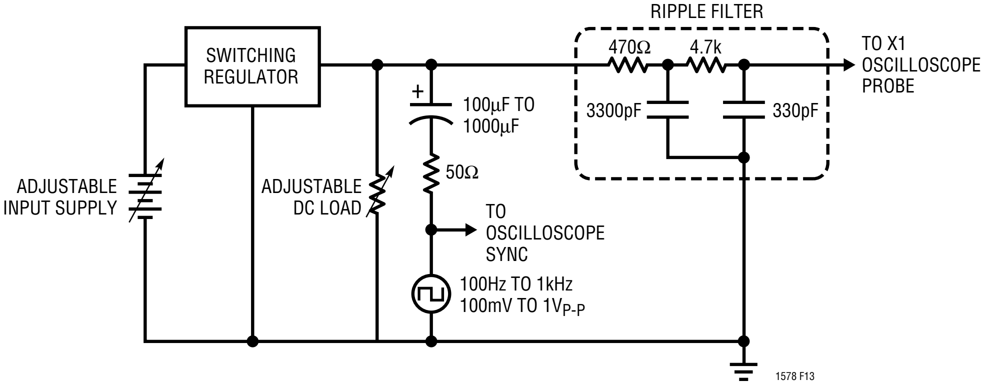

SWITCHING REGULATOR
RIPPLE FILTER
470Ω
4.7k
TO X1 OSCILLOSCOPE PROBE
+
100µF TO 1000µF
3300pF
330pF
50Ω
ADJUSTABLE INPUT SUPPLY
ADJUSTABLE DC LOAD
TO OSCILLOSCOPE SYNC
100Hz TO 1kHz
100mV TO 1V$_{P-P}$
1578 F13

Figure 13. Loop Stability Test Circuit

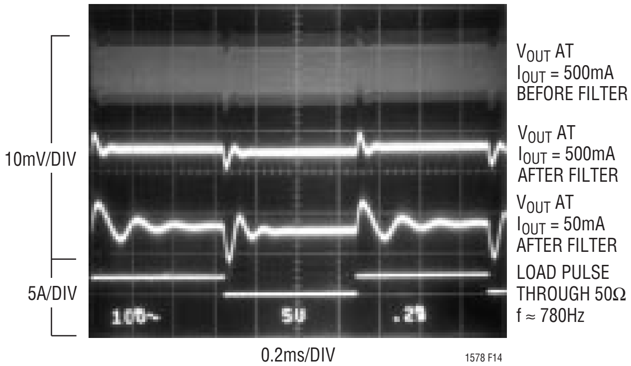


Figure 14. Loop Stability Check

APPLICATIONS INFORMATION

The output of the regulator contains both the desired low frequency transient information and a reasonable amount of high frequency (200kHz) ripple. The ripple makes it difficult to observe the small transient, so a two-pole, 100kHz filter has been added. This filter is not particularly critical; even if it attenuated the transient signal slightly, this wouldn't matter because amplitude is not critical.

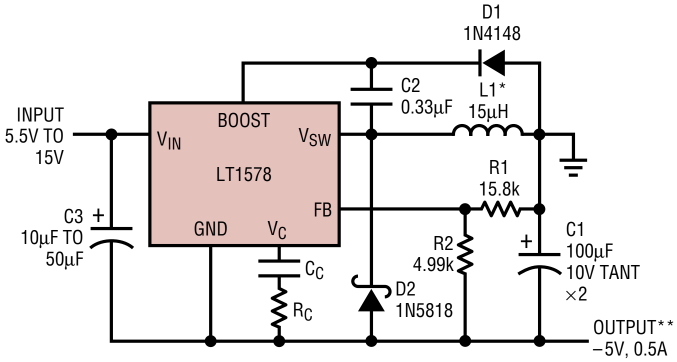
After verifying that the setup is working correctly, start varying load current and input voltage to see if you can find any combination that makes the transient response look suspiciously "ringy." This procedure may lead to an adjustment for best loop stability or faster loop transient response. Nearly always you will find that loop response looks better if you add in several kΩ for R_C. Do this only if necessary, because as explained before, R_C above 1k may require the addition of C_F to control V_C pin ripple. If everything looks OK, use a heat gun and cold spray on the circuit (especially the output capacitor) to bring out any temperature-dependent characteristics.

Keep in mind that this procedure does not take initial component tolerance into account. You should see fairly clean response under all load and line conditions to ensure that component variations will not cause problems. One note here: according to Murphy, the component most likely to be changed in production is the output capacitor, because that is the component most likely to have manufacturer variations (in ESR) large enough to cause problems. It would be a wise move to lock down the sources of the output capacitor in production. Also, try varying component values by a factor of 2 and see if the behavior is still acceptable. Double and halve the values of R_C and C_C and output capacitors. If the regulator still works correctly, it will likely be good in production.

A possible exception to the "clean response" rule is at very light loads, as evidenced in Figure 14 with I_{LOAD} = 50mA. Switching regulators tend to have dramatic shifts in loop response at very light loads, mostly because the inductor current becomes discontinuous. One common result is very slow but stable characteristics. A second possibility is low phase margin, as evidenced by ringing at the output with transients. The good news is that the low phase margin at light loads is not particularly sensitive to component variation, so if it looks reasonable under a transient test, it will probably not be a problem in production. Note that *frequency* of the light load ringing may vary with component tolerance but phase margin generally hangs in there.

POSITIVE-TO-NEGATIVE CONVERTER

The circuit in Figure 15 is a classic positive-to-negative topology using a grounded inductor. It differs from the standard approach in the way the IC chip derives its feedback signal. Because the LT1578 accepts only positive feedback signals, the ground pin must be tied to the regulated negative output. A resistor divider to ground or, in this case, the sense pin, then provides the proper feedback voltage for the chip.



* INCREASE L1 TO 30µH OR 60µH FOR HIGHER CURRENT APPLICATIONS. SEE APPLICATIONS INFORMATION

** MAXIMUM LOAD CURRENT DEPENDS ON MINIMUM INPUT VOLTAGE AND INDUCTOR SIZE. SEE APPLICATIONS INFORMATION

1578 F15

Figure 15. Positive-to-Negative Converter

Inverting regulators differ from buck regulators in the basic switching network. Current is delivered to the output as *square waves with a peak-to-peak amplitude much greater than load current*. This means that *maximum load current will be significantly less than the LT1578's 1.5A maximum switch current, even with large inductor values*. The buck converter in comparison, delivers current to the output as a triangular wave superimposed on a DC level equal to load current, and load current can approach 1.5A with large inductors. Output ripple voltage for the positive-to-negative converter will be much higher than a buck converter. Ripple current in the output capacitor will also be much higher. The following equations can be used to calculate operating conditions for the positive-to-negative converter.

Maximum load current:

$$I_{MAX} = \frac{\left[I_P - \dfrac{(V_{IN})(V_{OUT})}{2(V_{OUT}+V_{IN})(f)(L)}\right](V_{OUT})(V_{IN}-0.35)}{(V_{OUT}+V_{IN}-0.35)(V_{OUT}+V_F)}$$

I_P = Maximum rated switch current
V_{IN} = Minimum input voltage
V_{OUT} = Output voltage
V_F = Catch diode forward voltage
0.35 = Switch voltage drop at 1.5A

Example: with $V_{IN(MIN)} = 5.5V$, $V_{OUT} = 5V$, $L = 30\mu H$, $V_F = 0.5V$, $I_P = 1.5A$: $I_{MAX} = 0.6A$. Note that this equation does not take into account that maximum rated switch current (I_P) on the LT1578 is reduced slightly for duty cycles above 50%. If duty cycle is expected to exceed 50% (input voltage less than output voltage), use the actual I_P value from the Electrical Characteristics table.

Operating duty cycle:

$$DC = \frac{V_{OUT}+V_F}{V_{IN}-0.3+V_{OUT}+V_F}$$

(This formula uses an average value for switch loss, so it may be several percent in error.)

With the conditions above:

$$DC = \frac{5+0.5}{5.5-0.3+5+0.5} = 51\%$$

This duty cycle is close enough to 50% that I_P can be assumed to be 1.5A.

OUTPUT DIVIDER

If the adjustable part is used, the resistor connected to V_{OUT} (R2) should be set to approximately 5k. R1 is calculated from:

$$R1 = \frac{R2(V_{OUT}-1.21)}{1.21}$$

INDUCTOR VALUE

Unlike buck converters, positive-to-negative converters cannot use large inductor values to reduce output ripple voltage. At 200kHz, values larger than 75µH make almost no change in output ripple. The graph in Figure 16 shows peak-to-peak output ripple voltage for a 5V to –5V converter versus inductor value. The criteria for choosing the

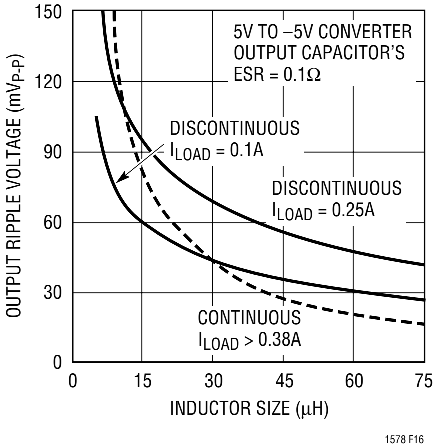


Figure 16. Ripple Voltage on Positive-to-Negative Converter

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inductor is therefore typically based on ensuring that peak switch current rating is not exceeded. This gives the lowest value of inductance that can be used, but in some cases (lower output load currents) it may give a value that creates unnecessarily high output ripple voltage. A compromise value is often chosen that reduces output ripple. As you can see from the graph, *large* inductors will not give arbitrarily low ripple, but *small* inductors can give high ripple.

The difficulty in calculating the minimum inductor size needed is that you must first know whether the switcher will be in continuous or discontinuous mode at the critical point where switch current is 1.5A. The first step is to use the following formula to calculate the load current where the switcher must use continuous mode. If your load current is less than this, use the discontinuous mode formula to calculate the minimum inductor value needed. If the load current is higher, use the continuous mode formula.

Output current where continuous mode is needed:

$$I_{CONT} = \sqrt{\frac{(V_{IN})^2(I_P)^2}{4(V_{IN}+V_{OUT})(V_{IN}+V_{OUT}+V_F)}}$$

Minimum inductor discontinuous mode:

$$L_{MIN} = \frac{2(V_{OUT})(I_{OUT})}{(f)(I_P)^2}$$

Minimum inductor continuous mode:

$$L_{MIN} = \frac{(V_{IN})(V_{OUT})}{2(f)(V_{IN}+V_{OUT})\left[I_P - I_{OUT}\left(1+\frac{(V_{OUT}+V_F)}{V_{IN}}\right)\right]}$$

For the example above, with maximum load current of 0.25A:

$$I_{CONT} = \sqrt{\frac{(5.5)^2(1.5)^2}{4(5.5+5)(5.5+5+0.5)}} = 0.38A$$

This says that discontinuous mode can be used and the minimum inductor needed is found from:

$$L_{MIN} = \frac{2(5)(0.25)}{\left(200 \bullet 10^3\right)(1.5)^2} = 5.6\mu H$$

In practice, the inductor should be increased by about 30% over the calculated minimum to handle losses and variations in value. This suggests a minimum inductor of 7.3μH for this application, but looking at the ripple voltage chart shows that output ripple voltage could be reduced by a factor of two by using a 30μH inductor. There is no rule of thumb here to make a final decision. If modest ripple is needed and the larger inductor does the trick, this is probably the best solution. If ripple is noncritical use the smaller inductor. If ripple is extremely critical, a second stage filter may have to be added in any case, and the lower value of inductance can be used. Keep in mind that the output capacitor is the other critical factor in determining output ripple voltage. Ripple shown on the graph (Figure 16) is with a capacitor's ESR of 0.1Ω. This is reasonable for AVX type TPS "D" or "E" size surface mount solid tantalum capacitors, but the final capacitor chosen must be looked at carefully for ESR characteristics.

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Ripple Current in the Input and Output Capacitors

Positive-to-negative converters have high ripple current in both the input and output capacitors. For long capacitor lifetime, the RMS value of this current must be less than the high frequency ripple current rating of the capacitor. The following formula will give an *approximate* value for RMS ripple current. *This formula assumes continuous conduction mode and a large inductor value.* Small inductors will give somewhat higher ripple current, especially in discontinuous mode. The exact formulas are very complex and appear in Application Note 44, pages 30 and 31. For our purposes here, a simple fudge factor (ff) is added. The value for ff is about 1.2 for load currents above 0.38A (in continuous conduction mode) and L ≥10µH. It increases to about 2.0 for smaller inductors at lower load currents (in discontinuous conduction mode).

$$\text{Capacitor } I_{RMS} = (ff)(I_{OUT})\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

ff = Fudge factor (1.2 to 2.0)

Diode Current

Average diode current is equal to load current. *Peak* diode current will be considerably higher.

Peak diode current:

$$\text{Continuous Mode} = I_{OUT}\frac{(V_{IN} + V_{OUT})}{V_{IN}} + \frac{(V_{IN})(V_{OUT})}{2(L)(f)(V_{IN} + V_{OUT})}$$

$$\text{Discontinuous Mode} = \sqrt{\frac{2(I_{OUT})(V_{OUT})}{(L)(f)}}$$

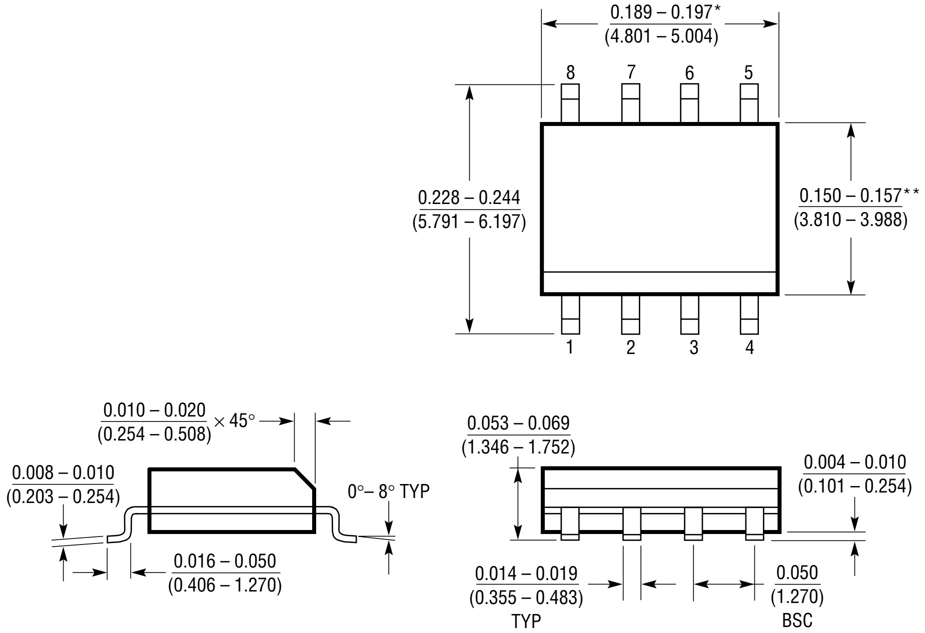
Keep in mind that during start-up and output overloads, the average diode current may be much higher than with normal loads. Care should be used if diodes rated less than 1A are used, especially if continuous overload conditions must be tolerated.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)

(LTC DWG # 05-08-1610)


0.189 – 0.197*
(4.801 – 5.004)
8
7
6
5
0.228 – 0.244
(5.791 – 6.197)
0.150 – 0.157**
(3.810 – 3.988)
1
2
3
4
0.010 – 0.020
(0.254 – 0.508)
× 45°
0.008 – 0.010
(0.203 – 0.254)
0°– 8° TYP
0.016 – 0.050
(0.406 – 1.270)
0.053 – 0.069
(1.346 – 1.752)
0.004 – 0.010
(0.101 – 0.254)
0.014 – 0.019
(0.355 – 0.483)
TYP
0.050
(1.270)
BSC

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

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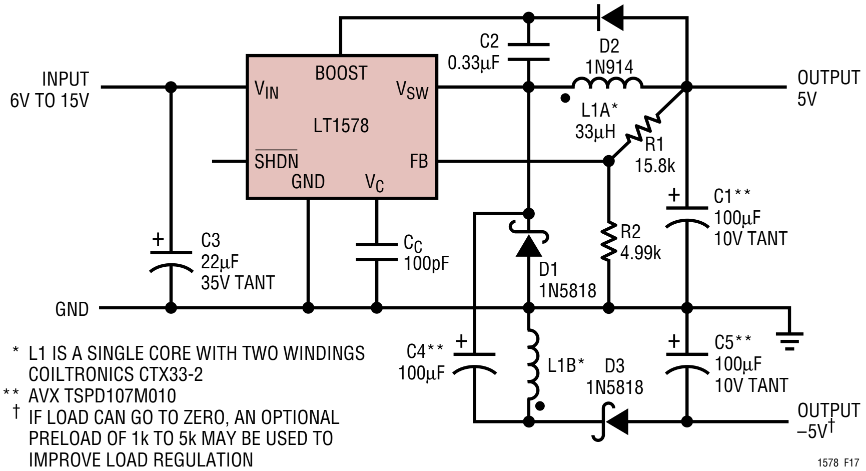
TYPICAL APPLICATION

Dual Output SEPIC Converter

The circuit in Figure 17 generates both positive and negative 5V outputs with a single piece of magnetics. The inductor L1 is a 33µH surface mount inductor from Coiltronics. It is manufactured with two identical windings that can be connected in series or parallel. The topology for the 5V output is a standard buck converter. The –5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates the SEPIC (Single-Ended Primary Inductance Converter) topology which improves regulation and reduces ripple current in L1. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. In a flyback converter, during switch on time, all the converter's energy is stored in L1A only, since no current flows in L1B. At switch off, energy is transferred by magnetic coupling into L1B, powering the –5V rail. C4 pulls L1B positive during switch on time, causing current to flow, and energy to build in L1B and C4. At switch off, the energy stored in both L1B and C4 supply the –5V rail. This reduces the current in L1A and changes L1B current waveform from square to triangular. For details on this circuit see Design Note 100.



* L1 IS A SINGLE CORE WITH TWO WINDINGS COILTRONICS CTX33-2

** AVX TSPD107M010

† IF LOAD CAN GO TO ZERO, AN OPTIONAL PRELOAD OF 1k TO 5k MAY BE USED TO IMPROVE LOAD REGULATION

Figure 17. Dual Output SEPIC Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1074/LT1076	Step-Down Switching Regulators	40V Input, 100kHz, 5A and 2A
LTC1174	High Efficiency Step-Down and Inverting DC/DC Converter	0.5A, 150kHz Burst Mode™ Operation
LT1370	High Efficiency DC/DC Converter	42V, 6A, 500kHz Switch
LT1371	High Efficiency DC/DC Converter	35V, 3A, 500kHz Switch
LT1372/LT1377	500kHz and 1MHz High Efficiency 1.5A Switching Regulators	Boost Topology
LT1376	High Efficiency Step-Down Switching Regulator	25V, 1.5A, 500kHz Switch
LT1507	High Efficiency Step-Down Switching Regulator	15V, 1.5A, 500kHz Switch
LT1676/LT1776	High Efficiency Step-Down Switching Regulators	7.4V to 60V Input, 100kHz/200kHz
LTC1772	SOT-23 Low Voltage Step-Down DC/DC Controller	550kHz, Drives PFET, 6-Lead SOT-23 Package; up to 4.5A Output Current
LTC1735	High Efficiency Step-Down Converter	Synchronous Buck Controller Drives External MOSFETs
LT1777	Low Noise Step-Down Switching Regulator	48V Input, Internally Limited dV/dt, Programmable di/dt

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