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IS34MW02G084/164

IS35MW02G084/164

2Gb SLC-4b ECC

**1.8V X8/X16 NAND FLASH MEMORY STANDARD NAND
INTERFACE**

2Gb(x8/x16) 1.8V NAND FLASH MEMORY with 4b ECC

FEATURES

- **Flexible & Efficient Memory Architecture**
 - Memory Cell: 1bit/Memory Cell
 - Organization: 256Mb x8 /128Mb x16
 - X8:
 - Memory Cell Array: (256M + 8M) x 8bit
 - Data Register: (2K + 64) x 8bit
 - Page Size: (2K + 64) Byte
 - Block Erase: (128K + 4K) Byte
 - X16:
 - Memory Cell Array: (128M + 4M) x 16bit
 - Data Register: (1K + 32) x 16bit
 - Page Size: (1K + 32) Byte
 - Block Erase: (64K + 2K) Byte
- **Highest performance**
 - Read Performance
 - Random Read: 25us (Max.)
 - Serial Access: 45ns (Max.)
 - Write Performance
 - Program time: 300us - typical
 - Block Erase time: 3ms – typical
- **Low Power with Wide Temp. Ranges**
 - Single 1.8V (1.7V to 1.95V) Voltage Supply
 - 15 mA Active Read Current
 - 10 μ A Standby Current
 - Temp Grades:
 - Industrial: -40°C to +85°C
 - Extended: -40°C to +105°C
 - Automotive, A1: -40°C to +85°C
 - Automotive, A2: -40°C to +105°C
- **Reliable CMOS Floating Gate Technology**
 - ECC Requirement: X8 - **4bit/512Byte**
X16 - **4bit/256Word**
 - Endurance: 100K Program/Erase cycles
 - Data Retention: 10 years
- **Efficient Read and Program modes**
 - Command/Address/Data Multiplexed I/O Interface
 - Command Register Operation
 - Automatic Page 0 Read at Power-Up Option
 - Boot from NAND support
 - Automatic Memory Download
 - NOP: 4 cycles
 - Cache Program Operation for High Performance Program
 - Cache Read Operation
 - Copy-Back Operation
 - EDO mode
 - OTP operation
 - Two-Plane Operation
 - Bad-Block-Protect
- **Advanced Security Protection**
 - Hardware Data Protection:
 - Program/Erase Lockout during Power Transitions
- **Industry Standard Pin-out & Packages**
 - T =48-pin TSOP (Type I) ⁽¹⁾
 - B =63-ball VFBGA

Notes:

1. Call Factory for TSOP (Type I) x16

GENERAL DESCRIPTION

The IS34/35MW2G084/164 are 256Mx8/128Mx16 bit with spare 8Mx8/4Mx16 bit capacity. The devices are offered in 1.8V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 2,048 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 2,112-Byte page in typical 300us and an erase operation can be performed in typical 3ms on a 128K-Byte for X8 device block (or 64K-Word for x16 device block).

Data in the page mode can be read out at 45ns cycle time per Word. The I/O pins serve as the ports for address and command inputs as well as data input/output.

The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array.

This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

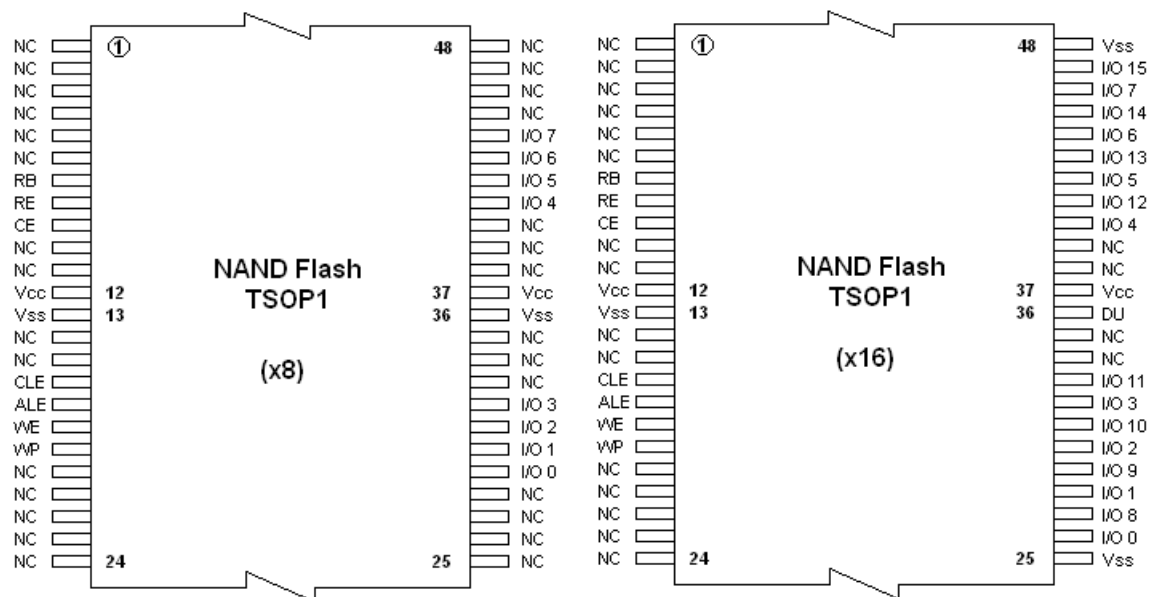
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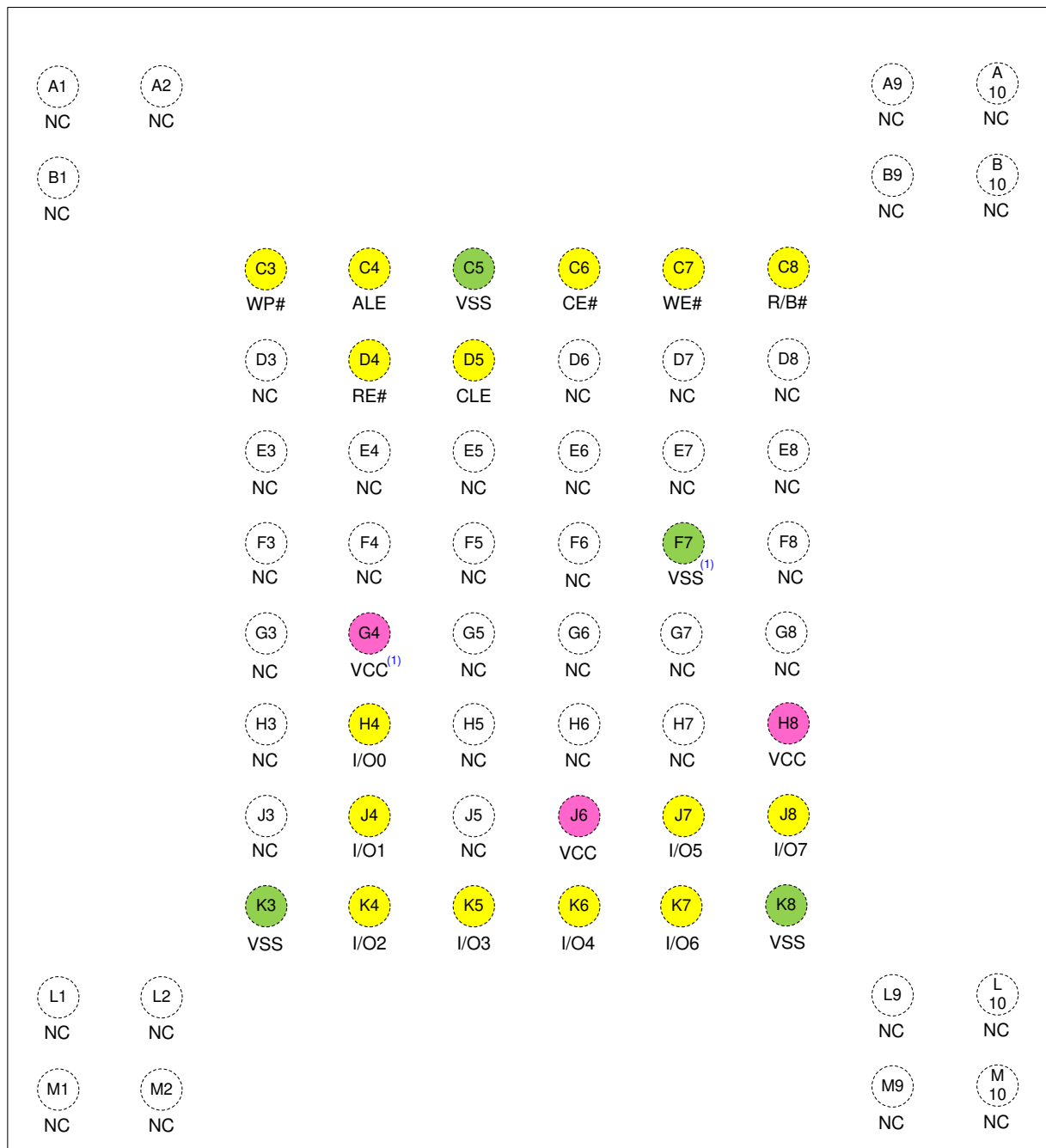
1. PIN CONFIGURATION

48-pin TSOP (Type I)



63-ball VFBGA (x8)

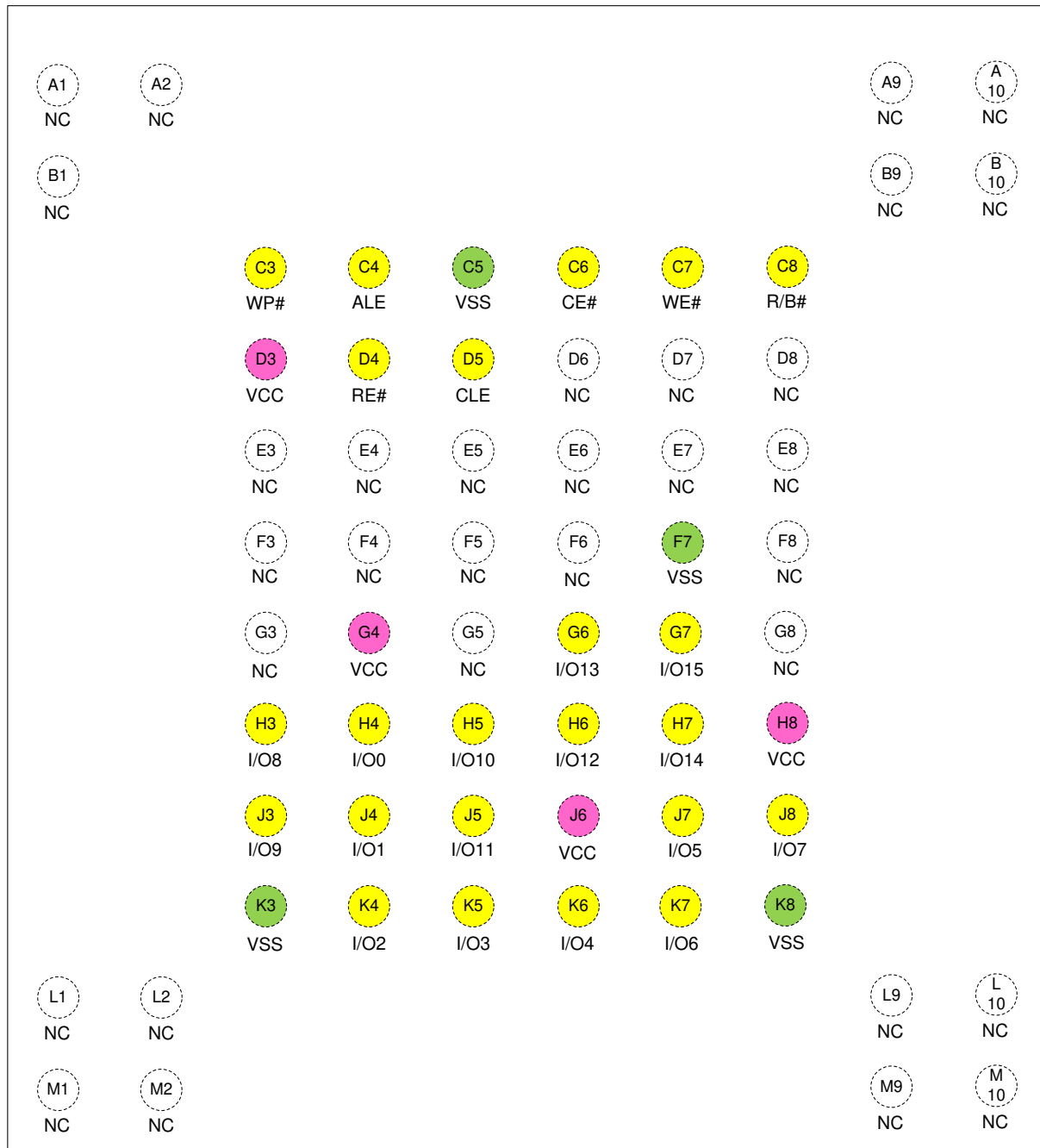
Balls Down, Top View



Note:

- These pins might not be bonded in the package; however it is recommended to connect these pins to the designated external sources for ONFI compatibility.

Balls Down, Top View



2. PIN DESCRIPTIONS

Pin Name	Pin Function
I/O0 ~ I/O7 (X8) I/O0 ~ I/O15 (X16)	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	ADDRESS LATCH ENABLE The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	CHIP ENABLE The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	READ ENABLE The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	WRITE ENABLE The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	WRITE PROTECT The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	READY/BUSY OUTPUT The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	POWER VCC is the power supply for device.
VSS	GROUND
N.C.	NO CONNECTION Lead is not internally connected.

Note: Connect all VCC and VSS pins of each device to common power supply outputs. Do not leave VCC or VSS disconnected.

3. BLOCK DIAGRAM

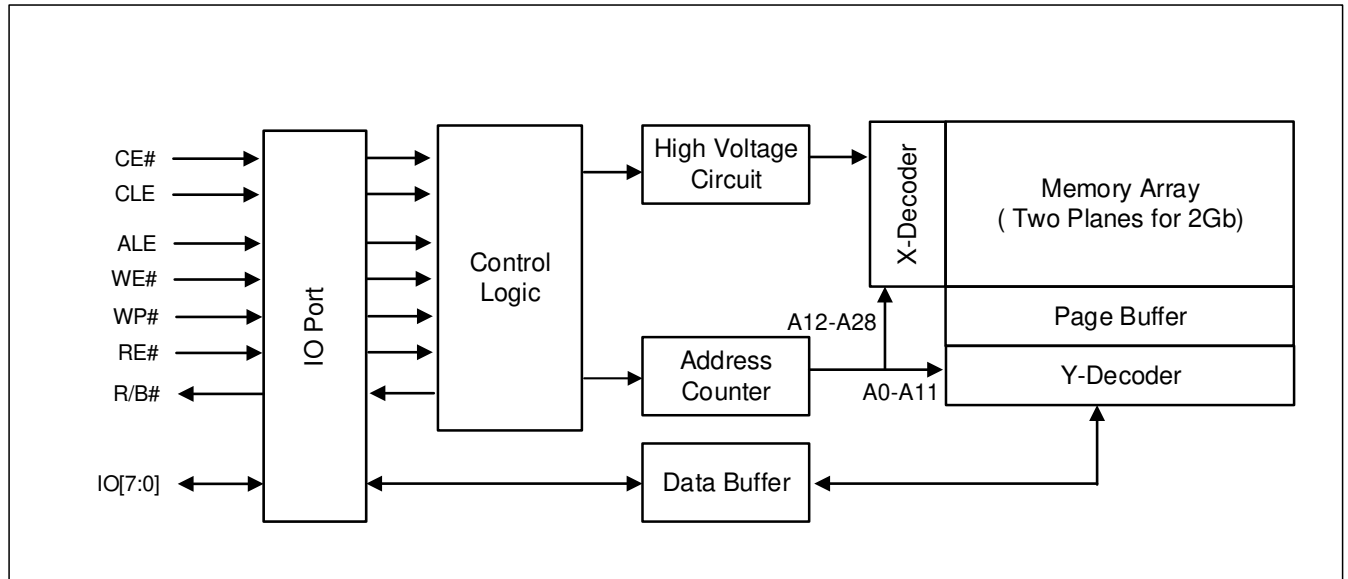


Figure 3.1 Functional Block Diagram(x8)

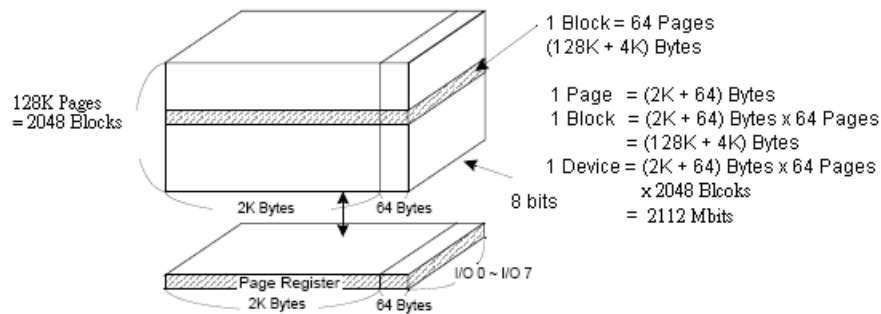


Figure 3.2 Array Organization(x8)

Table 3.1 ARRAY Address (x8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1 st cycle	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	Column Address
2 nd cycle	A ₈	A ₉	A ₁₀	A ₁₁	*L	*L	*L	*L	Column Address
3 rd cycle	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	A ₁₇	A ₁₈	A ₁₉	Row Address
4 th cycle	A ₂₀	A ₂₁	A ₂₂	A ₂₃	A ₂₄	A ₂₅	A ₂₆	A ₂₇	Row Address
5 th cycle	A ₂₈	*L	*L	*L	*L	*L	*L	*L	Row Address

Notes:

1. Column Address: Starting Address of the Register.
2. *L must be set to "Low".
3. The device ignores any additional input of address cycles than required.
4. A₁₈ is for Plane Address setting.

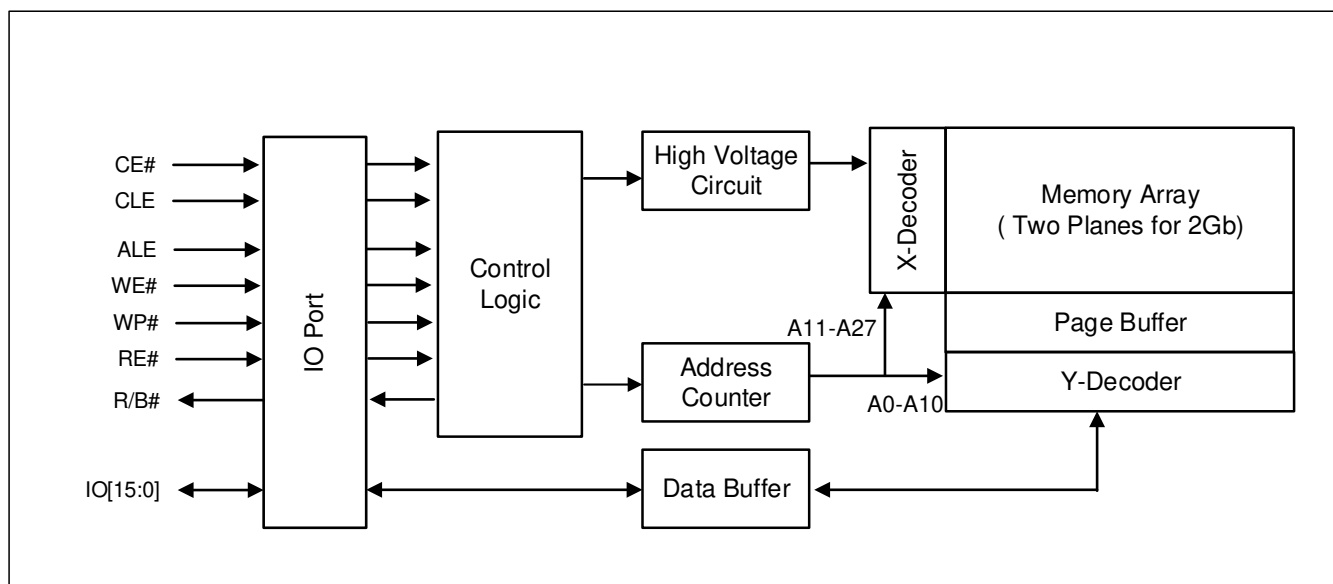


Figure 3.3 Functional Block Diagram(x16)

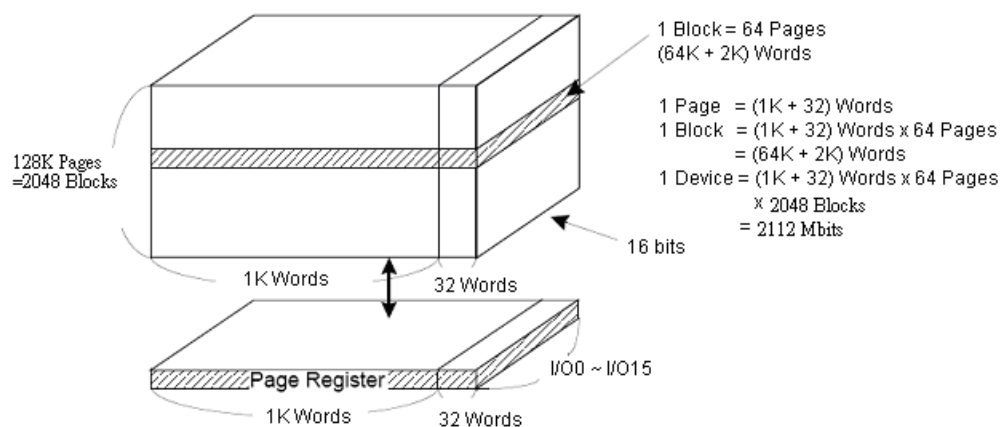


Figure 3.4 Array Organization(x8)

Table 3.2 ARRAY Address (x16)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1 st cycle	A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	Column Address
2 nd cycle	A ₈	A ₉	A ₁₀	*L	*L	*L	*L	*L	Column Address
3 rd cycle	A ₁₁	A ₁₂	A ₁₃	A ₁₄	A ₁₅	A ₁₆	A ₁₇	A ₁₈	Row Address
4 th cycle	A ₁₉	A ₂₀	A ₂₁	A ₂₂	A ₂₃	A ₂₄	A ₂₅	A ₂₆	Row Address
5 th cycle	A ₂₇	*L	*L	*L	*L	*L	*L	*L	Row Address

Notes:

1. Column Address: Starting Address of the Register.
2. *L must be set to "Low".
3. The device ignores any additional input of address cycles than required.
4. A₁₇ is for Plane Address setting.

4. OPERATION DESCRIPTION

The IS34/35MW02G084/164 are 2Gbit memory organized as 128K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2,048 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the device.

The device has addresses multiplexed into 8 or 16 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Table 4.1 Command Set

Function	1 st Cycle	2 nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input ⁽¹⁾	85h	-	
Random Data Output ⁽¹⁾	05h	E0h	
Read Status	70h	-	O
Read Status 2	F1h	-	O
Two-Plane Read ⁽³⁾	60h-60h	30h	
Two-Plane Read for Copy-Back	60h-60h	35h	
Two-Plane Random Data Output ^{(1) (3)}	00h-05h	E0h	
Two-Plane Page Program ⁽²⁾	80h-11h	81h-10h	
Two-Plane Copy-Back Program ⁽²⁾	85h-11h	81h-10h	
Two-Plane Block Erase	60h-60h	D0h	
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start For Last Page Cache Read	3Fh	-	
Two-Plane Cache Read ⁽³⁾	60h-60h	33h	
Two-Plane Cache Program ⁽²⁾	80h-11h	81h-15h	

Notes:

1. Random Data Input/Output can be executed in a page.
2. Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h and FFh.
3. Two-Plane Random Data Output must be used after Two-Plane Read operation or Two-Plane Cache Read operation.

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.6V to +4.6V
All I/O Voltage with Respect to Ground		-0.6V to $V_{CC} + 0.3V$ (< 4.6V)
V_{CC}		-0.6V to +4.6V
Short Circuit Current		5mA
Electrostatic Discharge Voltage (Human Body Model) ⁽²⁾		-2000V to +2000V

Notes:

1. Applied conditions greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. ANSI/ESDA/JEDEC JS-001

5.2 RECOMMENDED OPERATING CONDITIONS

Part Number	IS34/35MW02G084/164
Operating Temperature (Industrial Grade)	-40°C to 85°C
Operating Temperature (Extended Grade)	-40°C to 105°C
Operating Temperature (Automotive Grade A1)	-40°C to 85°C
Operating Temperature (Automotive Grade A2)	-40°C to 105°C
V_{CC} Power Supply	1.7V (VMIN) – 1.95V (VMAX); 1.8V (Typ)

5.3 DC CHARACTERISTICS

(Under operating range)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	$t_{RC}=t_{RCMin}$, $CE\#=V_{IL}$, $I_{OUT}=0mA$	-	15	30	mA
	Program	ICC2	-	-	15		
	Erase	ICC3	-	-	15		
Stand-by Current (TTL)		ISB1	$CE\#=V_{IH}$, $WP\#=0V/VCC$	-	-	1	uA
Stand-by Current (CMOS)		ISB2	$CE\#=VCC-0.2$, $WP\#=0V/VCC$	-	10	50	
Input Leakage Current		ILI	$V_{IN}=0$ to V_{cc} (max)	-	-	+/-10	
Output Leakage Current		ILO	$V_{OUT}=0$ to V_{cc} (max)	-	-	+/-10	
Input High Voltage		$V_{IH}^{(1)}$		$0.8 \times VCC$	-	$V_{cc}+0.3$	V
Input Low Voltage, All inputs		$V_{IL}^{(1)}$		-0.3	-	$0.2 \times VCC$	
Output High Voltage Level		VOH	$I_{OH}=-100\text{ uA}$	$VCC-0.1$	-	-	
Output Low Voltage Level		VOL	$I_{OL}=+100\text{ uA}$	-	-	0.1	
Output Low Current (R/B#)		I_{OL} (R/B#)	$VOL=0.2V$	3	4	-	mA

Notes:

- VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
- Typical value are measured at Vcc=1.8V, TA=25°C. Not 100% tested.

5.4 VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
IS34/35MW02G084/164	NVB	2,008	-	2,048	Block

Notes:

- The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
- The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 4bit/512Byte ECC.

5.5 AC MEASUREMENT CONDITION

Symbol	Parameter	Min	Max	Units
CL	Output Load	1 TTL GATE and CL = 50pF		pF
TR,TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0V to V _{CC}		V
VREFI	Input Timing Reference Voltages	0.5V _{CC}		V
VREFO	Output Timing Reference Voltages	0.5V _{CC}		V

Note:

1. Refer to 8.16 Ready/Busy#, R/B#'s Busy to Ready time is decided by pull up register (Rp) tied to R/B# pin.

5.6 AC PIN CAPACITANCE (TA = 25°C, VCC=1.8V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	-	-	10	pF
C _{I/O}	Input /Output Capacitance	V _{I/O} = 0V	-	-	10	pF

Note:

1. These parameters are characterized and not 100% tested.

5.7 MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input (5 clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input (5 clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X ⁽¹⁾	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V _{CC} ⁽²⁾	Stand-by	

Notes :

1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

5.8 ROGRAM/ERASE PERFORMANCNE

(Industrial: $T_A = -40$ to 85°C , Automotive, A1: $T_A = -40$ to 85°C , $V_{CC} = 1.7\text{V} \sim 1.95\text{V}$)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	300	750	us
Dummy Busy Time for Cache Operation	tCBSY	-	3	700	us
Number of Partial Program Cycles in the Same Page	Nop	-	-	4	cycle
Block Erase Time	tBERS	-	3	10	ms
Dummy Busy Time for Two-Plane Page Program	tDBSY	-	0.5	1	us

Notes:

1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V V_{CC} and 25°C temperature.
2. **tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.**
3. tCBSY max.time depends on timing between internal program completion and data-in.

5.9 AC CHARACTERISTICS FOR ADDRESS/ COMMAND/DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS ⁽¹⁾	25	-	ns
CLE Hold Time	tCLH	10	-	ns
CE# Setup Time	tCS ⁽¹⁾	35	-	ns
CE# Hold Time	tCH	10	-	ns
WE# Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS ⁽¹⁾	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS ⁽¹⁾	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	45	-	ns
WE# High Hold Time	tWH	15	-	ns
Address to Data Loading Time	tADL ⁽²⁾	100 ⁽²⁾	-	ns

Note:

1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. tADL is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

5.10 AC CHARACTERISTICS FOR OPERATION

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	25	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
RE# Pulse Width		tRP	25	-	ns
WE# High to Busy		tWB	-	100	ns
WP# Low to WE# Low (disable mode)		tWW	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		tRC	45	-	ns
RE# Access Time		tREA	-	30	ns
CE# Access Time		tCEA	-	45	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
CE# High to ALE or CLE Don't care		tCSD	0		ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5		ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	15	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Device Resetting Time during...	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5 ⁽¹⁾	us
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR	-	30	us

Note: If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

6. TIMING DIAGRAMS

6.1 COMMAND LATCH CYCLE

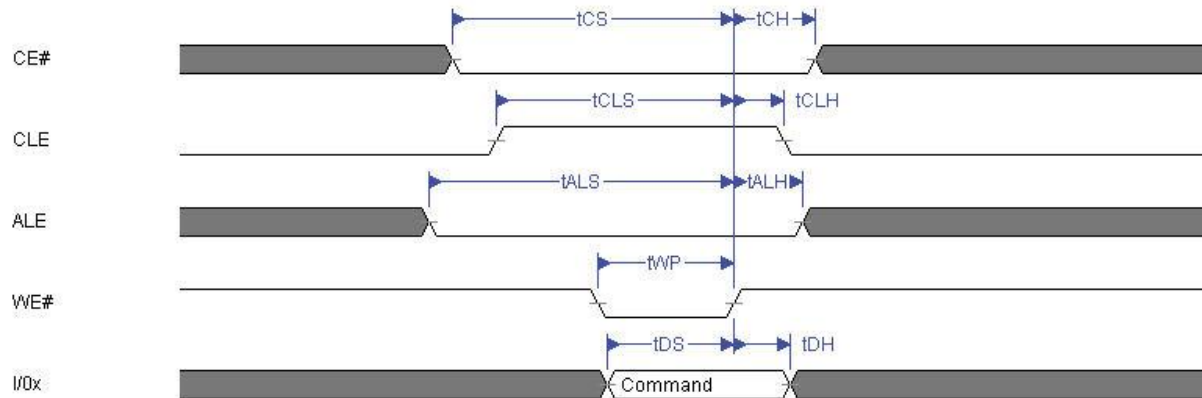


Figure 6.1 Command Latch Cycle

6.2 ADDRESS LATCH CYCLE

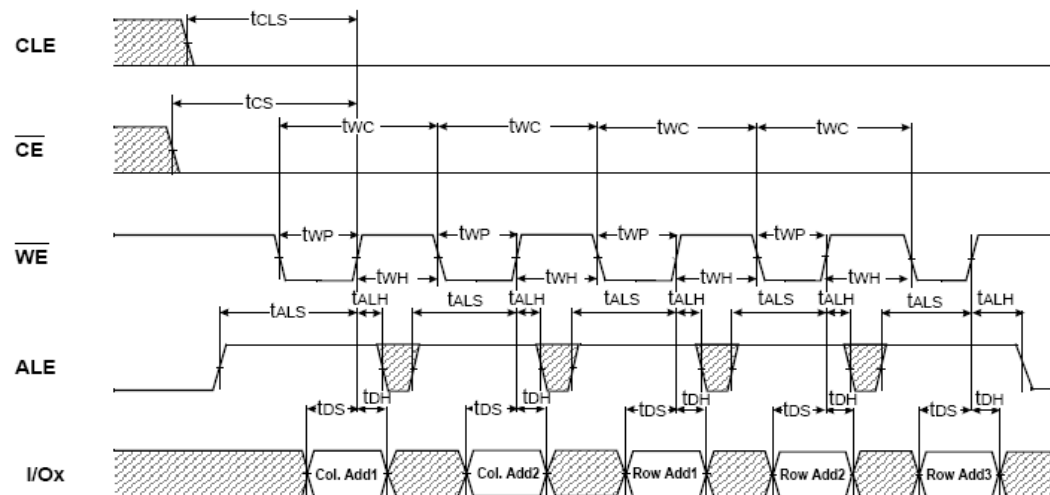


Figure 6.2 Address Latch Cycle

6.3 INPUT DATA LATCH CYCLE

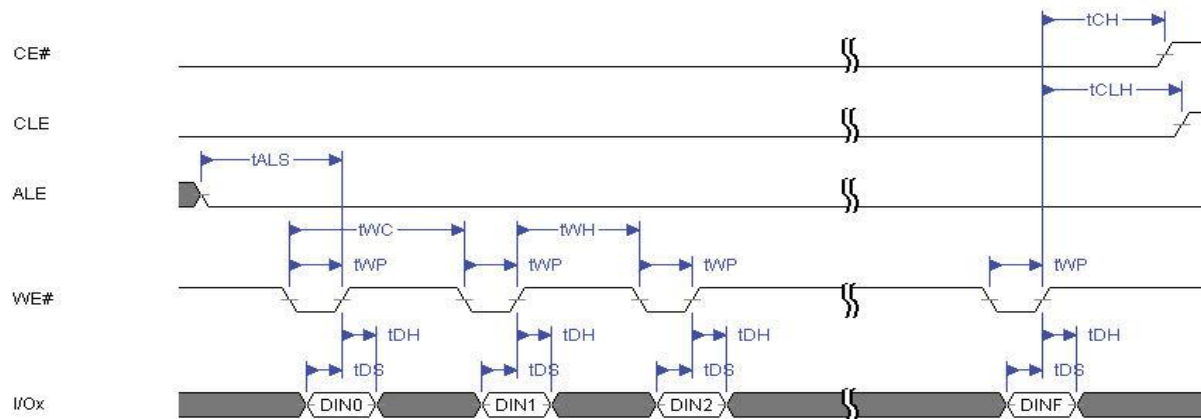
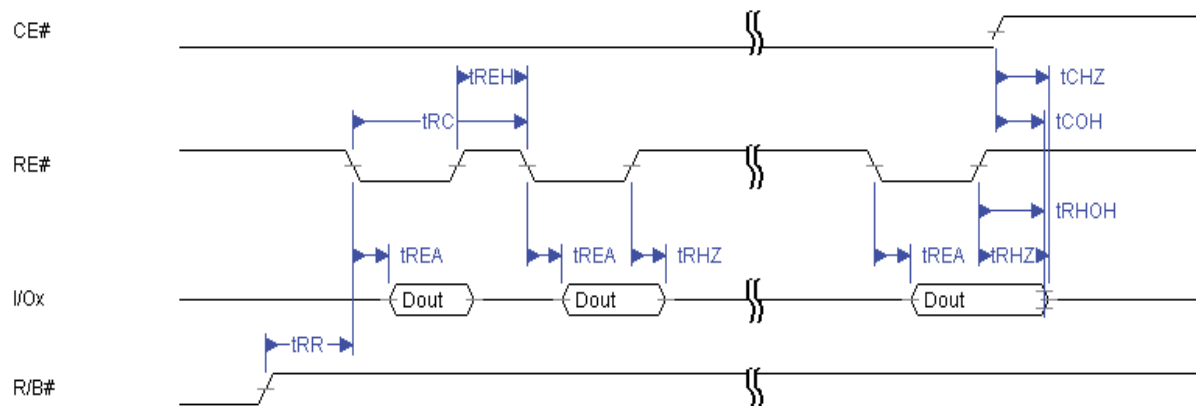


Figure 6.3 Input Data Latch Cycle

6.4 SERIAL ACCESS CYCLE AFTER READ (CLE=L, WE#=H, ALE=L)

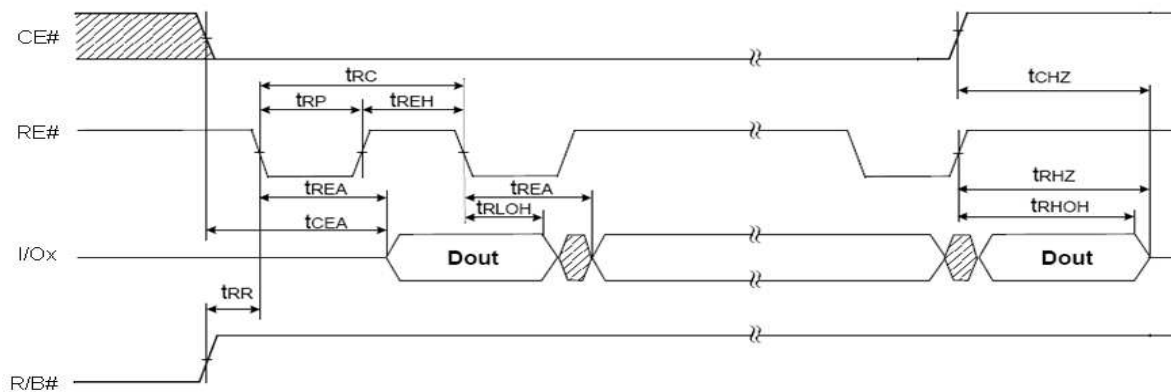


Note:

1. Dout transition is measured at $\pm 200\text{mV}$ from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure 6.4 Serial Access Cycle after Read

6.5 SERIAL ACCESS CYCLE AFTER READ (EDO TYPE CLE=L, WE#=H, ALE=L)



Note:

1. Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sample and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33MHZ.
tRHOH starts to be valid

Figure 6.5 Serial Access Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)

6.6 STATUS READ CYCLE

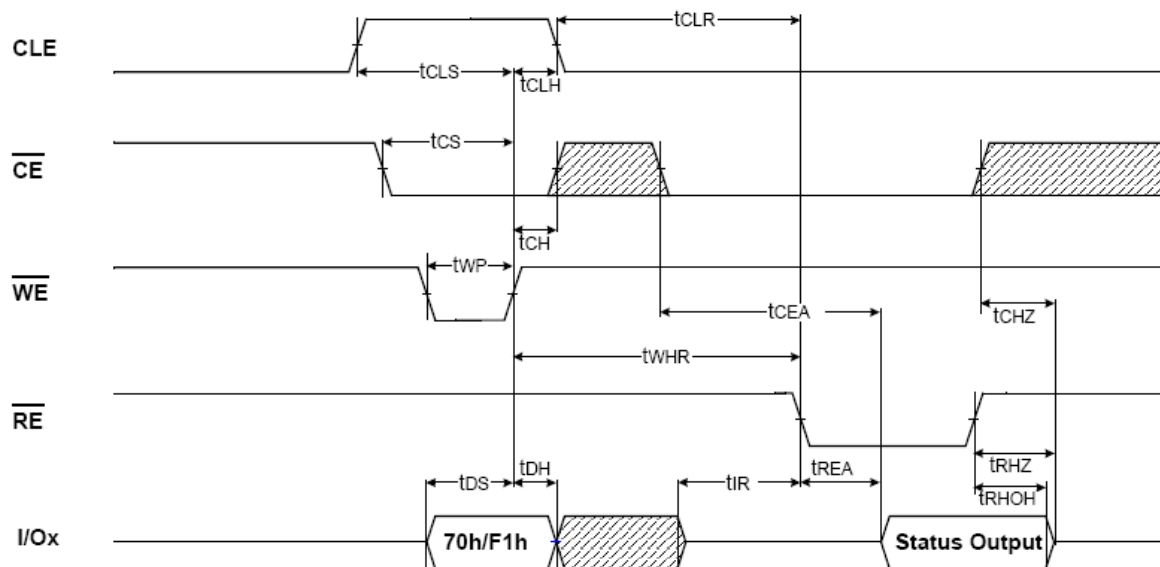


Figure 6.6 Status Read Cycle

6.7 READ OPERATION (ONE PAGE)

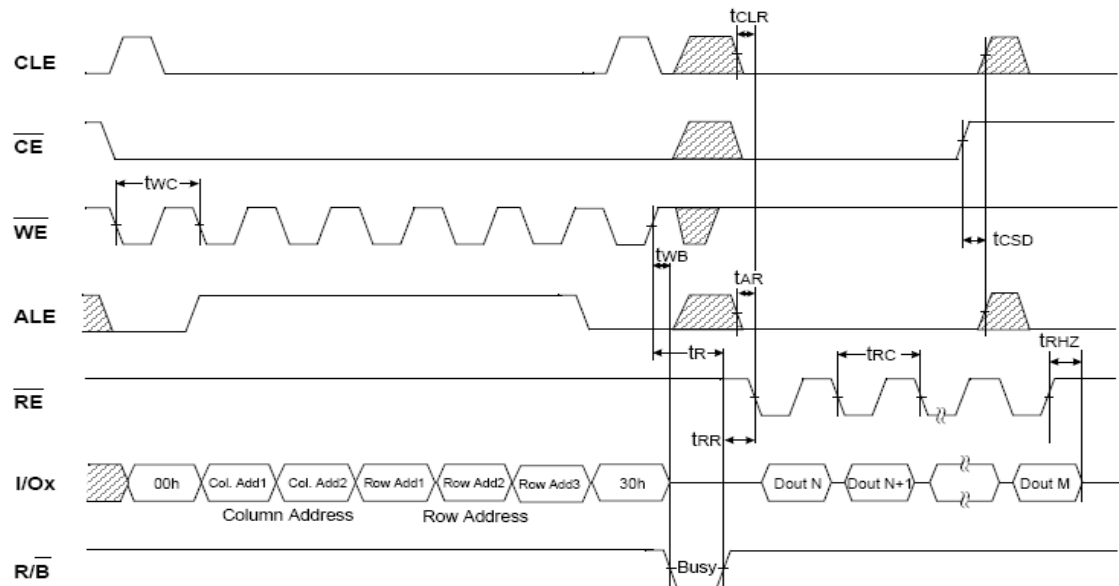


Figure 6.7 Read Operation (One Page)

6.8 READ OPERATION (INTERCEPTED BY CE#)

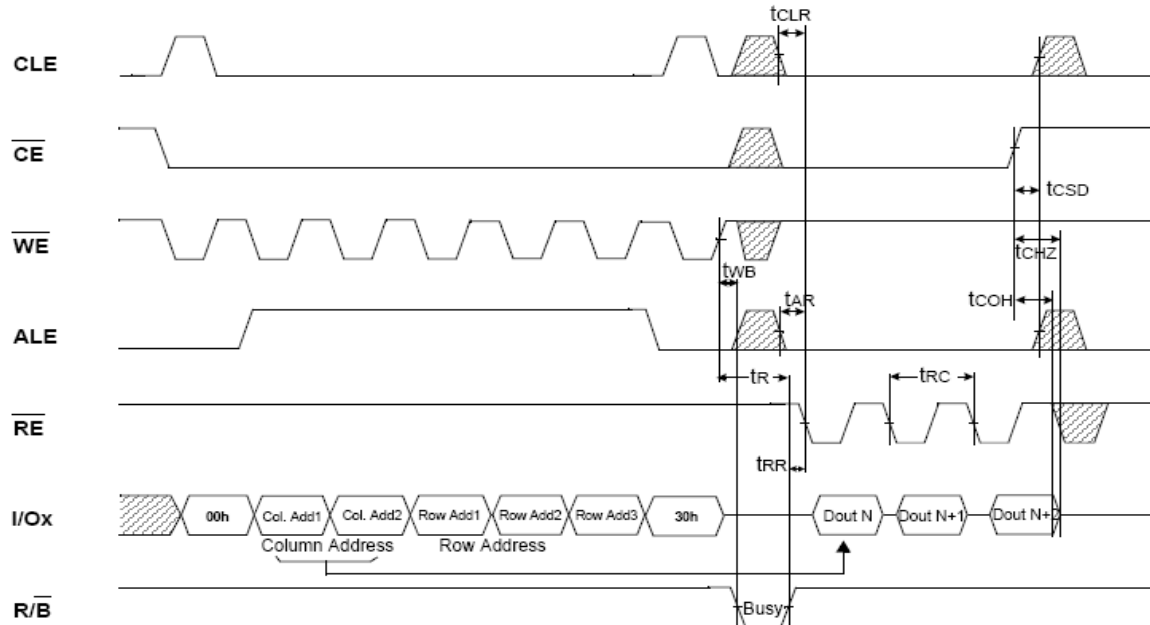


Figure 6.8 Read Operation (Intercepted by CE#)

6.9 RANDOM DATA OUTPUT IN A PAGE

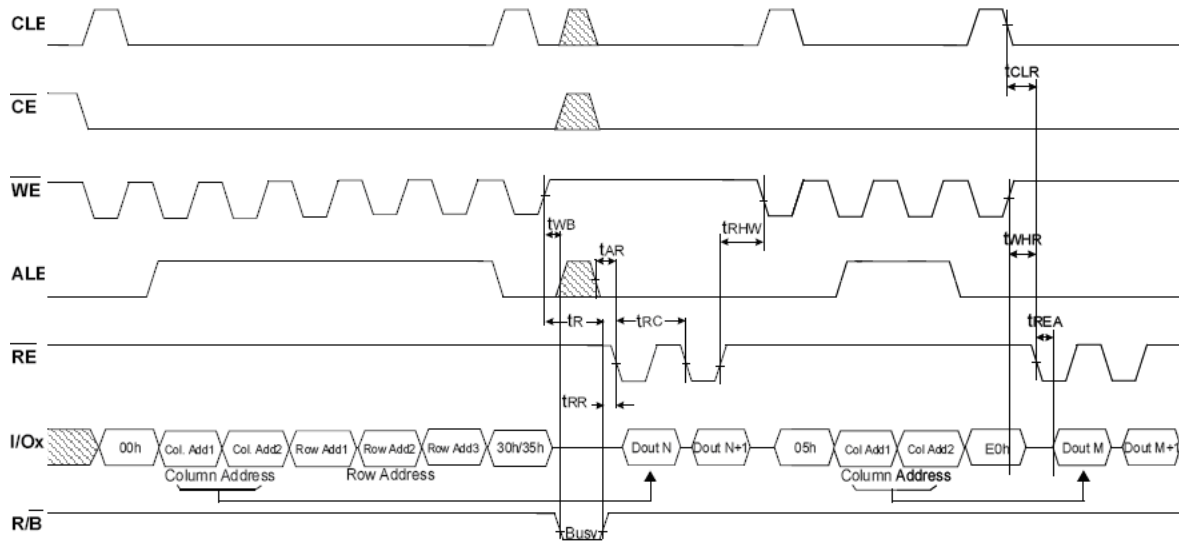


Figure 6.9 Random Data Output in a Page

6.10 PAGE PROGRAM OPERATION

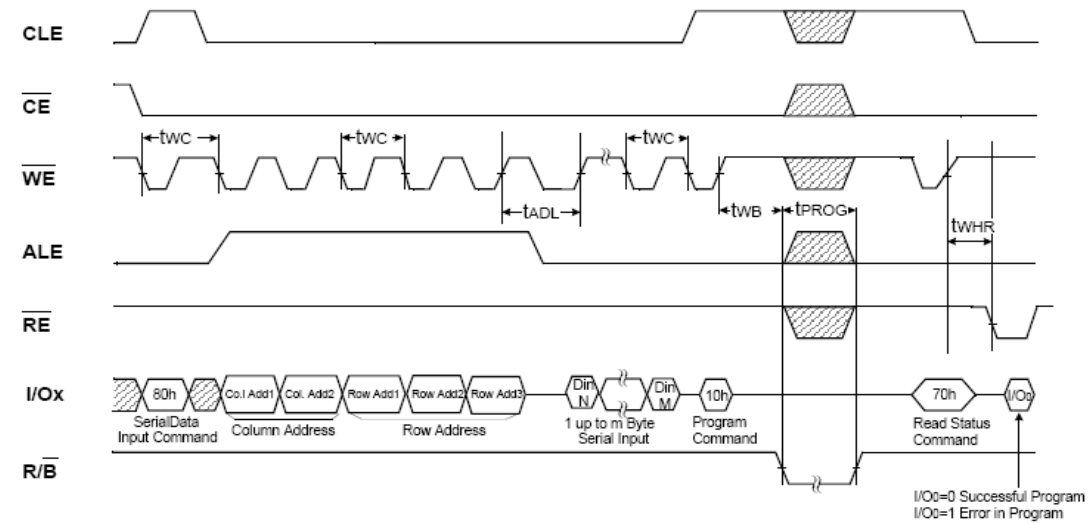


Figure 6.10 Page Program Operation