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Revision History

AS4C64M16MD2-25BCN / AS4C32M32MD2-25BCN 134 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	July. 2016

KEY FEATURE

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS, DQS#), These are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK and CK#)
- Differential data strobes (DQS and DQS#)
- Commands & addresses entered on both positive and negative CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst Length: 4 (default), 8 or 16
- Burst Type: Sequential or Interleave
- Read & Write latency : Refer to Table 47
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Auto Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Deep Power Down Mode
- HSUL_12 compatible inputs
- VDD1/VDD2/VDDQ
  : 1.8V/1.2V/1.2V
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, center aligned data input
- Auto refresh duty cycle :
  - 7.8us for -30 to 85 °C

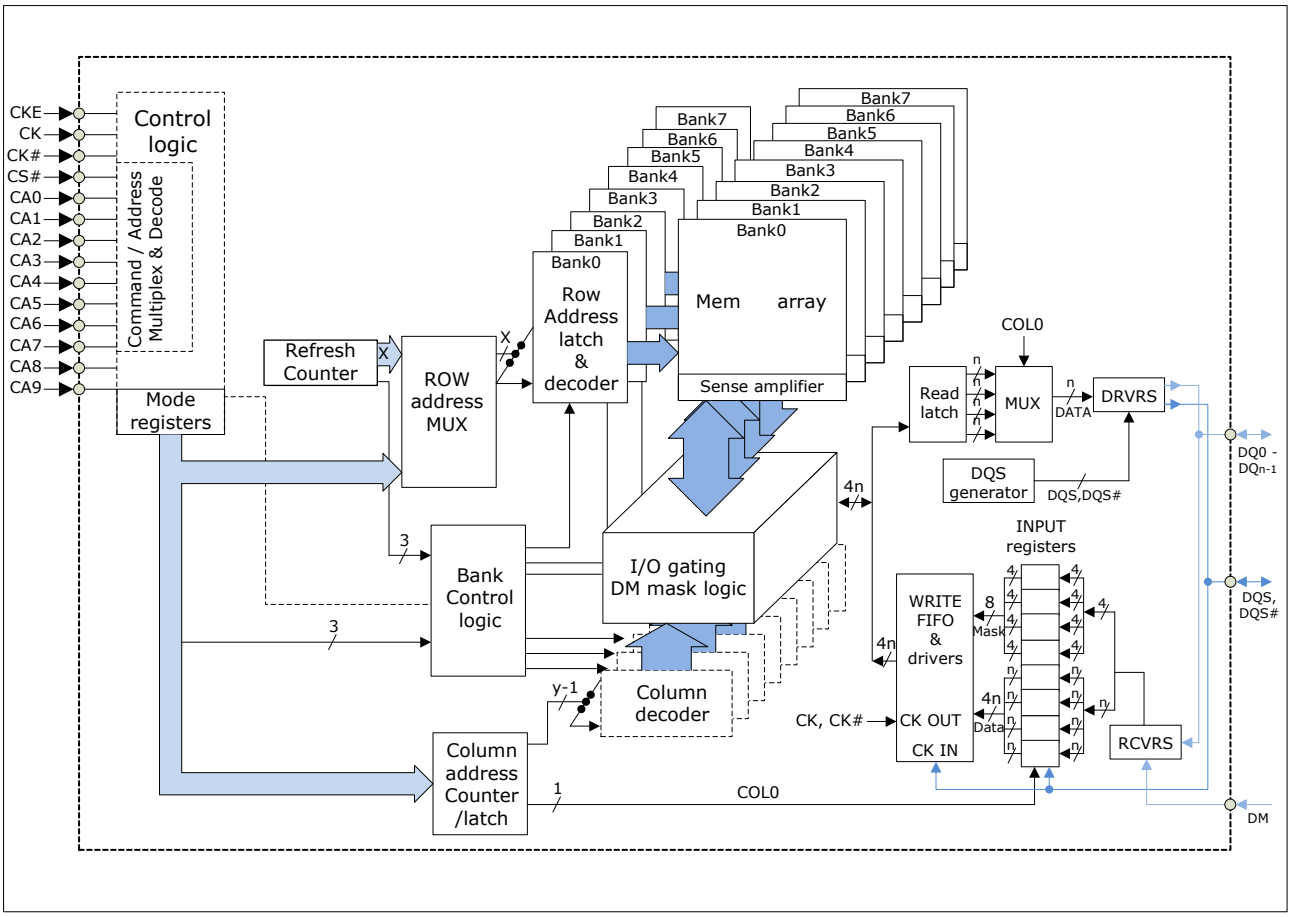
Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C64M16MD2-25BCN	64Mx16	Commercial -30°C to +85°C	400	134-ball FBGA
AS4C32M32MD2-25BCN	32Mx32	Commercial -30°C to +85°C	400	134-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	RL	WL	tRCD (ns)	tRP (ns)
DDR2L-800	400MHz	6	3	18	18

1. Functional Block Diagrams



2. Ball Descriptions

2-1. Pad Definition and Description

Name	Type	Description
CK, CK#	Input	**Clock**: CK and CK# are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CS# and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and CK#. The positive Clock edge is defined by the crosspoint of a rising CK and a falling CK#. The negative Clock edge is defined by the crosspoint of a falling CK and a rising CK#.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS#	Input	**Chip Select:** CS# is considered part of the command code. See Command Truth Table for command code descriptions. CS# is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	Data Inputs/Output: Bi-directional data bus
DQS0, DQS0#, DQS1, DQS1# (x16) DQS0 - DQS3, DQS0# - DQS3 (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0 and DQS0# correspond to the data on DQ0 - DQ7; DQS1 and DQS1# to the data on DQ8 - DQ15. For x32 DQS0 and DQS0# correspond to the data on DQ0 - DQ7, DQS1 and DQS1# to the data on DQ8 - DQ15, DQS2 and DQS2# to the data on DQ16 - DQ23, DQS3 and DQS3# to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS#). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
VDD1	Supply	**Core Power Supply 1:** Core power supply
*V*DD2	Supply	**Core Power Supply 2:** Core power supply
*V*DDQ	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
*V*REF(CA)	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS#, CK, and CK# input buffers.
*V*REF(DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers
*V*SS	Supply	**Ground**
*V*SSQ	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

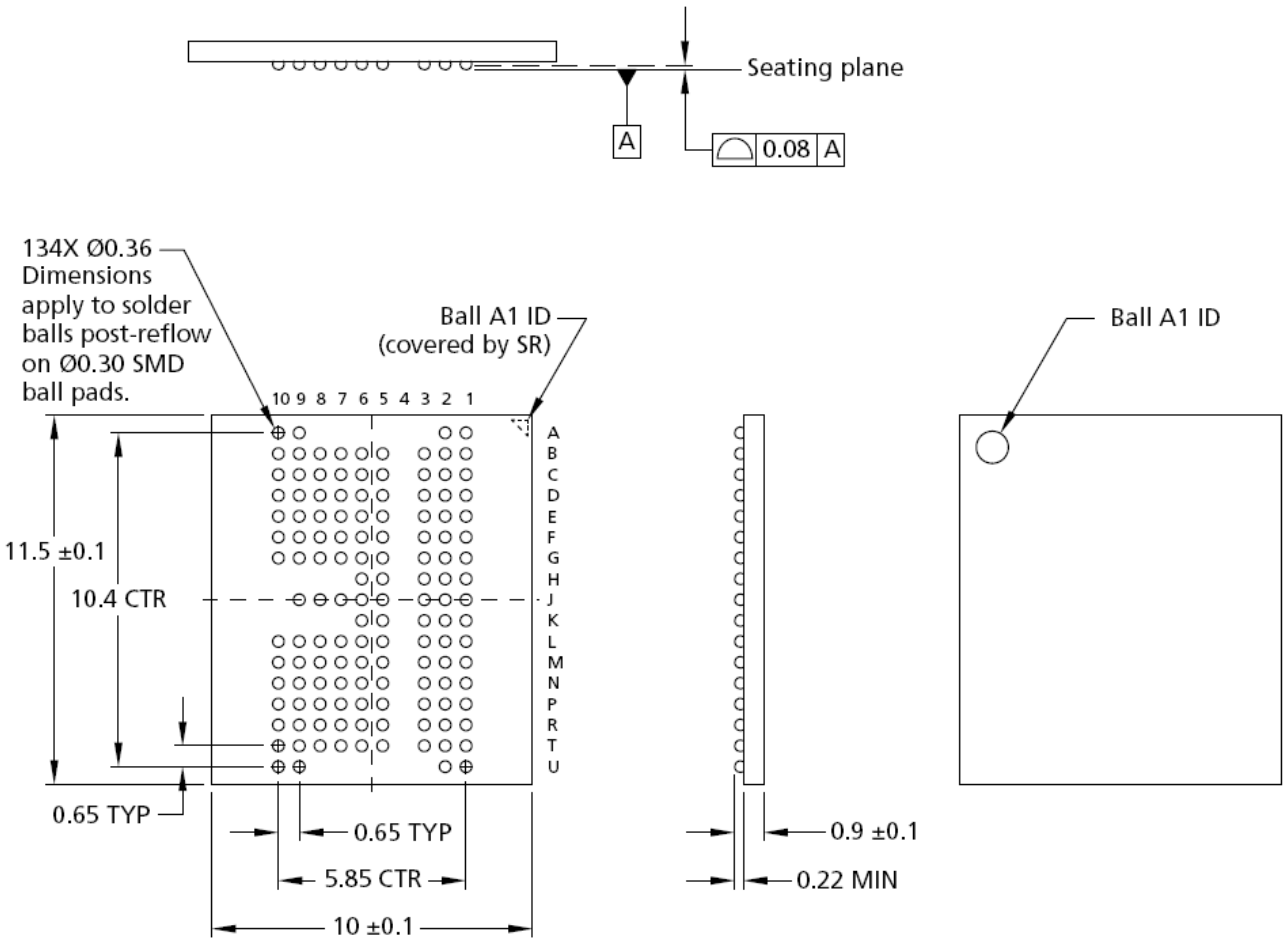
NOTE : Data includes DQ and DM

LPDDR2 SDRAM Addressing

ITEM		1Gb
Number of banks		8
Bank address pins		BA0~BA2
Auto precharge pin		A10/AP
X16	Row addresses	R0-R12
	Column addresses	C0-C9
	tREFI(μs)	7.8
X32	Row addresses	R0-R12
	Column addresses	C0-C8
	tREFI(μs)	7.8

NOTE 1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
NOTE 2. tREFI values for all bank refresh is Tc = -25~85℃, Tc means Operating Case Temperature.
NOTE 3. Row and Column Address values on the CA bus that are not used are “don’t care.”

2-2. Package Dimension : 134-Ball FBGA – 10mm x 11.5mm x 1.0mm (max)



2-3. Package Ballout

134Ball FBGA										
	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU
B	DNU	NC	NC	NB	VDD2	VDD1	DQ31 NC	DQ29 NC	DQ26 NC	DNU
C	VDD1	VSS	NC	NB	VSS	VSSQ	VDDQ	DQ25 NC	VSSQ	VDDQ
D	VSS	VDD2	ZQ0	NB	VDDQ	DQ30 NC	DQ27 NC	DQS3 NC	DQS3# NC	VSSQ
E	VSS	CA9	CA8	NB	DQ28 NC	DQ24 NC	DM3 NC	DQ15	VDDQ	VSSQ
F	NC	CA6	CA7	NB	VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)	NB	DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ
H	NC	VSS	CK#	NB	DM1	VDDQ	NB	NB	NB	NB
J	VSS	NC	CK	NB	VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	NB
K	CKE	NC	NC	NB	DM0	VDDQ	NB	NB	NB	NB
L	CS#	NC	NC	NB	DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2	NB	VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSS	NC	CA1	NB	DQ19 NC	DQ23 NC	DM2 NC	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0	NB	VDDQ	DQ17 NC	DQ20 NC	DQS2 NC	DQS2# NC	VSSQ
R	VDD1	VSS	NC	NB	VSS	VSSQ	VDDQ	DQ22 NC	VSSQ	VDDQ
T	DNU	NC	NC	NB	VDD2	VDD1	DQ16 NC	DQ18 NC	DQ21 NC	DNU
U	DNU	DNU	NB	NB	NB	NB	NB	NB	DNU	DNU

[Top View]

1st Row	x32 Device		Power		Ground
2nd Row	x16 Device		ZQ		NC/DNU
			NB		

3. Functional Description

LPDDR2 is a high-speed SDRAM device internally configured as a 8-Bank memory.

These devices contain the following number of bits:

1 Gb has 1,073,741,824 bits

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.Prior to normal operation, the LPDDR2 must be initialized..

3.1 Simplified LPDDR2 Bus Interface State Diagram

The simplified LPDDR2 bus interface state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see “LPDDR2 Command Definitions and Timing Diagrams”

Simplified LPDDR2 Bus Interface State Diagram

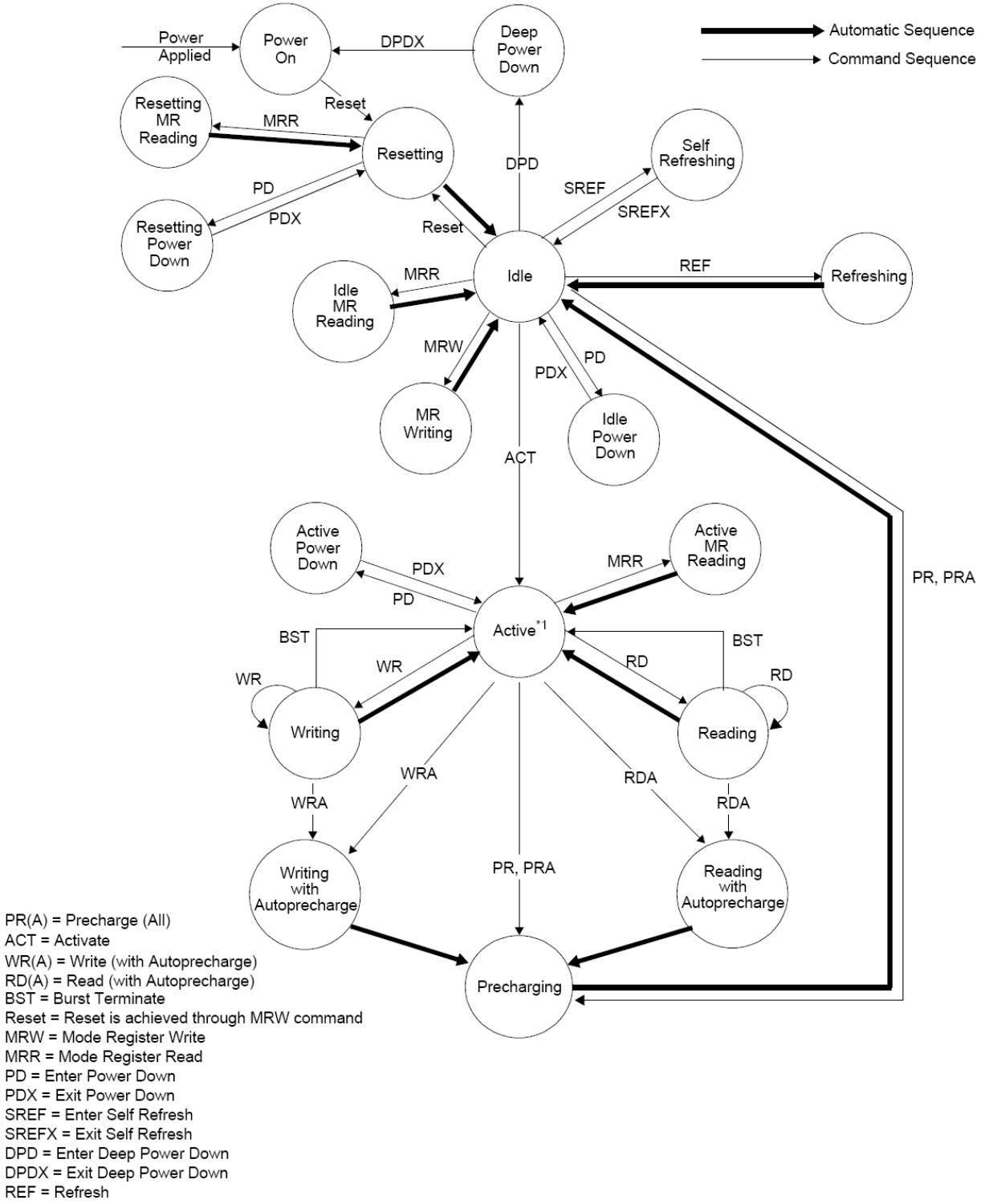


Figure 3.1 LPDDR2 : Simplified Bus Interface State Diagram

NOTE 1 These transitions apply for LPDDR2-SX devices only.
NOTE 2 For LPDDR2-SDRAM in the Idle state, all banks are precharged.
NOTE 3 Use caution with this diagram. It is intented to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one Bank/Row

3.2 Power-up, Initialization, and Power-Off

LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation

3.2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=< 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up.

CK, CK#, CS#, and CA input levels must be between VSSCA and VDD2 during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where *any* power supply first reaches 300 mV.

After Ta is reached, VDD1 must be greater than VDD2 - 200 mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDD2 - 200 mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

After Ta is reached, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.

NOTE VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

2. CKE and clock:

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 ns, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS# and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 ns to 100 ns), if any Mode Register Reads are performed.

Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 us. (Td).

3. Reset command:

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command (for LPDDR2-SX) to the MRW Reset command. Wait for at least t_{INIT4} = 1us while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.

Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see “Powerdown”).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0, “DAI”) is set to zero “DAI complete“ by the memory device, the device is in idle state (**Tf**).

The state of the DAI status bit can be determined by an MRR command to MR0.

All SDRAM devices will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration:

After tINIT5 (**Tf**), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). For

LPDDR2 devices which do not support the ZQ Calibration command, this command shall be ignored. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:
After tZQINIT (**Tg**), MRW commands shall be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.
The LPDDR2 device will now be in IDLE state and ready for any valid command.
After **Tg**, the clock frequency may be changed according to the clock frequency change procedure described in section "Input clock stop and frequency change" of this specification.

Table 1 – Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	ms	Maximum Power Ramp Time
tINIT1	100		ns	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		us	Minimum Idle time after first CKE assertion
tINIT4	1		us	Minimum Idle time after Reset command
tINIT5		10	us	Maximum duration of Device Auto-Initialization
tZQINIT	1		us	ZQ Initial Calibration for LPDDR2-S4 devices
tCKb	18	100	ns	Clock cycle time during boot

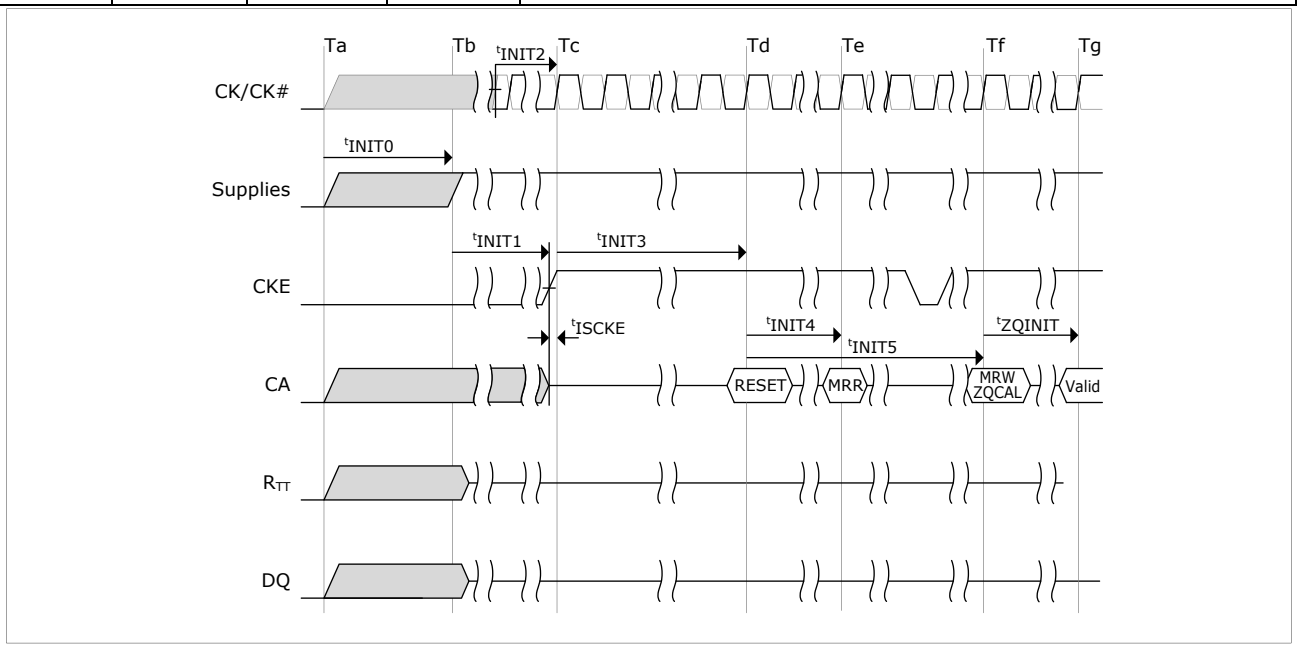


Figure 3.2 Power Ramp and Initialization Sequence

3.2.2 Initialization after Reset (without Power ramp):

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

3.2.3 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device. Unless specified otherwise, these steps are mandatory and apply to S4 devices.
While removing power, CKE shall be held at a logic low level (=< 0.2 x VDD2), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low. DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDD2 during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.
Tz is the point where *all* power supplies are below 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (tPOFF) shall be less than 2s.
The following conditions apply:
Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.
Between Tx and Tz, VDD1 and VDD2 must be greater than VDD2 - 200 mV.
Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.
Between Tx and Tz, VREF must always be less than all other supply voltages.
The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

Table 2 – Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
tPOFF	-	2	s	Maximum Power-Off ramp time

3.2.4 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.
Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.
Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.
VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.
Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

3.3 Mode Register Definition

3.3.1 Mode Register Assignment and Definition in LPDDR2 SDRAM

Table 3 shows the 16 common mode registers for LPDDR2 SDRAM Table 4 shows only LPDDR2 SDRAM mode registers. Additionally Table 5 shows RFU mode registers and Reset Command.

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 3 – Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01h	Device Feature 1	W	nWR(for AP)			WC	BT	BL		
2	02h	Device Feature 2	W	(RFU)			RL & WL				
3	03h	I/O Config-1	W	(RFU)			DS				
4	04h	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05h	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06h	Basic Config-2	R	Revision ID1							
7	07h	Basic Config-3	R	Revision ID2							
8	08h	Basic Config-4	R	I/O width		Density				Type	
9	09h	Test Mode	W	Vendor-Specific Test Mode							
10	0Ah	IO Calibration	W	Calibration Code							
11:15	0Bh~0Fh	(reserved)		(RFU)							

Table 4 — Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10h	PASR_Bank (S4)	W	Bank Mask							
17	11h	PASR_Seg	W	Segment Mask							
18:19	12h:13h	(Reserved)		(RFU)							

Mode Register Assignment in LPDDR2 SDRAM (NVM Part)

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20:31	14h~1Fh	(Do Not Use)									

Table 5 – Mode Register Assignment in LPDDR2 SDRAM

MR#	MA<7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20h	DQ Calibration Pattern A	R	See " DQ Calibration:							
33:39	21h:27h	(Do Not Use)									
40	28h	DQ Calibration Pattern B	R	See " DQ Calibration:							
41:47:00	29h:2Fh	(Do Not Use)									
48:62	30h~3Eh	(Reserved)		(RFU)							
63	3Fh	Reset	W	X							
64:126	40h:7Eh	(Reserved)		(RFU)							
127	7Fh	(Do Not Use)									
128:190	80h: BEh	Reserved for Vendor Use)		(RFU)							
191	BFh	(Do Not Use)									
192:254	C0h:FEh	Reserved for Vendor Use)		(RFU)							
255	FFh	(Do Not Use)									

The following notes apply to Tables 3-5:
NOTE 1 RFU bits shall be set to '0' during Mode Register writes.
NOTE 2 RFU bits shall be read as '0' during Mode Register reads.
NOTE 3 All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS,DQS# shall be toggled.
NOTE 4 All Mode Registers that are specified as RFU shall not be written.
NOTE 5 Writes to read-only registers shall have no impact on the functionality of the device.

MR0 Device Information (MA <7:0> =00H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI (Optional)		RFU	DI	DAI

DAI(Device Auto-Initialization Status)	Read-only	OP0	**0_B**: DAI complete **1_B**: DAI still in progress	
DI (Device Information)	Read-only	OP1	**0_B**: S4 SDRAM **1_B**: Do Not Use	
RZQI (Built in Self Test for RZQ Information)	Read -only	OP4:OP3	**00_B** : RZQ self test not supported) **01_B** : ZQ-pin may connect to VDD2 or float **10_B** : ZQ-pin may short to GND **11_B** : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD2 or float nor short to GND)	1

NOTE 1 RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
NOTE 2 If ZQ is connected to VDD2 to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDD2, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
NOTE 3 In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per NOTE 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
NOTE 4 In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-ohm +/-1%).

MR1 Device Feature 1 (MA <7:0> =01H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP<2:0>	**010_B**: BL4 (default) **011_B**: BL8 **110_B**: BL16 **All others** : reserved	
BT	Write-only	OP<3>	**0_B**: Sequential (default) **1_B**: Interleaved	1
WC	Write-only	OP<4>	**0_B**: Wrap (default) **1_B**: No wrap (allowed for SDRAM BL4 only)	
nWR	Write-only	OP<7:5>	**001_B**: nWR =3(default) **010_B**: nWR =4 **011_B**: nWR =5 **100_B**: nWR =6 **101_B**: nWR =7 **110_B** :nWR =8 All others : reserved	2

NOTE 1 BL 16, interleaved is not an official combination to be supported.
NOTE 2 Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table 6 - Burst Sequence by BL,BT, and WC

C3	C2	C1	C0	W/C	BT	BL	Burst Cycle Number are Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_B	0_B	wrap	any	4	0	1	2	3												
X	X	1_B	0_B				2	3	0	1												
X	X	X	0_B	nw	any		y	y+1	y+2	y+3												
X	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
X	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
X	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
X	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
X	1_B	1B	0_B				6	7	4	5	2	3	0	1								
X	X	X	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_B		int		illegal (not allowed)															
X	X	X	0_B	nw	any		illegal (not allowed)															

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary.

The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 7 for the respective density and bus width combinations.

Table 7 – LPDDR2- SX Non Wrap Restrictions

	1Gb
Not across full page boundary	
x16	3FE, 3FF, 000, 001
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
x16	1FE, 1FF, 200, 201
x32	None

NOTE 1 Non - wrap BL =4 data-orders shown above are prohibited

MR2 Device Feature 2 (MA <7:0> =02H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP<3:0>	**0001_B**: RL =3 /WL=1(default) **0010_B**: RL =4 /WL=2 **0011_B**: RL =5 /WL=2 **0100_B**: RL =6 /WL=3 **0101_B**: RL =7 /WL=4 **0110_B** :RL =8 /WL=4 **All others** : reserved	

MR3 I/O Configuration 1 (MA <7:0> =03H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP<3:0>	**0000_B:** reserved **0001_B**: 34.3-ohm typical **0010_B**: 40-ohm typical (default) **0011_B**: 48-ohm typical **0100_B**: 60-ohm typical **0101_B**: reserved for 68.6-ohm typical **0110_B** :80-ohm typical **0111_B** :120-ohm typical (optional) **All others** : reserved	

MR4 Device Temperature (MA <7:0> =04H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B**: SDRAM Low temperature operating limit exceeded **001_B**: 4X t_{REF}, 4x t_{REFIqb}, 4x t_{REFW} **010_B**: 2X t_{REF}, 2x t_{REFIqb}, 2x t_{REFW} **011_B**: 1X t_{REF}, 1x t_{REFIqb}, 1x t_{REFW} (≤85℃) **100_B**: Reserved **101_B**: 0.25X t_{REF}, 0.25x t_{REFIqb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B** :0.25X t_{REF}, 0.25x t_{REFIqb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B** :SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B**: OP<2:0> value has not changed since last read of MR4 **1_B**: OP<2:0> value has changed since last read of MR4

NOTE 1 A Mode Register Read from MR4 will reset OP7 to '0'.
NOTE 2 OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.

NOTE 3 If OP2 equals '1', the device temperature is greater than 85℃
NOTE 4 OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
NOTE 5 LPDDR2 might not operate properly when OP[2:0] = 000B or 111B.
NOTE 6 LPDDR2-SX devices shall be de-rated by adding 1.875 ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating in Table 52. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
NOTE 8 See "Temperature Sensor" for information on the recommended frequency of reading MR4.

MR5 Basic Configuration 1 (MA <7:0> =05H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacture ID							

LPDDR2 Manufacture ID	Read-only	OP<7:0>	**0000 0000$_B$:** Reserved **0000 0001$_B$:** Samsung **0000 0010$_B$:** Qimonda **0000 0011$_B$:** Elpida **0000 0100$_B$:** Etron **0000 0101$_B$:** Nanya **0000 0111$_B$:** Mosel **0000 1000$_B$:** Winbond **0000 1001$_B$:** ESMT **0000 1010$_B$:** Reserved **0000 1011$_B$:** Spansion **0000 1100$_B$:** SST **0000 1101$_B$:** ZMOS **0000 1110$_B$:** Intel **0001 1100$_B$:** Alliance **1111 1110$_B$:** Numonyx **1111 1111$_B$:** Micron **All Others :** Reserved	

MR6 Basic Configuration 2 (MA<7:0> = 06H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP<7:0>	**0001 0001$_B$**: Q-version	

NOTE 1 MR6 is Vendor Specific

MR7 Basic Configuration 3 (MA <7:0> =07H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP<7:0>	**0000 0000$_B$**: A-version	

NOTE 1 MR7 is Vendor Specific

MR8_Basic Configuration 4 (MA<7:0> = 08BH):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	**00$_B$**: S4 SDRAM **01$_B$**: Reserved **10$_B$**: Do Not Use **11$_B$**: Reserved	
Density	Read-only	OP<5:2>	**0000$_B$**: 64Mb **0001$_B$**: 128Mb **0010$_B$**: 256Mb **0011$_B$**: 512Mb **0100$_B$**: 1Gb **0101$_B$**: 2Gb **0110$_B$**: 4Gb **0111$_B$** 8Gb **1000$_B$**: 16Gb **1001$_B$**: 32Gb **All others** : reserved	
I/O Width	Read-only	OP<7:6>	**00$_B$**: x32 **01$_B$**: x16 **10$_B$**: x8 **11$_B$**: not used	

MR9_Test Mode (MA<7:0> = 09H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = 0AH):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP<7:0>	**0xFF$_B$**: Calibration command after initialization **0xAB$_B$**: Long calibration **0x56$_B$**: Short calibration **0xC3$_B$**: ZQ Reset **Others** : Reserved

NOTE 1 Host processor shall not write MR10 with "Reserved" values
NOTE 2 LPDDR2 devices shall ignore calibration command when a "Reserved" value is written into MR10.
NOTE 3 See AC timing table for the calibration latency.
NOTE 4 If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDD2, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the

device.
NOTE 5 LPDDR2 devices that do not support calibration shall ignore the ZQ Calibration command.
NOTE 6 Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

MR11:15_(Reserved) (MA<7:0> = 0BH-0FH):

MR16_PASR_Bank Mask (MA<7:0> = 010H): S2 and S4 SDRAM only

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Bank Mask (4-bank or 8 bank)							

S4 SDRAM :

Bank <7:0> Mask	Write-only	OP<7:0>	0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)	1

1. For 4-bank S4 SDRAM, only<3:0> are used.

OP	Bank Mask	4-Bank S4 SDRAM	8-Bank S4 SDRAM
0	XXXX XXX1	Bank 0	Bank 0
1	XXXX XX1X	Bank 1	Bank 1
2	XXXX X1XX	Bank 2	Bank 2
3	XXXX 1XXX	Bank 3	Bank 3
4	XXX1 XXXX	-	Bank 4
5	XX1X XXXX	-	Bank 5
6	X1XX XXXX	-	Bank 6
7	1XXX XXXX	-	Bank 7

MR17_PASR_Segment Mask (MA<7:0> = 011H): 1Gb ~ 8Gb S4 SDRAM only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	0_B: refresh enable to the segment (=unmasked, default) 1_B: refresh blocked (=masked)

			1Gb	2Gb, 4Gb	8Gb
Segment	OP	Segment Mask	R12 : 10	R13 : 11	R14 : 12
0	0	XXXX XXX1	000_B		
1	1	XXXX XX1X	001_B		
2	2	XXXX X1XX	010_B		
3	3	XXXX 1XXX	011_B		
4	4	XXX1 XXXX	100_B		
5	5	XX1X XXXX	101_B		
6	6	X1XX XXXX	110_B		
7	7	1XXX XXXX	111_B		

NOTE This table indicates the range of row addresses in each masked segment X is do not care for a particular segment

MR18-19_Reserved (MA<7:0> = 012H - 013H):
MR20-31_Do Not Use, NVM only

MR32_DQ Calibration Pattern A (MA<7:0> = 20H):
Reads to MR32 return DQ Calibration Pattern "A". See "DQ Calibration".

MR33:39_(Do Not Use) (MA<7:0> = 21H-27H):
MR40_DQ Calibration Pattern B (MA<7:0> = 28H):
Reads to MR40 return DQ Calibration Pattern "B". See "DQ Calibration".

MR41:47_(Do Not Use) (MA<7:0> = 29H-2FH):

MR48:62_(Reserved) (MA<7:0> = 30H-3EH):

MR63_Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

NOTE1 For additional information on MRW RESET see " Mode Register Write Command "

MR64:126_(Reserved) (MA<7:0> = 40H-7EH):

MR127_(Do Not Use) (MA<7:0> = 7FH):

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 80H-BEH):

MR191_(Do Not Use) (MA<7:0> = BFH):

MR192:254_(Reserved for Vendor Use) (MA<7:0> = C0H-FEH):

MR255_(Do Not Use) (MA<7:0> = FFH):

4. LPDDR2 Command Definitions and Timing Diagrams

4.1 Active Command

4.1.1 LPDDR2-SX: Activate Command

The SDRAM Activate command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA2 are used to select the desired bank. The row address R0 through R14 is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

• 8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

• 8-bank device Precharge All Allowance : tRP for a Precharge All command for an 8-bank device shall equal tRPab, which is greater than tRPpb.

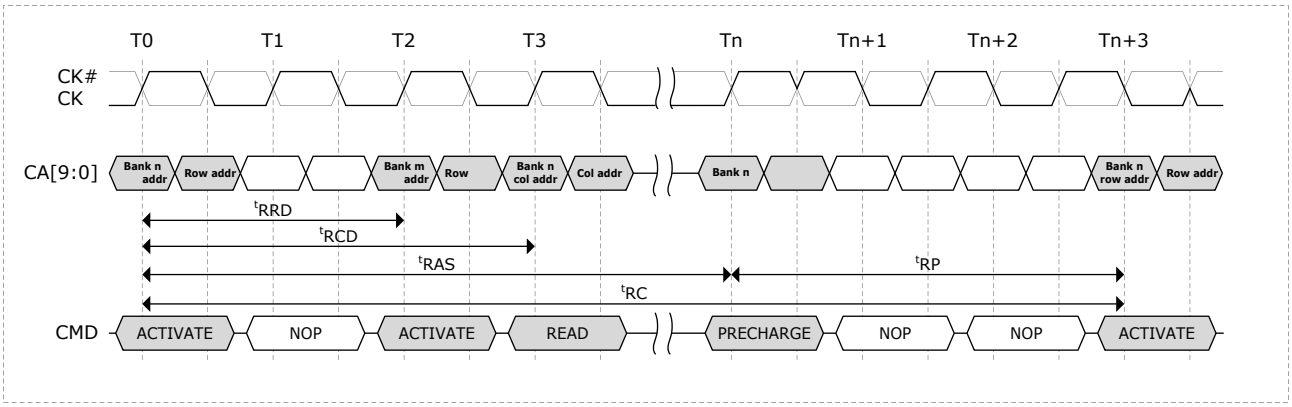


Figure 4.1 — LPDDR2-SX: Activate command cycle: t_{RCD} = 3, t_{RP} = 3, t_{RRD} = 2

NOTE 1 A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge.

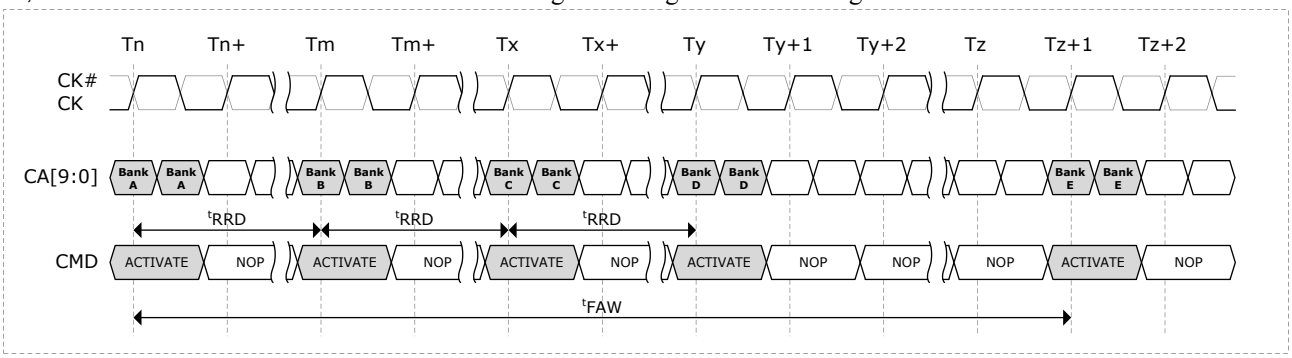
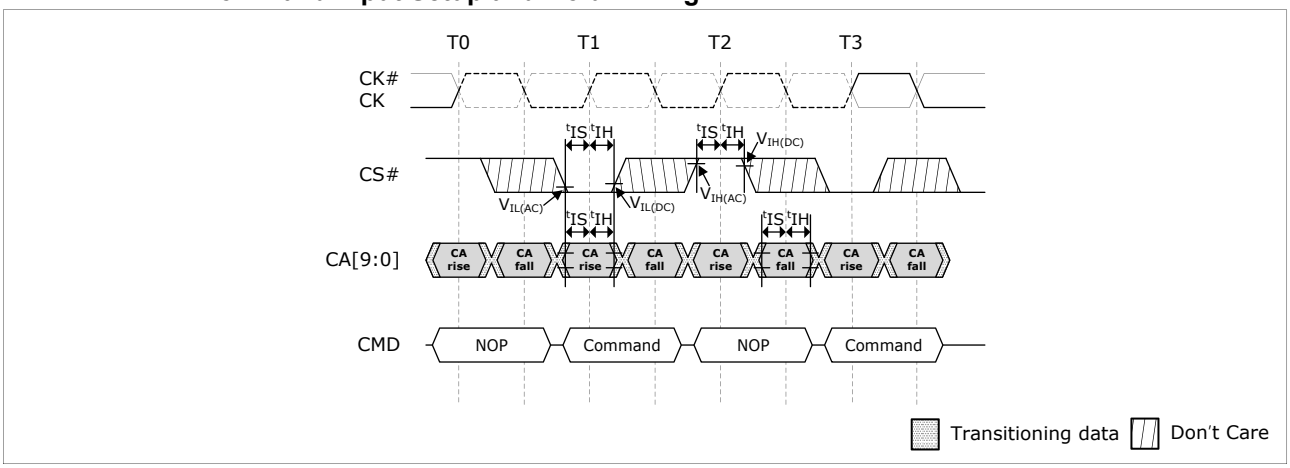


Figure 4.2 — LPDDR2-SX: t_{FAW} timing

NOTE 1: For 8-bank devices only.

4.2 LPDDR2 Command Input Signal Timing Definition

4.2.1 LPDDR2 Command Input Setup and Hold Timing



NOTE : Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 4.3 — LPDDR2: Command Input Setup and Hold Timing