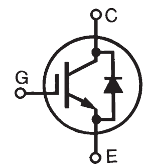
IXYS

High Voltage, High Gain BiMOSFET™

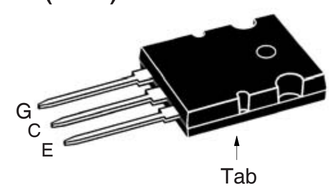
IXBK64N250
IXBX64N250

V_{CES} = 2500V
I_{C110} = 64A
$V_{CE(sat)}$ ≤ 3.0V

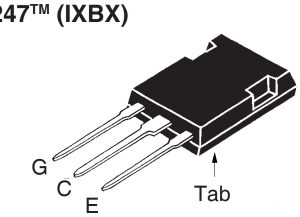
Monolithic Bipolar MOS Transistor



TO-264 (IXBK)



PLUS247™ (IXBX)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	2500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	2500	V
V_{GES}	Continuous	±25	V
V_{GEM}	Transient	±35	V
I_{C25}	T_C = 25°C (Chip Capability)	156	A
I_{LRMS}	Lead Current Limit, RMS	120	A
I_{C100}	T_C = 110°C	64	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA	V_{GE}= 15V, T_{VJ} = 125°C, R_G = 1Ω	I_{CM} = 160	A
(RBSOA)	Clamped Inductive Load	V_{CE} ≤ 0.8 • V_{CES}	
T_{SC} **(SCSOA)**	V_{GE} = 15V, T_J = 125°C, R_G = 5Ω, V_{CE} = 1250V, Non-Repetitive	10	μs
P_C	T_C = 25°C	735	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in.
F_C	Mounting Force (PLUS247)	20..120/4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	2500			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			50	μA
	T_J = 125°C			6	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = I_{C110}, V_{GE} = 15V, Note 1		2.5	3.0	V
	T_J = 125°C		3.1		V

Features

- High Blocking Voltage
- Low Switching Losses
- High Current Handling Capability
- Anti-Parallel Diode

Advantages

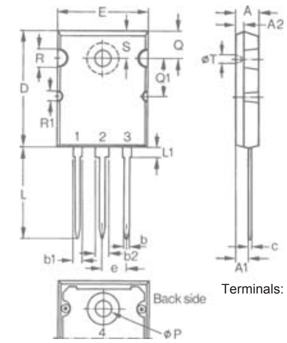
- High Power Density
- Low Gate Drive Requirement

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies (UPS)
- Capacitor Discharge Circuits
- Laser Generators

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fS}	$I_C = I_{C110}$, V_{CE} = 10V, Note 1	40	72		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		8900		pF
C_{oes}			345		pF
C_{res}			118		pF
Q_g	$I_C = I_{C110}$, V_{GE} = 15V, V_{CE} = 600V		400		nC
Q_{ge}			46		nC
Q_{gc}			155		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		49		ns
t_r	I_C = 128A, V_{GE} = 15V, tp = 1μs		318		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 1Ω		232		ns
t_f			170		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		54		ns
t_r	I_C = 128A, V_{GE} = 15V, tp = 1μs		578		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 1Ω		222		ns
t_f			175		ns
R_{thJC}				0.17	°C/W
R_{thCS}			0.15		°C/W

TO-264 Outline



Terminals: 1 - Gate
2 - Collector
3 - Emitter
4 - Collector

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

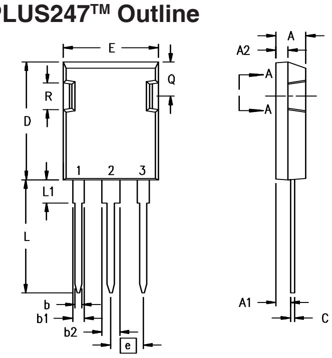
Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Min.	Typ.	Max	
V_F	$I_F = I_{C110}$, V_{GE} = 0V, Note 1			3.0	V
t_{rr}	$I_F = I_{C110}$, V_{GE} = 0V, $-di_F/dt$ = 650A/μs		160		ns
I_{RM}	V_R = 600V, V_{GE} = 0V		480		A

Note 1: Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

Additional provisions for lead-to-lead isolation are required at V_{CE} >1200V.

PLUS247™ Outline



Terminals: 1 - Gate
2 - Collector
3 - Emitter

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ T_J = 25ºC

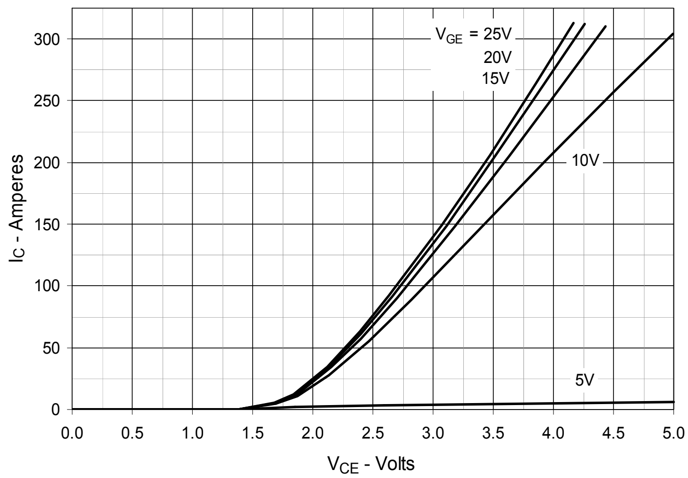


Fig. 2. Output Characteristics @ T_J = 125ºC

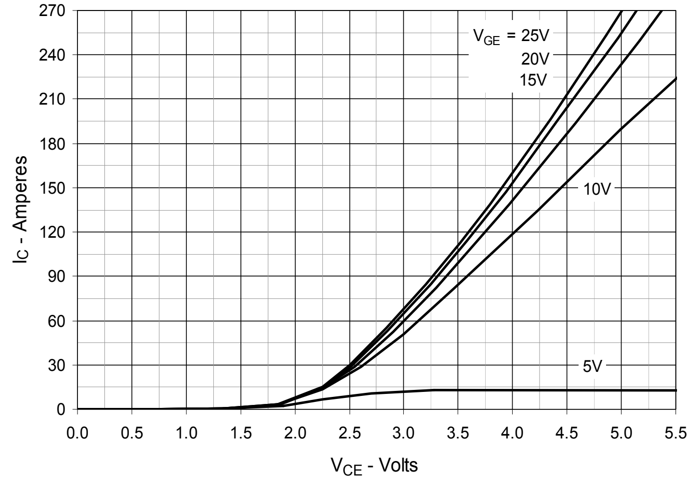


Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature

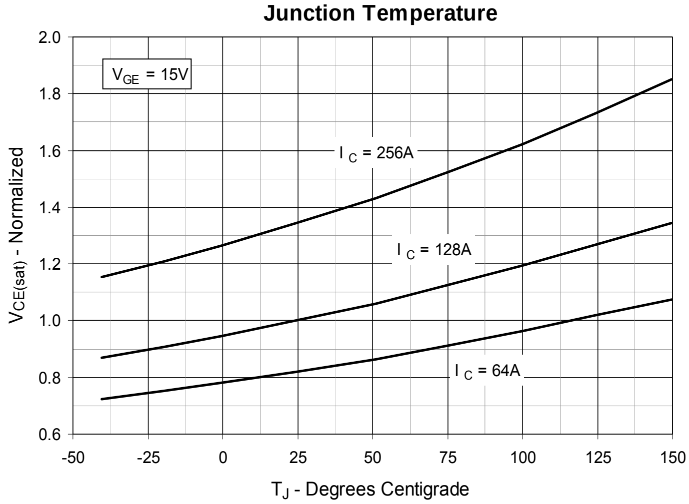


Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

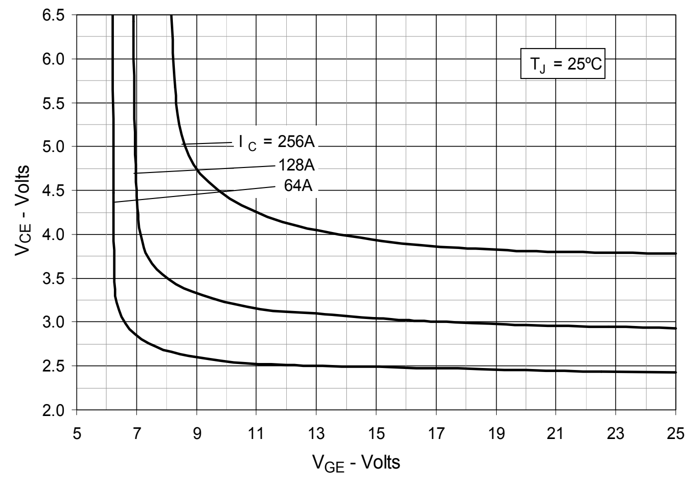


Fig. 5. Breakdown & Threshold Voltages vs. Junction Temperature

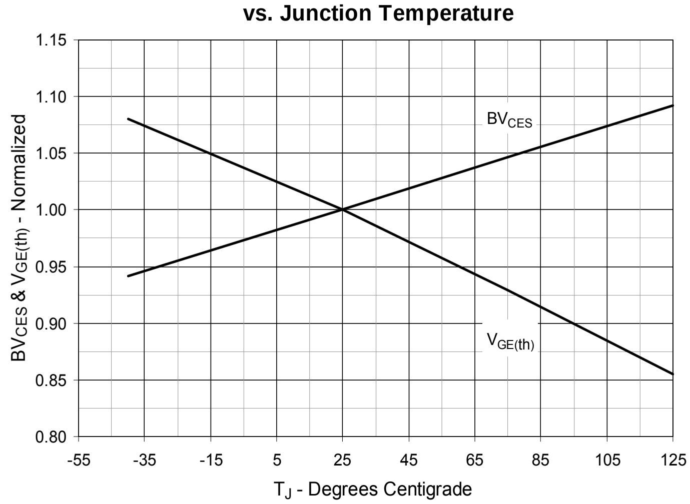


Fig. 6. Input Admittance

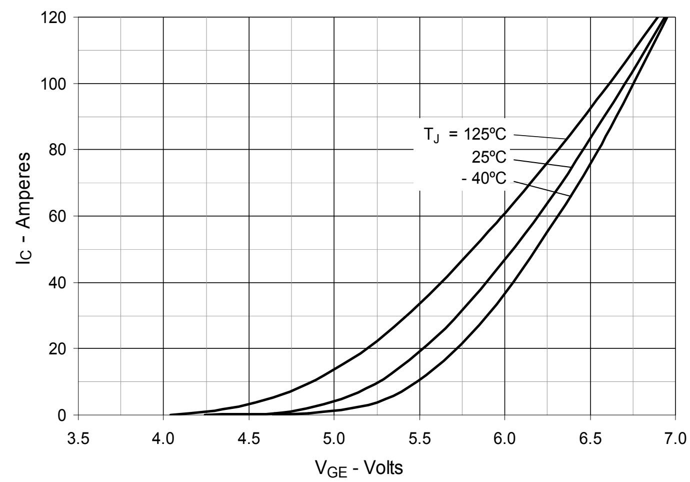


Fig. 7. Transconductance

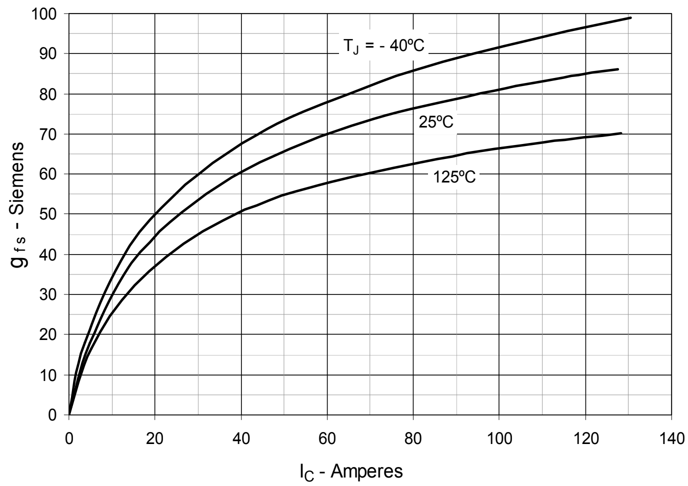


Fig. 8. Forward Voltage Drop of Intrinsic Diode

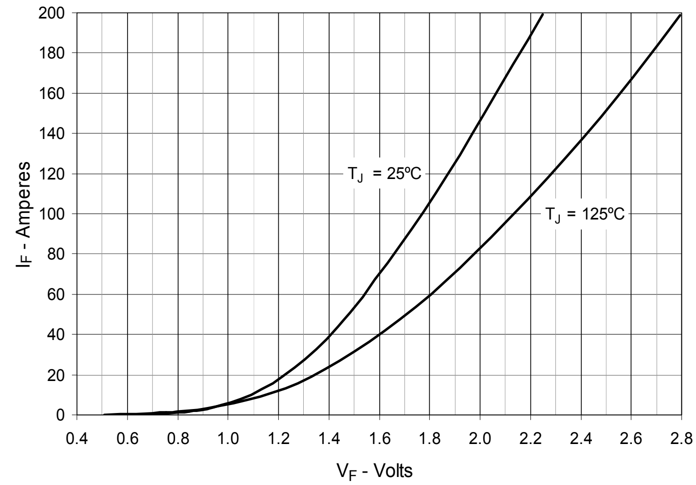


Fig. 9. Gate Charge

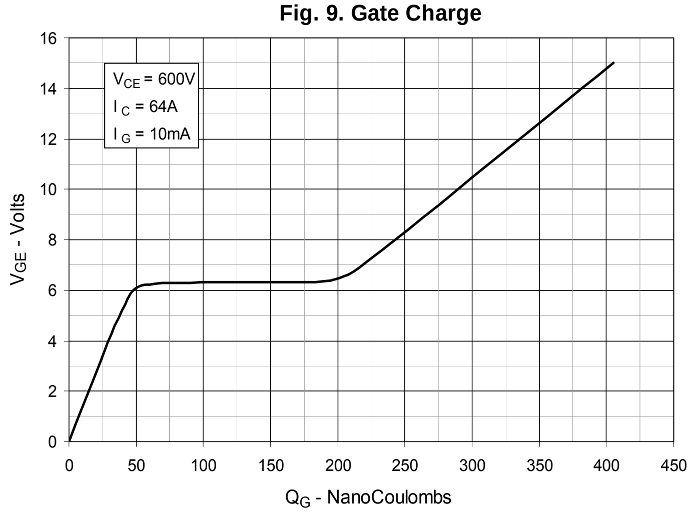


Fig. 10. Capacitance

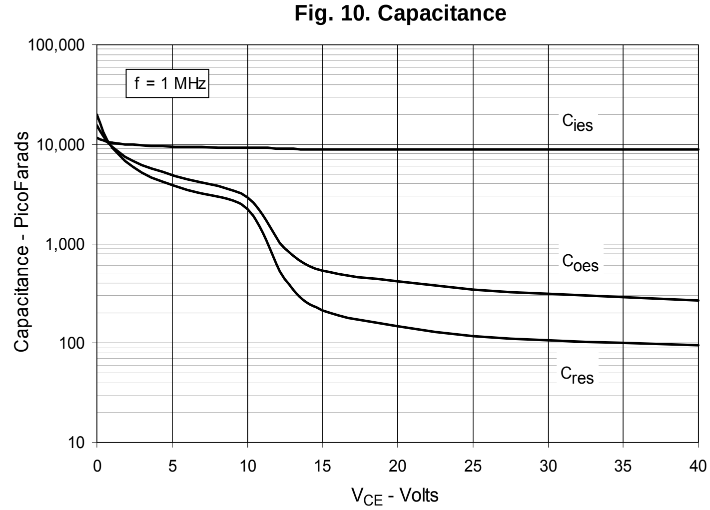


Fig. 11. Reverse-Bias Safe Operating Area

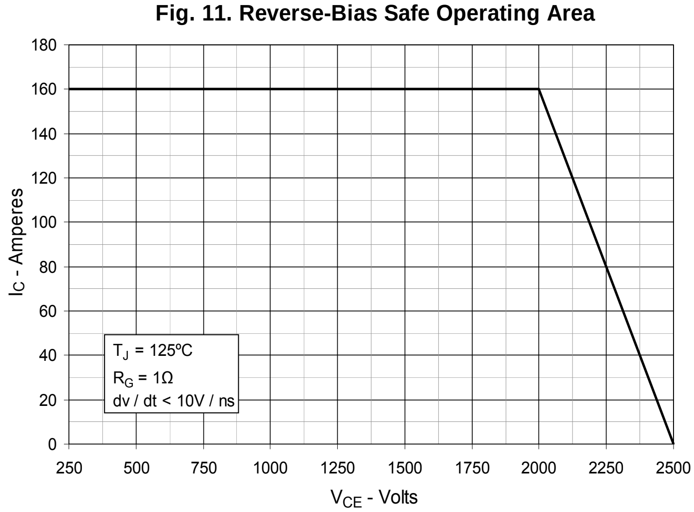


Fig. 12. Forward-Bias Safe Operating Area

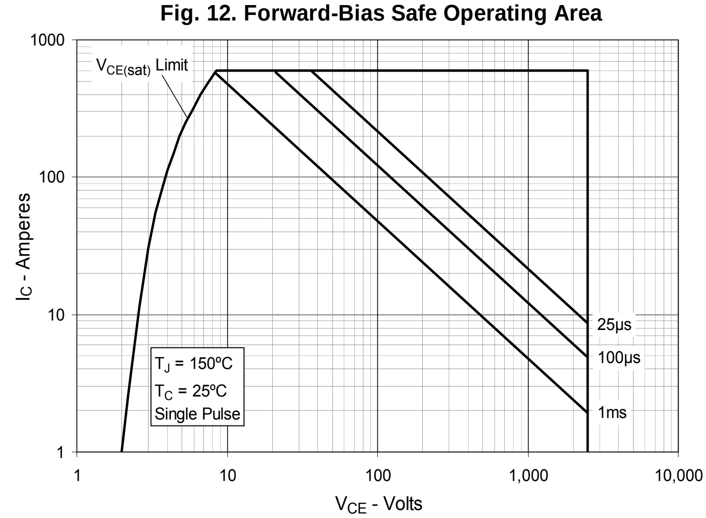


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

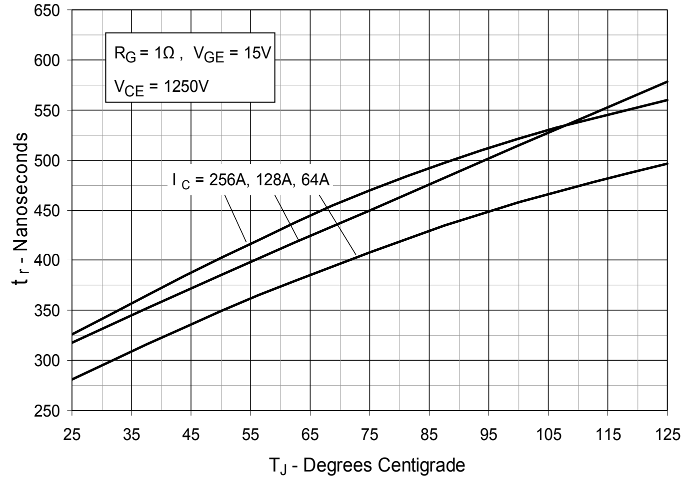


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

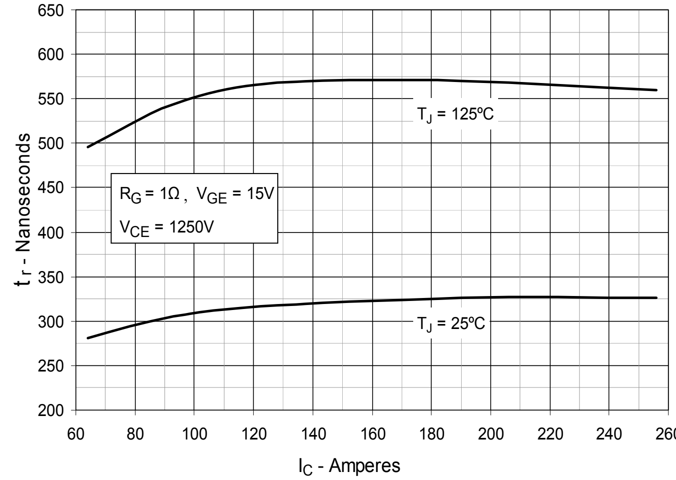


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

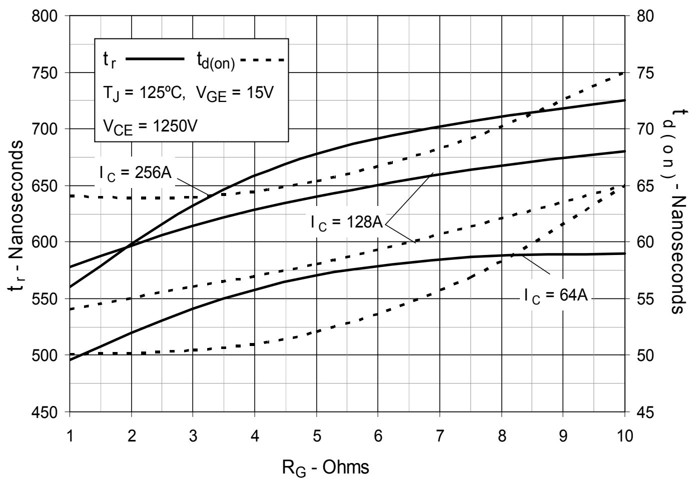


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

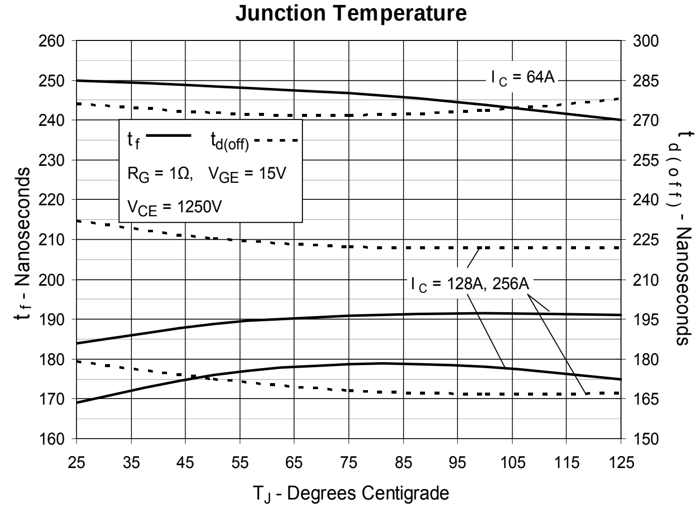


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

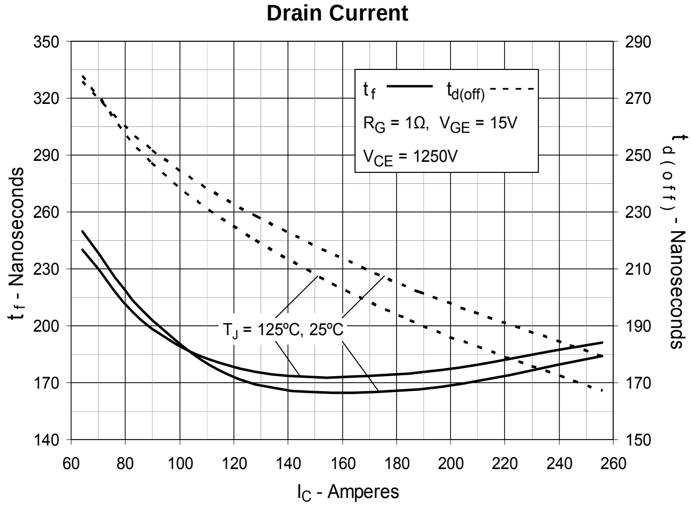
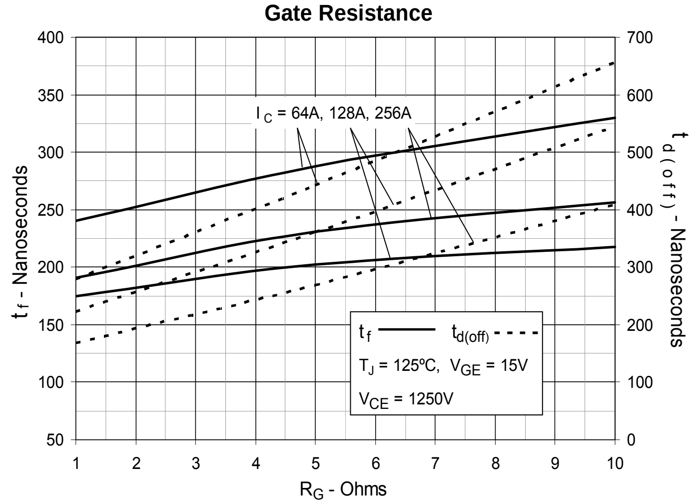


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance



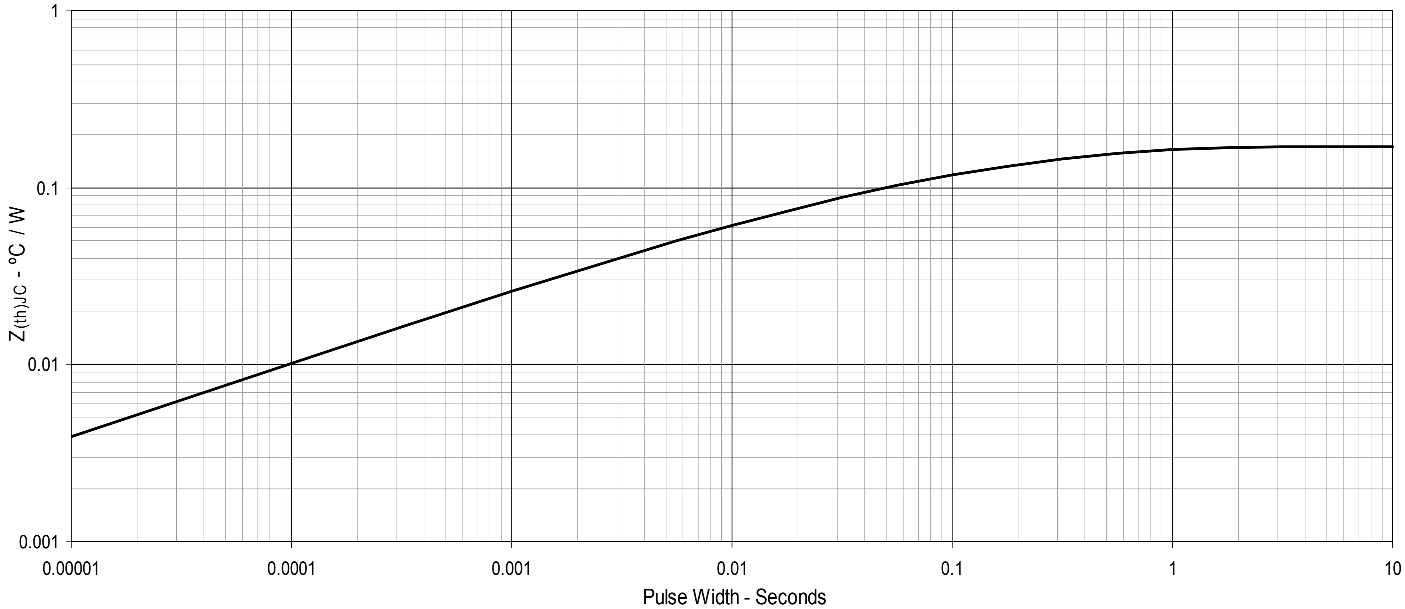


Fig. 19. Maximum Transient Thermal Impedance