ISL8117EVAL1Z Evaluation Board User Guide

Description

The ISL8117EVAL1Z evaluation board (shown in Figure 1) features the ISL8117. The ISL8117 is a 60V high voltage synchronous buck controller that offers external soft-start, independent enable functions and integrates UV/OV/OC/OT protection. Its current mode control architecture and internal compensation network keep peripheral component count minimal. Programmable switching frequency ranging from 100kHz to 2MHz helps to optimize inductor size while the strong gate driver delivers up to 30A for the buck output.

Specifications

The ISL8117EVAL1Z evaluation board is designed for high current applications. The current rating of the ISL8117EVAL1Z is limited by the FETs and inductor selected. The electrical ratings of ISL8117EVAL1Z are shown in Table 1.

TABLE 1. ELECTRICAL RATINGS

PARAMETER	RATING
Input Voltage	4.5V to 60V
Switching Frequency	600kHz
Output Voltage	3.3V
Output Current	6A
OCP Set Point	Minimum 8A at ambient room temperature

Key Features

- Small, compact design
- Wide input range: 4.5V to 60V
- High light-load efficiency in pulse skipping DEM operation
- Programmable soft-start
- Optional DEM/CCM operation
- Supports prebias output with SR soft-start
- External frequency sync
- PGOOD indicator
- OCP, OVP, OTP, UVP protection

References

- ISL8117 datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL8117EVAL1Z	High Voltage PWM Step-down Synchronous Buck Controller

FIGURE 1. ISL8117EVAL1Z TOP SIDE

FIGURE 2. ISL8117EVAL1Z BOTTOM SIDE

Recommended Testing Equipment

The following materials are recommended to perform testing:

- 0V to 60V power supply with at least 10A source current capability
- Electronic loads capable of sinking current up to 10A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

Quick Test Guide

1. Jumper J7 provides the option to select CCM or DEM. Please refer to Table 2 for the desired operating option. Ensure that the circuit is correctly connected to the supply and electronic loads prior to applying any power. Please refer to Figure 4 for proper setup.
2. Turn on the power supply.
3. Adjust input voltage V_{IN} within the specified range and observe output voltage. The output voltage variation should be within 3%.
4. Adjust load current within the specified range and observe output voltage. The output voltage variation should be within 3%.
5. Use an oscilloscope to observe output voltage ripple and phase node ringing. For accurate measurement, please refer to Figure 3 for proper test setup.

TABLE 2. OPERATING OPTIONS

JUMPER #	POSITION	FUNCTION
J7	CCM (pins 1-2)	Continuous current mode
	DEM (pins 2-3)	Diode emulation mode
J6	(Pins 1-2)	Disable the PWM

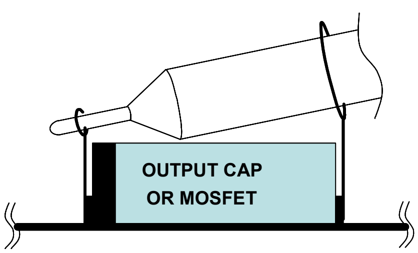

FIGURE 3. PROPER PROBE SETUP TO MEASURE OUTPUT RIPPLE AND PHASE NODE RINGING

Functional Description

The ISL8117EVAL1Z is a compact design with high efficiency and high power density.

As shown in Figure 4 on page 3, 4.5V to 60V V_{IN} is supplied to J1 (+) and J2 (-). The regulated 12V output on J3 (+) and J5 (-) can supply up to 6A to the load.

As shown in Table 2, connector J7 provides selection of either CCM mode (shorting pin 1 and pin 2) or DEM mode (shorting pin 2 and pin 3). Connector J6 provides an option to disable the converter by shorting its pin 1 and pin 2.

Operating Range

The input voltage range is from 4.5V to 60V for an output voltage of 3.3V. The rated load current is 6A with the OCP point set at minimum 8A at room temperature ambient conditions.

The temperature operating range of ISL8117 is -40°C to +125°C. Please note that airflow is needed for higher temperature ambient conditions.

PCB Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL8117 based DC/DC converter. The ISL8117 switches at a very high frequency and therefore the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device overvoltage stress and ringing. Careful component selection and proper PC board layout minimizes the magnitude of these voltage spikes.

There are three sets of critical components in a DC/DC converter using the ISL8117: the controller, the switching power components and the small signal components. The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer printed circuit board is recommended.

Layout Considerations

1. The input capacitors, upper FET, lower FET, inductor and output capacitor should be placed first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitors very close to the MOSFETs.
2. If signal components and the IC are placed in a separate area to the power train, it is recommended to use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for power ground and small signal ground. Connect the SGND and PGND together close to the IC. DO NOT connect them together anywhere else.
3. The loop formed by the input capacitor, the top FET and the bottom FET must be kept as small as possible.
4. Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the lower FET. The LGATE connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place VCC5V bypass capacitor very close to the VCC5V pin of the IC and connect its ground to the PGND plane.
7. Place the gate drive components - optional BOOT diode and BOOT capacitors - together near the controller IC.
8. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances.
9. Use copper filled polygons or wide but short trace to connect the junction of the upper FET, lower FET and output inductor. Also keep the PHASE node connection to the IC short. DO NOT unnecessarily oversize the copper islands for the PHASE node. Since the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise.
10. Route all high speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths including feedback resistors, current limit setting resistor, soft-starting capacitor and EN pull-down resistor should be connected to this SGND plane.
12. Separate the current sensing trace from the PHASE node connection.
13. Ensure the feedback connection to the output capacitor is short and direct.

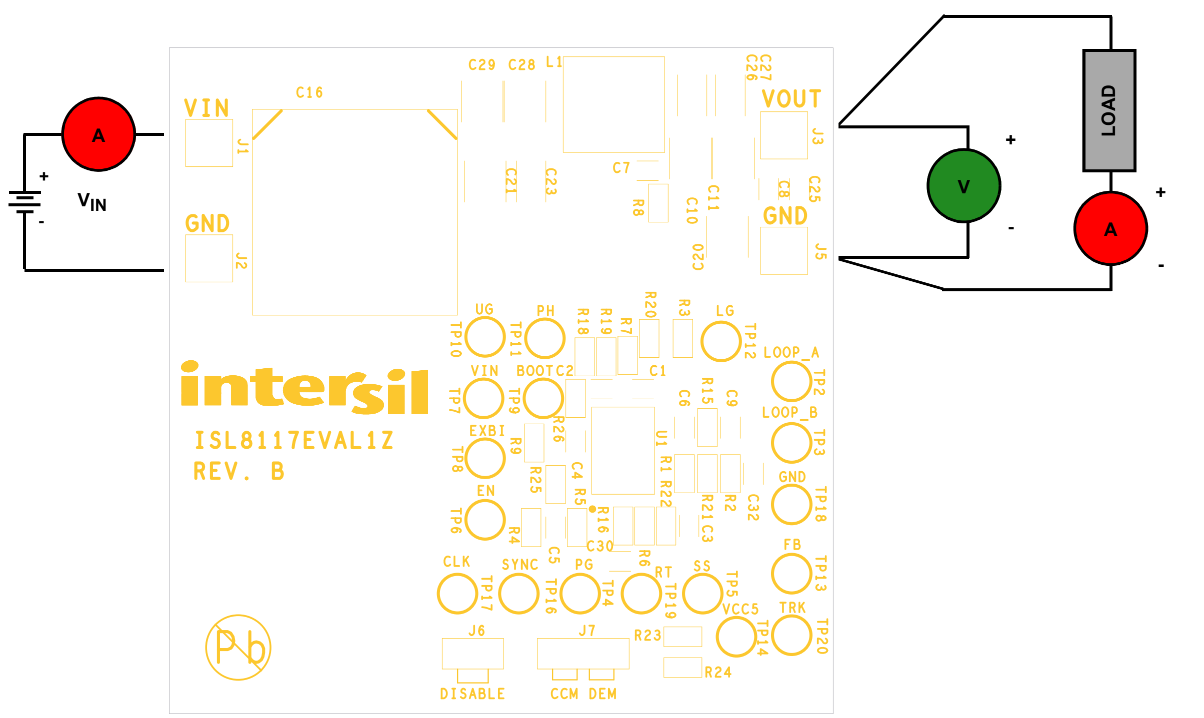

FIGURE 4. PROPER TEST SETUP

Typical Evaluation Board Performance Curves V_{IN} = 24V, V_{OUT} = 3.3V, unless otherwise noted.

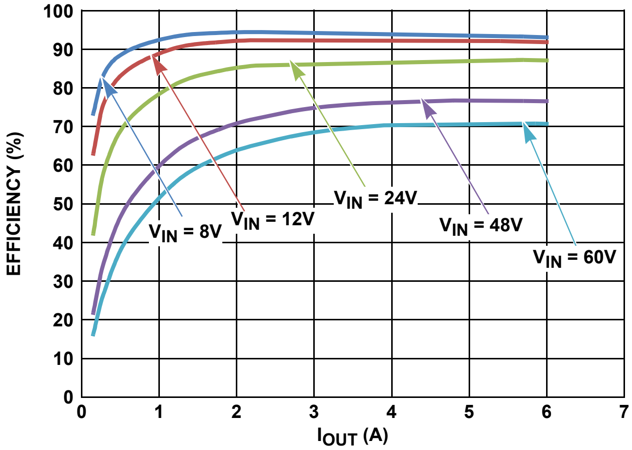

FIGURE 5. CCM EFFICIENCY

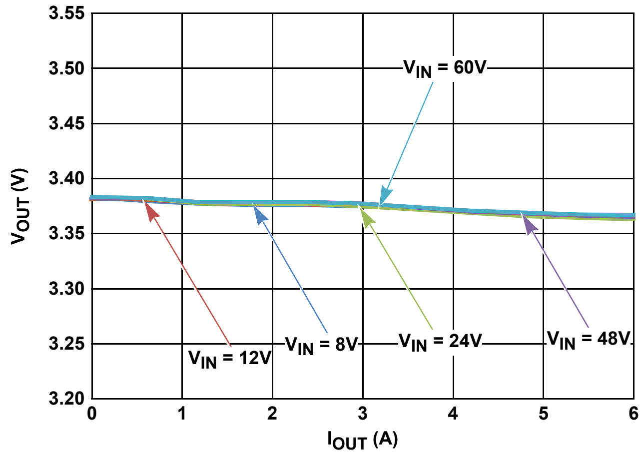

FIGURE 6. CCM LOAD REGULATION

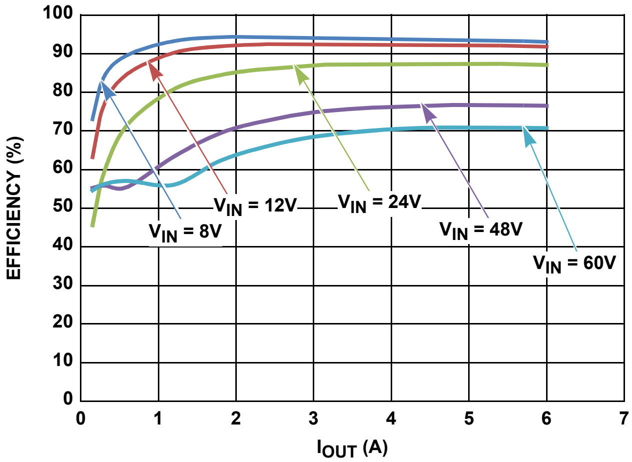

FIGURE 7. DEM EFFICIENCY

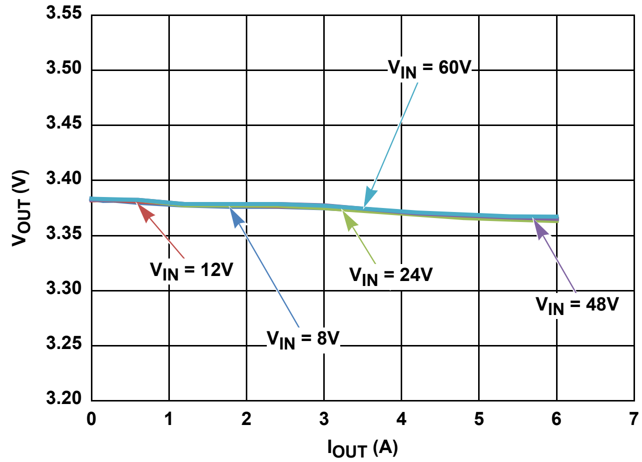

FIGURE 8. DEM LOAD REGULATION

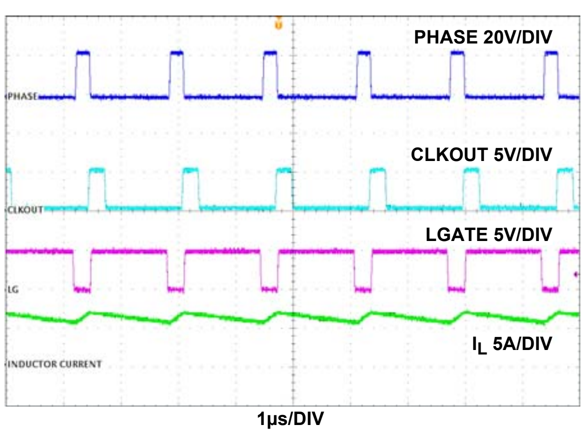

FIGURE 9. PHASE, LGATE, CLKOUT AND INDUCTOR CURRENT WAVEFORMS, I_O = 6A

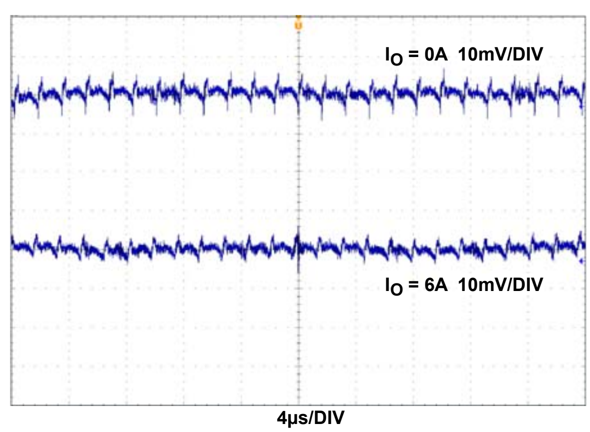

FIGURE 10. OUTPUT RIPPLE, MODE = CCM

Typical Evaluation Board Performance Curves

V_{IN} = 24V, V_{OUT} = 3.3V, unless otherwise noted.

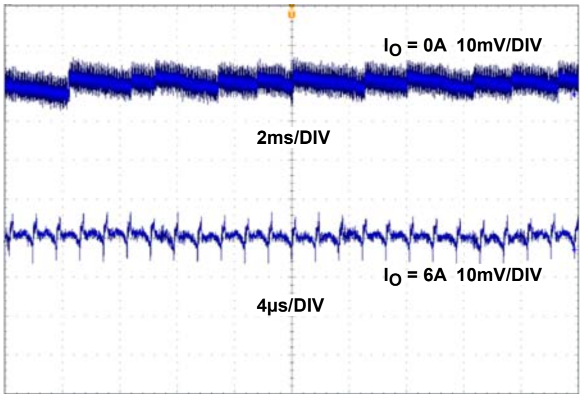

FIGURE 11. OUTPUT RIPPLE, MODE = DEM

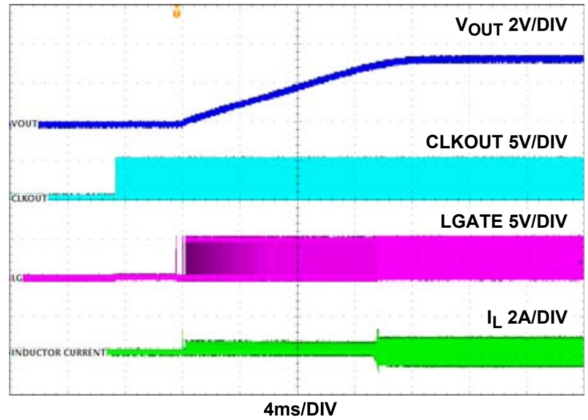

FIGURE 12. CCM START-UP WAVEFORMS: V_{OUT}, LGATE, CLKOUT, I_L, I_O = 0A

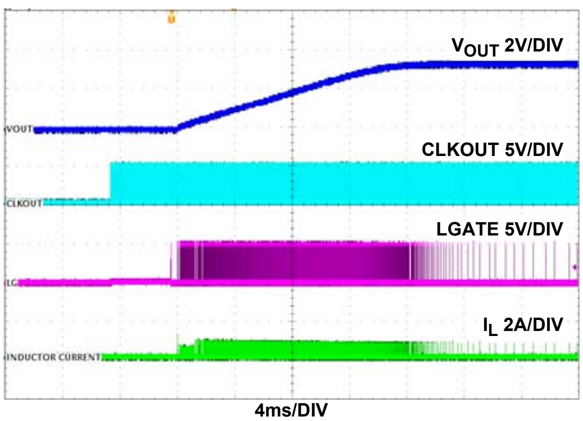

FIGURE 13. DEM START-UP WAVEFORMS: V_{OUT}, LGATE, CLKOUT, I_L, I_O = 0A

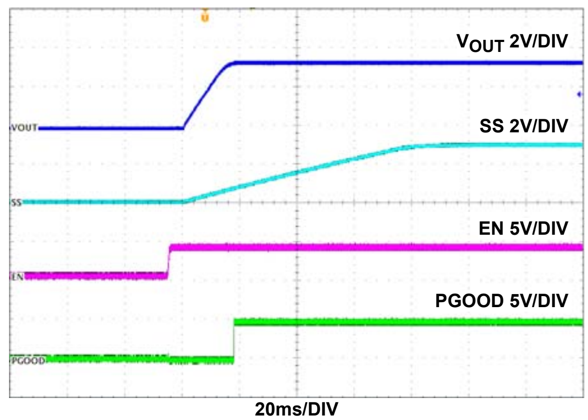

FIGURE 14. CCM START-UP WAVEFORMS: V_{OUT}, SS, EN, PGOOD, I_O = 0A

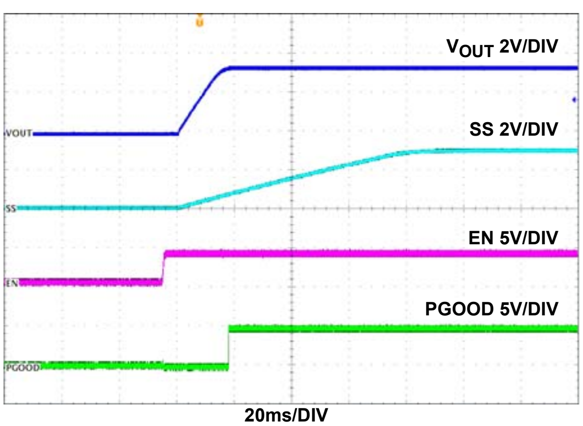

FIGURE 15. DEM START-UP WAVEFORMS: V_{OUT}, SS, EN, PGOOD, I_O = 0A

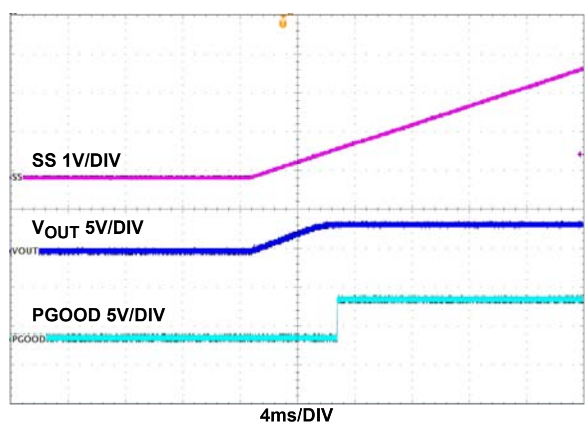

FIGURE 16. TRACKING WAVEFORMS, I_O = 0A

Typical Evaluation Board Performance Curves
V_{IN} = 24V, V_{OUT} = 3.3V, unless otherwise noted.

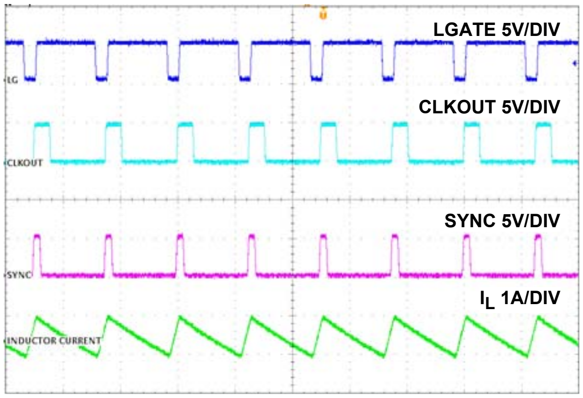

FIGURE 17. FREQUENCY SYNCHRONIZATION WAVEFORMS, I_O = 0A

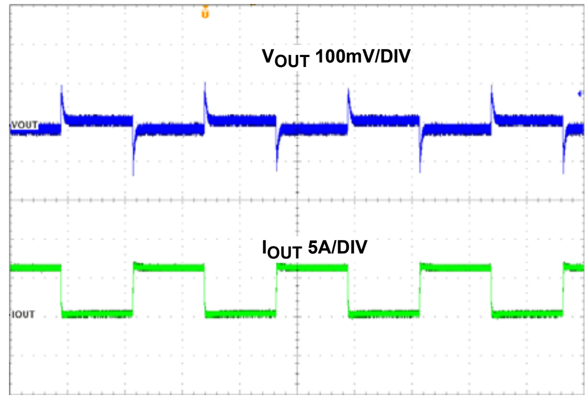

FIGURE 18. LOAD TRANSIENT, I_O = 0A TO 6A, 1A/µs, CCM

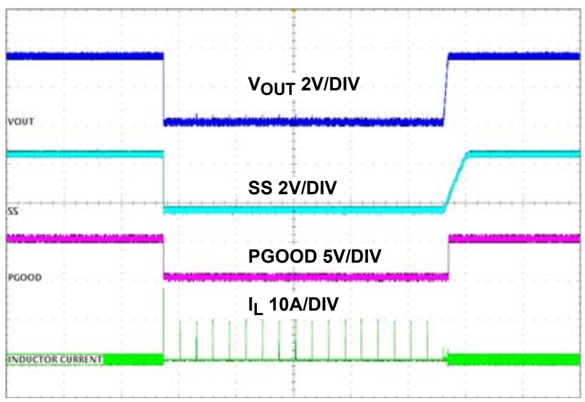

FIGURE 19. SHORT CIRCUIT WAVEFORMS

Schematic

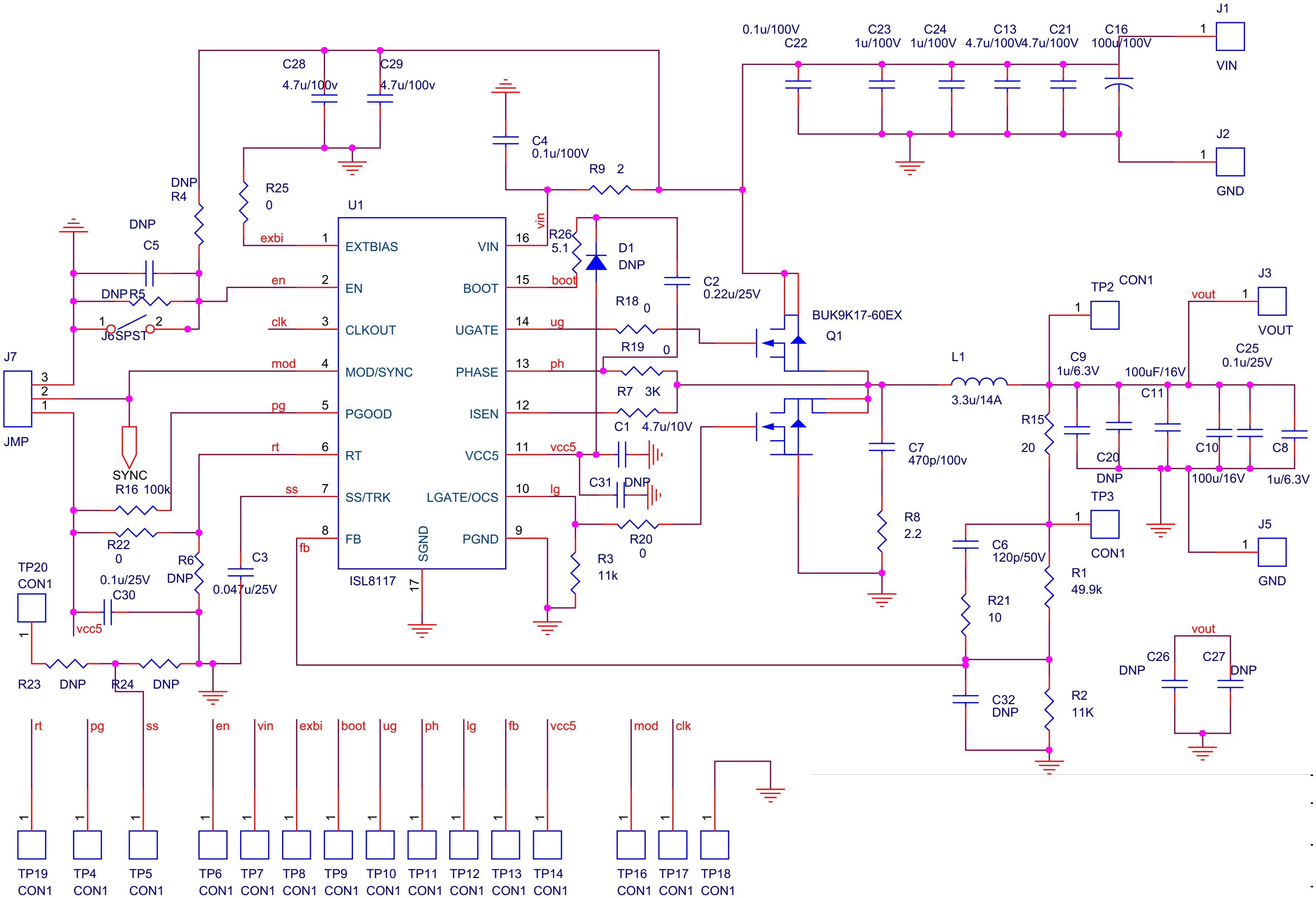

FIGURE 20. ISL8117EVAL1Z SCHEMATIC

ISL8117EVAL1Z Bill of Materials

MANUFACTURER PART	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL8117EVAL1ZREVBPCB	1	ea		PWB-PCB, ISL8117EVAL1Z, REVB, ROHS	SHENZHEN MULTILAYER PCB TECHNOLOGY CO., LTD
GRM32EC70J107ME15L	2	ea	C10, C11	CAP, SMD, 1210, 100µF, 6.3V, 20%, X7S, ROHS	MURATA
C0603X7R101-104KNE	2	ea	C4, C22	CAP, SMD, 0603, 0.1µF, 100V, 10%, X7R, ROHS	VENKEL
GRM39X7R104K025AD	2	ea	C25, C30	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	MURATA
ECJ1VB0J105K	2	ea	C8, C9	CAP, SMD, 0603, 1µF, 6.3V, 10%, X5R, ROHS	PANASONIC
C1608C0G1H121J080AA	1	ea	C6	CAP, SMD, 0603, 120pF, 50V, 5%, C0G, ROHS	TDK
C1608X7R1E224K	1	ea	C2	CAP, SMD, 0603, 0.22µF, 25V, 10%, X7R, ROHS	TDK
VJ0603Y471KXBA	1	ea	C7	CAP, SMD, 0603, 470pF, 100V, 10%, X7R, ROHS	VISHAY
GRM188R71E473KA01D	1	ea	C3	CAP, SMD, 0603, 0.047µF, 25V, 10%, X7R, ROHS	MURATA
0805ZD475MAT2A	1	ea	C1	CAP, SMD, 0805, 4.7µF, 10V, 20%, X5R, ROHS	AVX
C1206X7R101-105KNE	2	ea	C23, C24	CAP, SMD, 1206, 1µF, 100V, 10%, X7R, ROHS	VENKEL
CGA6M3X7S2A475K200AB	4	ea	C13, C21, C28, C29	CAP, SMD, 1210, 4.7µF, 100V, 10%, X7S, ROHS	TDK
	0	ea	C20	CAP, SMD, 1210, DNP-PLACE HOLDER, ROHS	
7443340330	1	ea	L1	COIL-PWR INDUCTOR, SMD, 8.4x7.9, 3.3µH, 20%, 14A, ROHS	Wurth Electronics
EMVH101GDA101MLH0S	1	ea	C16	CAP, SMD, 16x16.5mm, 100µF, 100V, 20%, ALUM.ELEC., ROHS	UNITED CHEMI-CON
1514-2	4	ea	J1, J2, J3, J5	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
5007	18	ea	TP2-TP14, TP16-TP20	CONN-COMPACT TEST PT, VERTICAL, WHT, ROHS	KEYSTONE
68000-236HLF	1	ea	J7	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI
69190-202HLF	1	ea	J6	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS	BERG/FCI
SPC02SYAN	2	ea	J6, J7	CONN-JUMPER, SHORTING, 2P, BLACK, GOLD, ROHS	SULLINS
ISL8117FVEZ	1	ea	U1	IC-55V SWITCHING CONTROLLER, 16P, HTSSOP, ROHS	INTERSIL
BUK9K17-60EX	1	ea	Q1	TRANSIST-MOS, DUAL N-CHANNEL, SMD, 8P, 56LFPAK, 60V, 26A, ROHS	NXP SEMICONDUCTOR
RK73H1JT10R0F	1	ea	R21	RES, SMD, 0603, 10Ω, 1/10W, 1%, TF, ROHS	KOA
ERJ-3EKF20R0V	1	ea	R15	RES, SMD, 0603, 20Ω, 1/10W, 1%, TF, ROHS	PANASONIC
ERJ-3RQF2R2V	2	ea	R8, R9	RES, SMD, 0603, 2.2Ω, 1/10W, 1%,TF, ROHS	PANASONIC
CR0603-10W-05R1FT	1	ea	R26	RES, SMD, 0603, 5.1Ω, 1/10W, 1%, TF, ROHS	VENKEL
CR0603-10W-000T	5	ea	R18, R19, R20, R22, R25	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL
CR0603-10W-1003FT	1	ea	R16	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	VENKEL
ERJ-3EKF1102V	2	ea	R2, R3	RESISTOR, SMD, 0603, 11k, 1/10W, 1%, TF, ROHS	PANASONIC
RC0603FR-073KL	1	ea	R7	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	YAGEO
CR0603-10W-4992FT	1	ea	R1	RES, SMD, 0603, 49.9k, 1/10W, 1%, TF, ROHS	VENKEL
	0	ea	R4, R5, R6, R23, R24	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	
	0	ea	C26, C27	RES, SMD, 1206, DNP, DNP, DNP, TF, ROHS	
R25-1001002	4	ea	Four corners	STANDOFF, M2.5, 10mm, METRIC, F/F, HEX, THREADED, ROHS	HARWIN INC

ISL8117EVAL1Z Bill of Materials (Continued)

MANUFACTURER PART	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
29301	4	ea	Four corners	SCREW, M2.5, 6mm, METRIC, PANHEAD, SLOTTED, STEEL, ROHS	KEYSTONE
	0	ea	C5, C31, C32	DO NOT POPULATE OR PURCHASE	
	0	ea	D1	DO NOT POPULATE OR PURCHASE	

ISL8117EVAL1Z PCB Layout

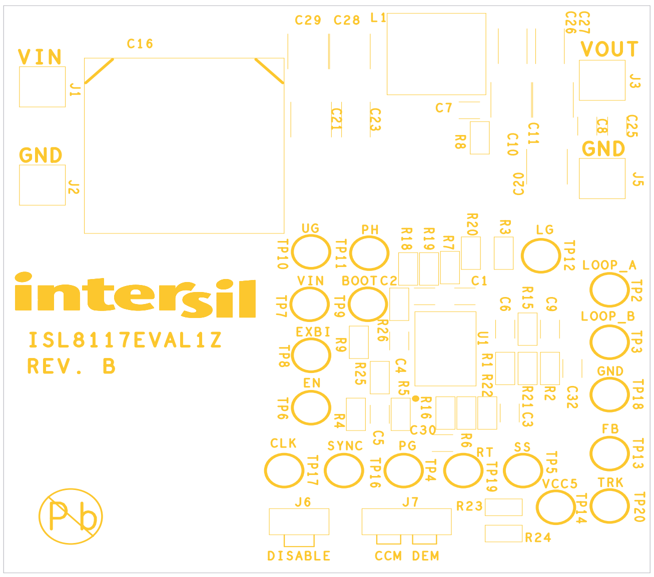

FIGURE 21. SILKSCREEN TOP

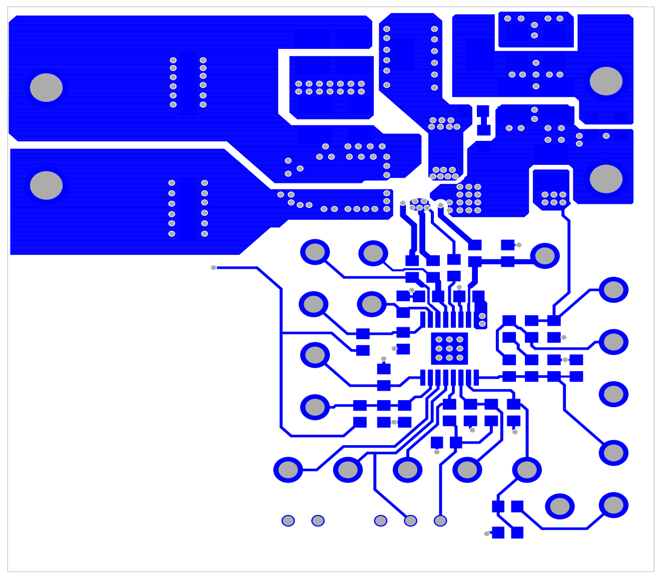

FIGURE 22. TOP LAYER

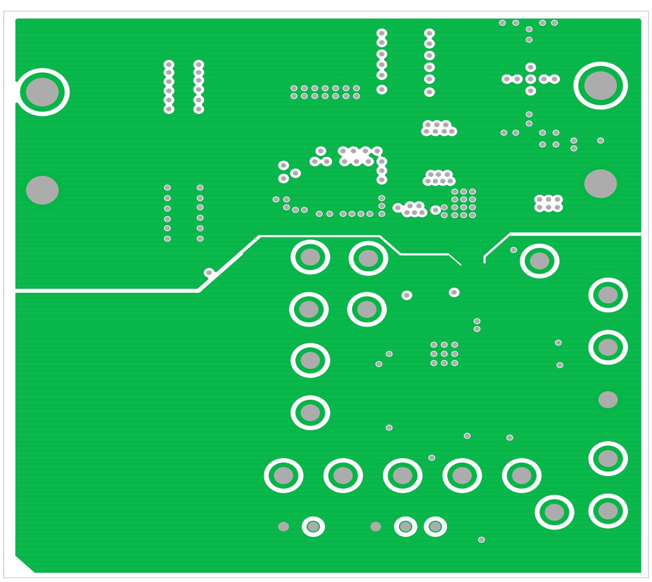

FIGURE 23. SECOND LAYER (SOLID GROUND)

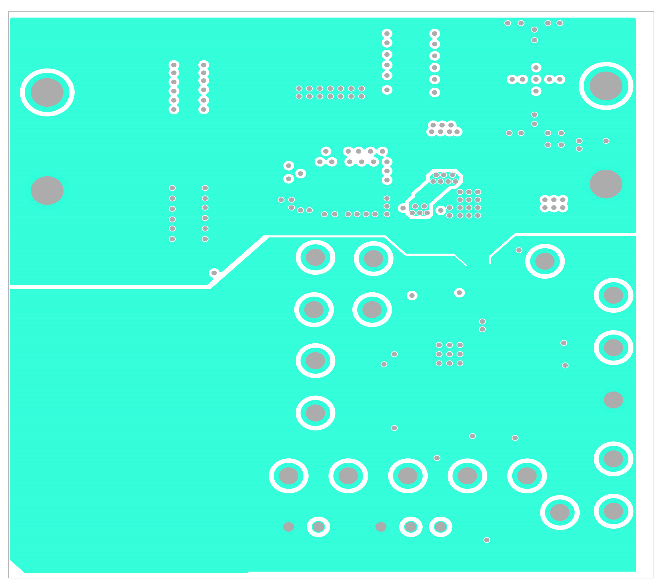

FIGURE 24. THIRD LAYER

ISL8117EVAL1Z PCB Layout (Continued)

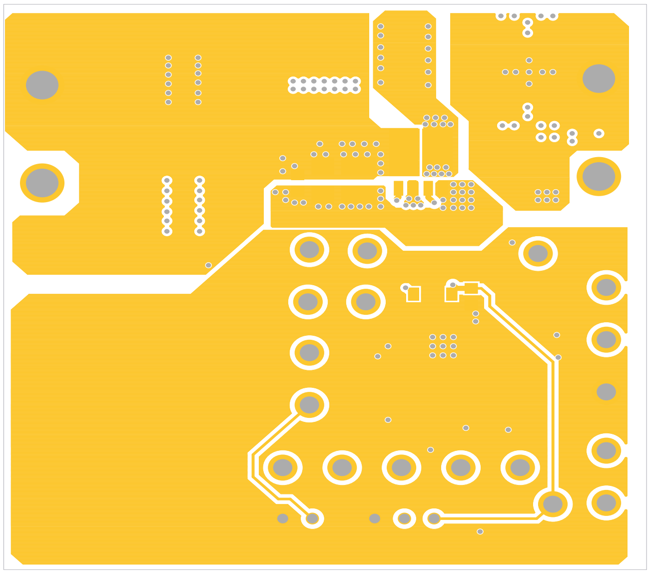

FIGURE 25. BOTTOM LAYER

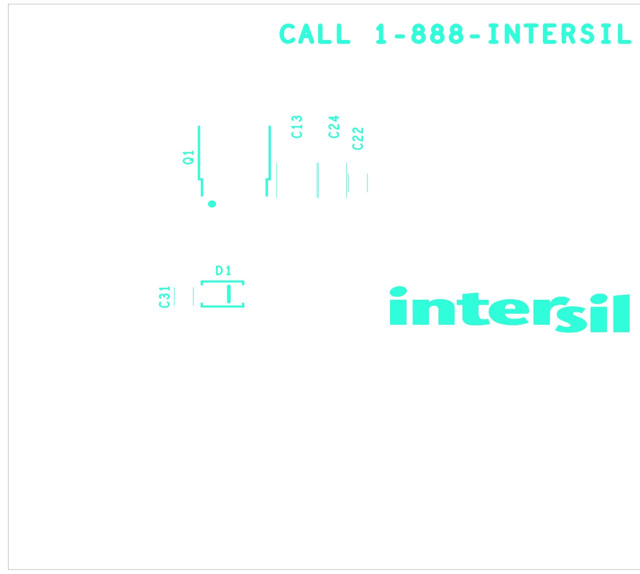

FIGURE 26. SILKSCREEN BOTTOM