

ISL80102, ISL80103 High Performance 2A and 3A LDOs Evaluation Board User Guide

Description

The ISL80102 and ISL80103 are high performance, low voltage, high current low dropout linear regulator specified at 2A and 3A, respectively. Rated for an input voltage from 2.2V to 6V, these LDOs can provide outputs from 0.8V to 5V on the adjustable version. The ISL80103EVAL2Z provides a simple platform to evaluate performance of the ISL80102, ISL80103.

The ISL80103EVAL2Z evaluation board comes with the adjustable output version of the IC. Jumpers are provided to set the desired output voltage. Fixed output versions are sampled in the accompanying kit.

The figures with operating conditions at 3A in this Application Note are applicable only to the ISL80103. All other information is applicable to both the ISL80102 and ISL80103.

What's Inside

The evaluation kit contains the following:

- The ISL80103EVAL2Z
- Fixed output versions of either the ISL80102 or the ISL80103
- The ISL80102, ISL80103 data sheet ([FN6660](#))
- This evaluation kit document

Required Equipment

The following equipment is recommended to perform the tests:

- 0V to 6V power supply capable of sourcing at least 5A
- Electronic load capable of sinking up to 5A
- Digital multimeters
- 200MHz oscilloscope

Test Procedure

- 1) Select the desired output voltage by shorting one of the jumpers from J1 through J6.
- 2) Ensure that output capacitor and Cpb are set according to recommended values shown in Table 1.
- 3) Place jumper JP1 in the 'enable' position. It is recommended to not leave the ENABLE pin floating.
- 4) Set the power supply for the desired input voltage and the load as desired and connect them to the input and output of the board, respectively.
- 5) Turn the power supply on and observe the output.

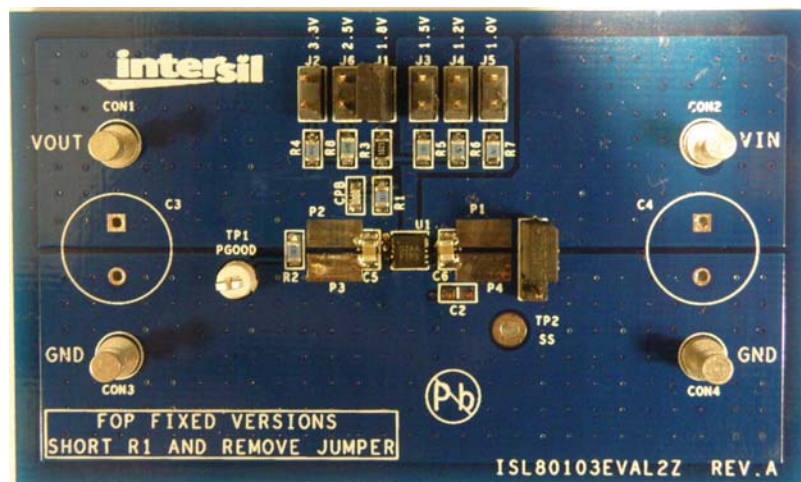


FIGURE 1. ISL80103EVAL2Z

Optimizing LDO Performance

Performance of the ISL80102, ISL80103 can be optimized by following these simple guidelines.

Phase Boost Capacitor (C_{PB})

On the adjustable version of the ISL80102, ISL80103, phase margin and crossover frequency can be increased by placing a small capacitor across the top resistor in the feedback resistor divider. C_{PB} and R_{TOP} as shown in Figure 2 place a zero at $F_z = 1/(2 \cdot \pi \cdot R_{TOP} \cdot C_{PB})$

The zero increases the crossover frequency of the LDO and provides additional phase resulting in faster load transient response.

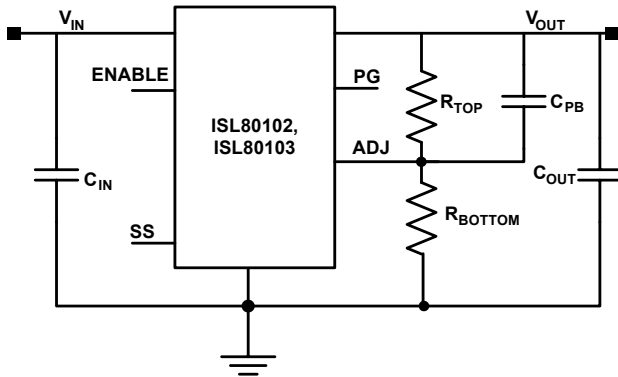


FIGURE 2. ISL80102, ISL80103 TYPICAL APPLICATION

Output Capacitor (C_{OUT})

Output capacitor selection is important to achieve the desired load transient performance. The ISL80102, ISL80103 uses state-of-the-art internal compensation to be compatible with different types of output capacitors, including multi-layer ceramic, POSCAP and aluminum/tantalum electrolytic.

There is a growing trend to use very-low ESR multi-layer ceramic capacitors (MLCC) for applications because they can support fast load transients and also bypass very high frequency noise from other sources. However, effective capacitance of MLCC's drops with applied voltage, age and temperature. X7R and X5R dielectric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within $\pm 20\%$ of nominal over full operating ratings of temperature and voltage.

Table 1 gives the recommended values for output capacitor (MLCC X5R/X7R) and C_{PB} for different voltage rails.

The right selection of output capacitor and C_{PB} also helps to provide better PSRR at high frequencies.

TABLE 1.

| V _{OUT} | R _{TOP} | R _{BOTTOM} | C _{PB} | C _{OUT} |
|------------------|------------------|---------------------|-----------------|------------------|
| 5.0V | 2.61kΩ | 287Ω | 47pF | 10μF |
| 3.3V | 2.61kΩ | 464Ω | 47pF | 10μF |
| 2.5V | 2.61kΩ | 649Ω | 47pF | 10μF |
| 1.8V* | 2.61kΩ | 1.0kΩ | 47pF | 10μF |
| 1.8V* | 2.61kΩ | 1.0kΩ | 82pF | 22μF |
| 1.5V | 2.61kΩ | 1.3kΩ | 82pF | 22μF |
| 1.2V | 2.61kΩ | 1.87kΩ | 150pF | 47μF |
| 1.0V | 2.61kΩ | 2.61kΩ | 150pF | 47μF |
| 0.8V | 2.61kΩ | 4.32kΩ | 150pF | 47μF |

NOTE: *Either option could be used depending on cost/performance requirements

Layout Guidelines

A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance. Parasitic inductance should be kept to a minimum. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The 'SENSE' trace in fixed voltage parts and the 'ADJ' trace in adjustable voltage parts must be away from noisy planes and traces.

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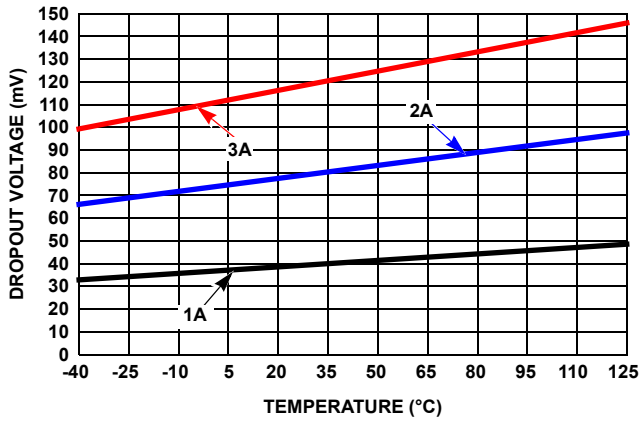


FIGURE 3. DROPOUT vs TEMPERATURE

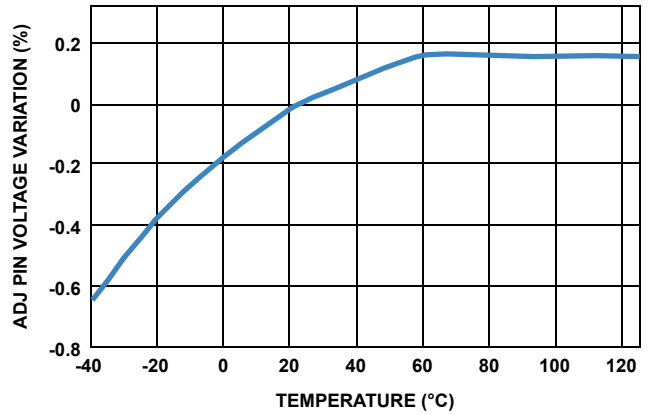


FIGURE 4. OUTPUT VOLTAGE vs TEMPERATURE

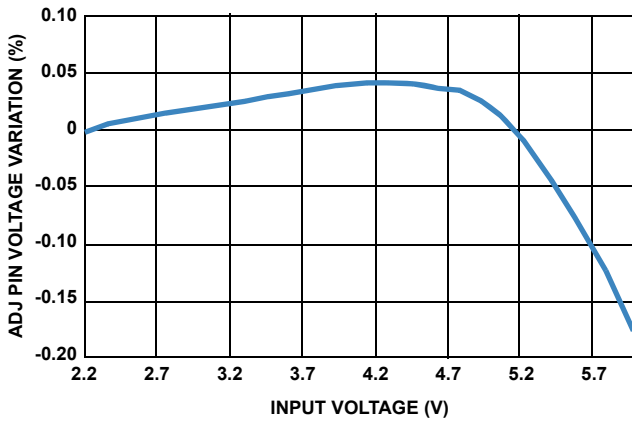


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE

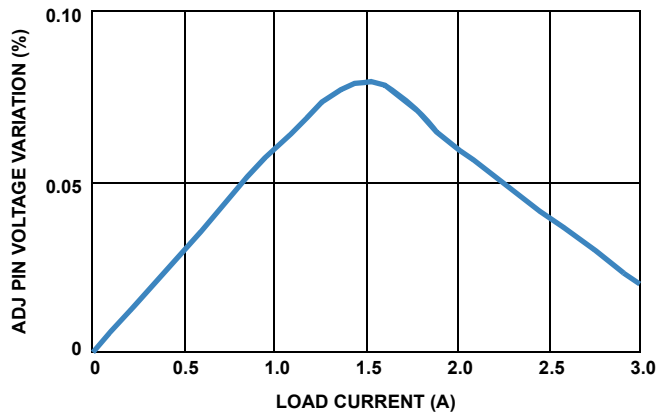


FIGURE 6. OUTPUT VOLTAGE vs LOAD CURRENT

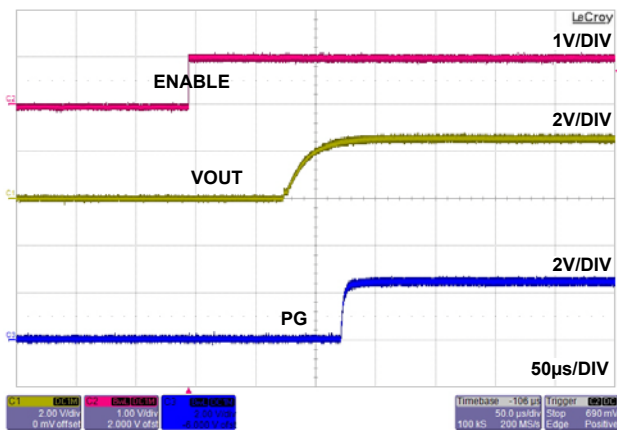


FIGURE 7. START-UP WAVEFORMS

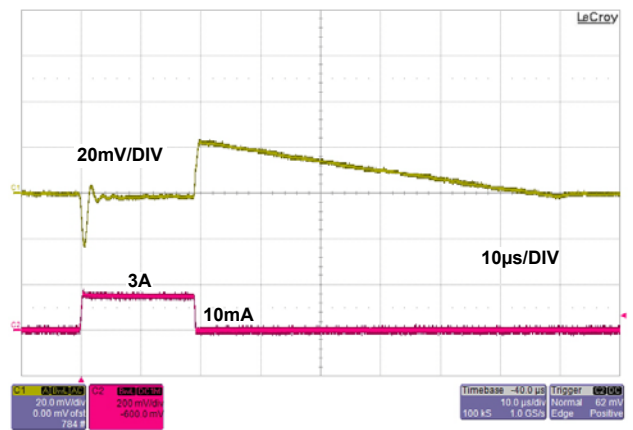


FIGURE 8. LOAD TRANSIENCE FOR $V_{OUT} = 1.0V$, $C_{OUT} = 47\mu F$, $C_{pb} = 150pF$

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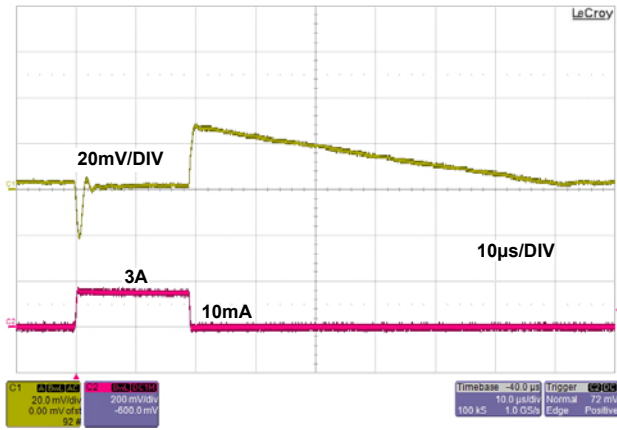


FIGURE 9. LOAD TRANSIENCE FOR $V_{OUT} = 1.2V$, $C_{OUT} = 47\mu F$, $C_{pb} = 150pF$

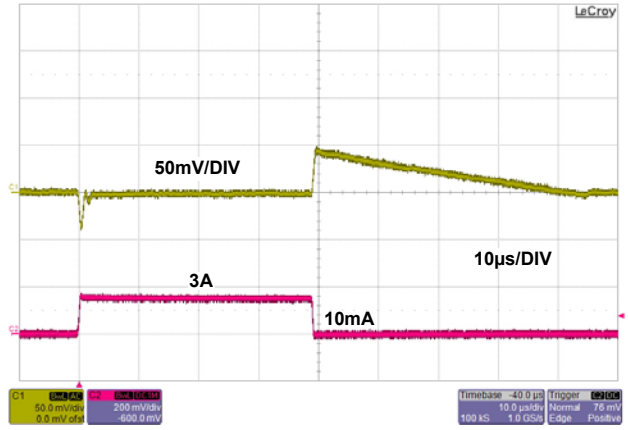


FIGURE 10. LOAD TRANSIENCE FOR $V_{OUT} = 1.5V$, $C_{OUT} = 22\mu F$, $C_{pb} = 82pF$

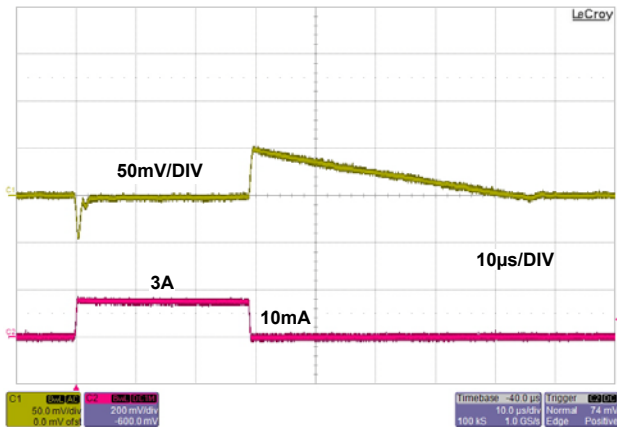


FIGURE 11. LOAD TRANSIENCE FOR $V_{OUT} = 1.8V$, $C_{OUT} = 22\mu F$, $C_{pb} = 82pF$

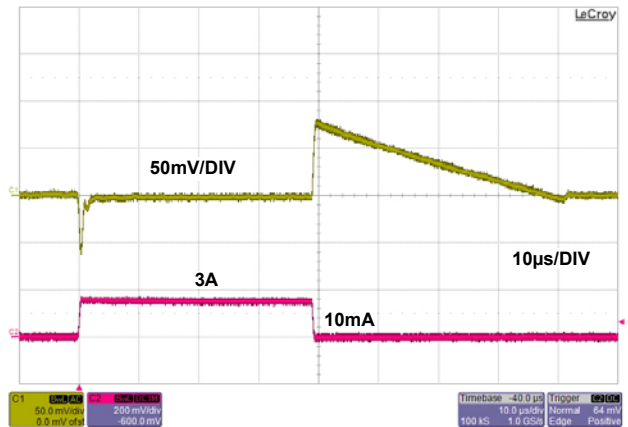


FIGURE 12. LOAD TRANSIENCE FOR $V_{OUT} = 1.8V$, $C_{OUT} = 10\mu F$, $C_{pb} = 47pF$

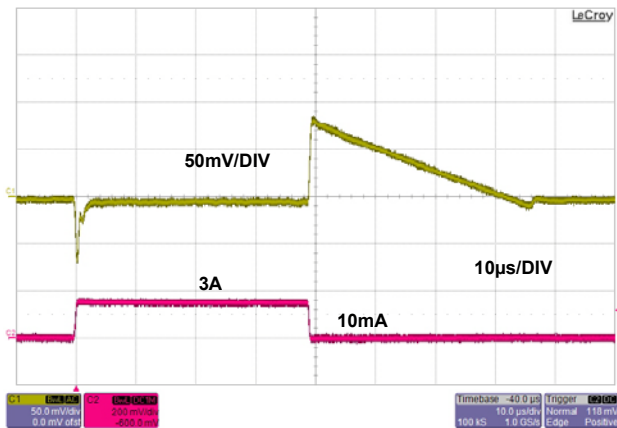


FIGURE 13. LOAD TRANSIENCE FOR $V_{OUT} = 2.5V$, $C_{OUT} = 10\mu F$, $C_{pb} = 47pF$

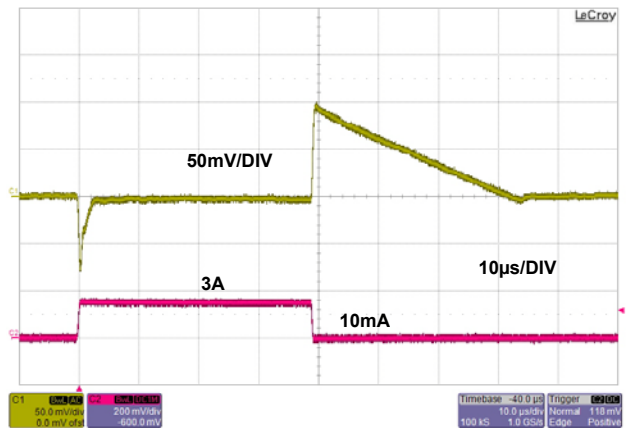


FIGURE 14. LOAD TRANSIENCE FOR $V_{OUT} = 3.3V$, $C_{OUT} = 10\mu F$, $C_{pb} = 47pF$

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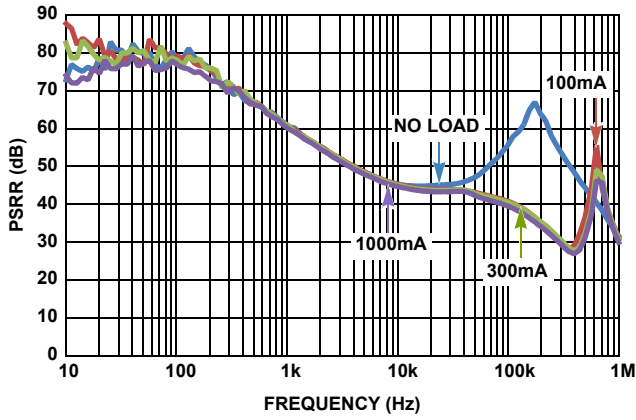


FIGURE 15. PSRR FOR $V_{OUT} = 1.0V$, $C_{OUT} = 47\mu F$, $C_{pb} = 150pF$

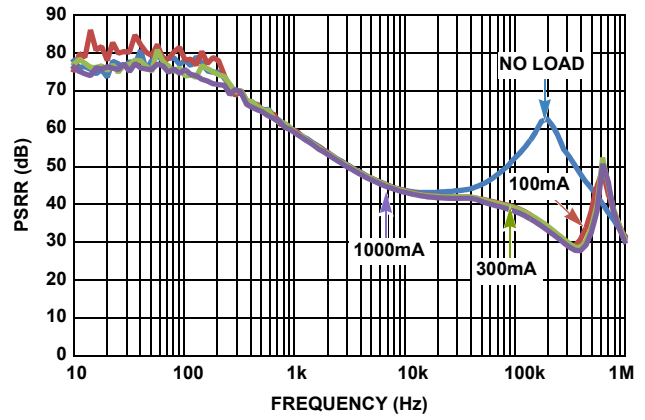


FIGURE 16. PSRR FOR $V_{OUT} = 1.2V$, $C_{OUT} = 47\mu F$, $C_{pb} = 150pF$

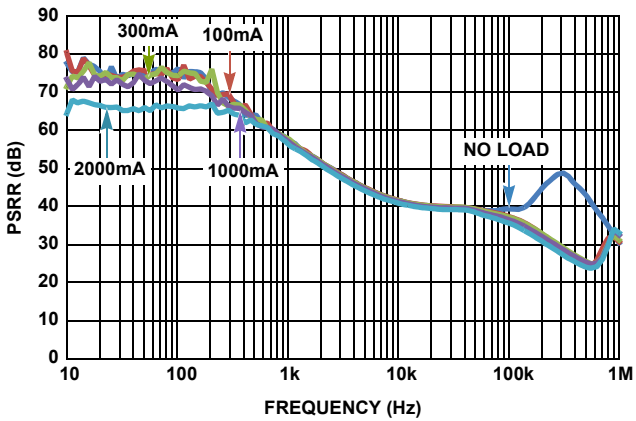


FIGURE 17. PSRR FOR $V_{OUT} = 1.5V$, $C_{OUT} = 22\mu F$, $C_{pb} = 82pF$

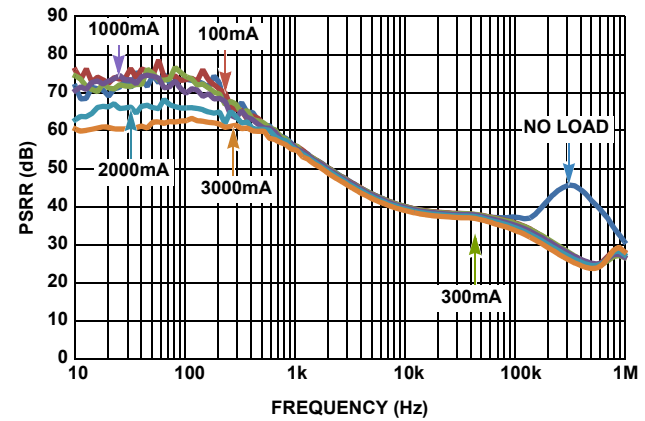


FIGURE 18. PSRR FOR $V_{OUT} = 1.8V$, $C_{OUT} = 22\mu F$, $C_{pb} = 82pF$

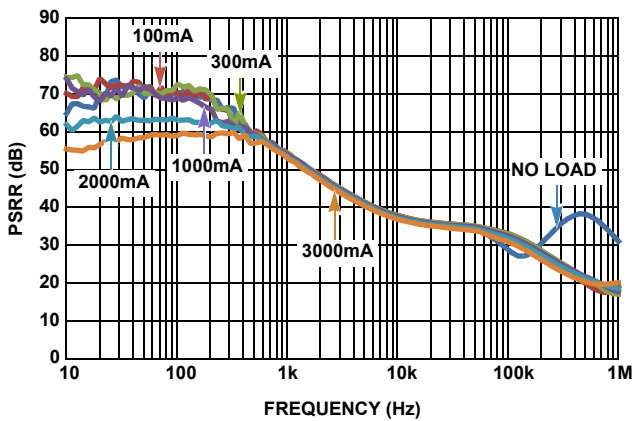


FIGURE 19. PSRR FOR $V_{OUT} = 2.5V$, $C_{OUT} = 10\mu F$, $C_{pb} = 47pF$

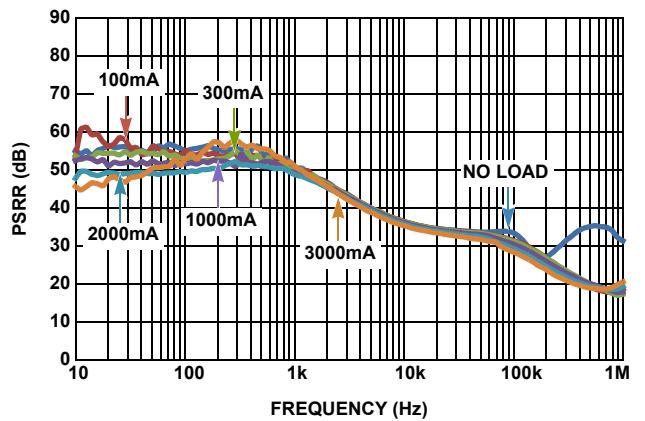


FIGURE 20. PSRR FOR $V_{OUT} = 3.3V$, $C_{OUT} = 10\mu F$, $C_{pb} = 47pF$

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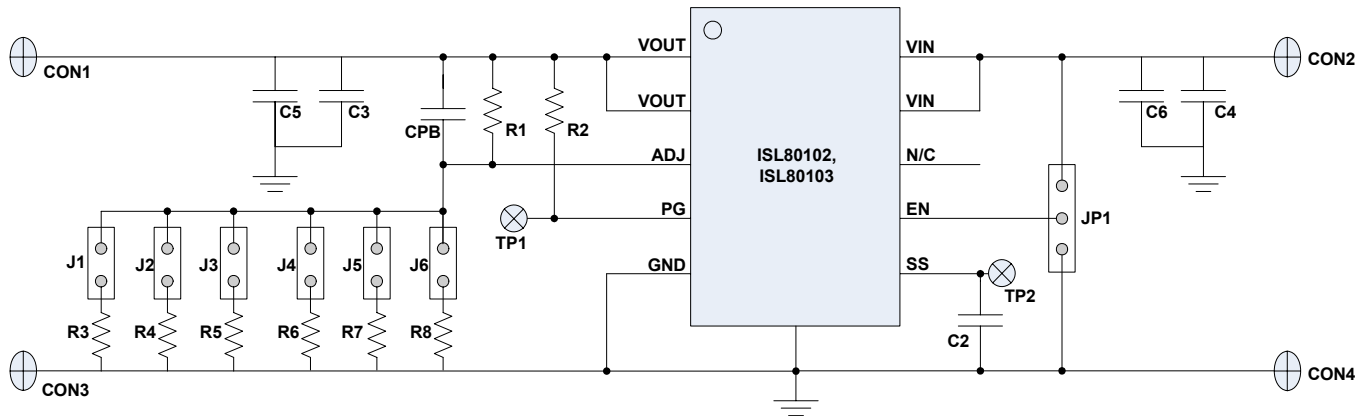


TABLE 2. BILL OF MATERIALS

| ITEM | QTY | REFERENCE DESIGNATOR | VALUE | DESCRIPTION | MANUFACTURER | PART NUMBER |
|------|-----|------------------------|----------------|--------------------------------|--------------|--------------------------------|
| 1 | 2 | C5, C6 | 10 μ F | CAP, SMD, 0805, 16V, 10%, | Generic | |
| 2 | 1 | CPB | 47pF | CAP, SMD, 0603 | Generic | |
| 3 | 1 | U1 | | ISL80102IRAJZ or ISL80103IRAJZ | Intersil | ISL80102IRAJZ or ISL80103IRAJZ |
| 4 | 1 | R1 | 2.61k Ω | RES, SMD, 0603, 1% | Generic | |
| 5 | 1 | R2 | 100k Ω | RES, SMD, 0603, 1% | Generic | |
| 6 | 1 | R3 | 1k Ω | RES, SMD, 0603, 1% | Generic | |
| 7 | 1 | R4 | 464 Ω | RES, SMD, 0603, 1% | Generic | |
| 8 | 1 | R5 | 1.3k Ω | RES, SMD, 0603, 1% | Generic | |
| 9 | 1 | R6 | 1.87k Ω | RES, SMD, 0603, 1% | Generic | |
| 10 | 1 | R7 | 2.61k Ω | RES, SMD, 0603, 1% | Generic | |
| 11 | 1 | R8 | 649 Ω | RES, SMD, 0603, 1% | Generic | |
| 12 | 1 | JP1 | | Jumper | Generic | |
| 13 | 6 | J1, J2, J3, J4, J5, J6 | | Jumper | Generic | |
| 14 | 1 | TP1 | | Test Point | Keystone | 5007 |
| 15 | 4 | CON1, CON2, CON3, CON4 | | Terminal Connector | Keystone | 1514-2 |
| | | C2, C3, C4, TP2 | | DNP | | |

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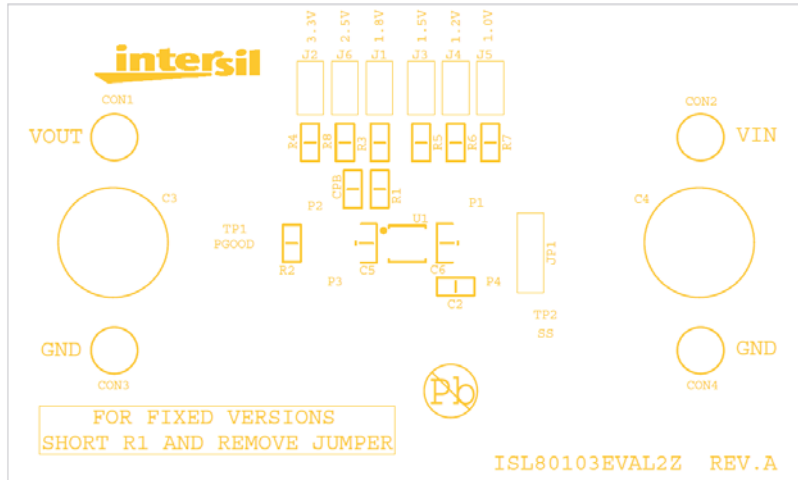


FIGURE 21. ISL80103EVAL2Z COMPONENT PLACEMENT

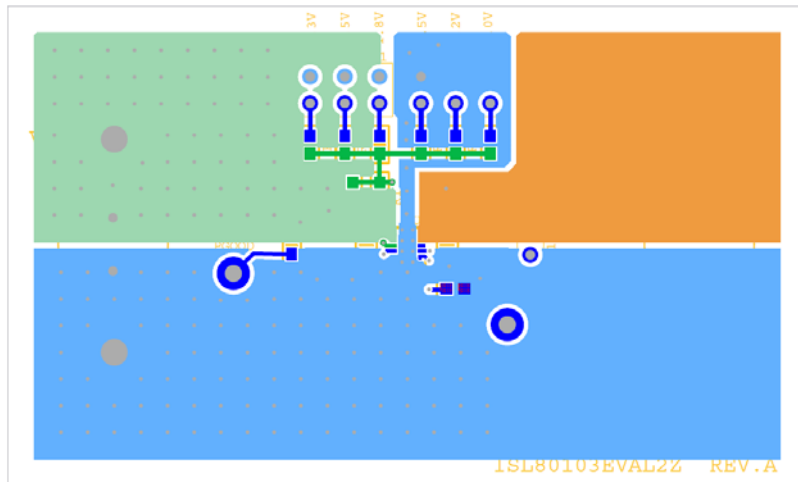


FIGURE 22. ISL80103EVAL2Z TOP LAYER

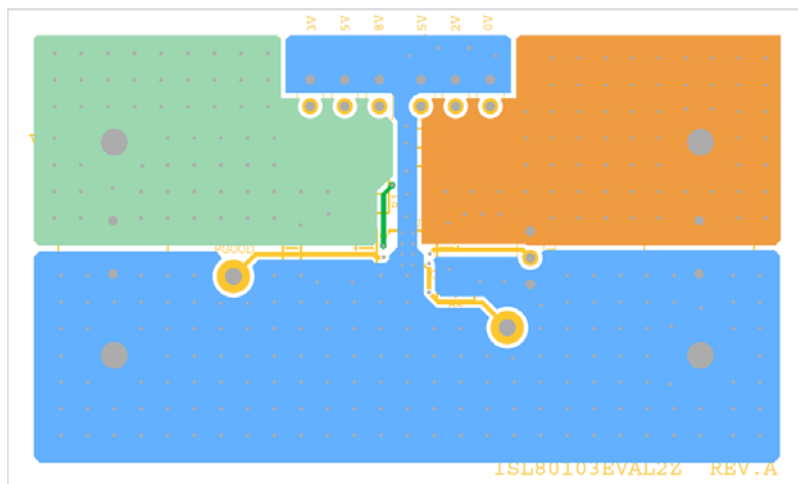


FIGURE 23. ISL80103EVAL2Z BOTTOM LAYER

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