IS61WV12824

128K x 24 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

AUGUST 2017

FEATURES

- High-speed access time: 8, 10 ns
- High-performance, low-power CMOS process
- TTL compatible interface levels
- Single power supply
  VDD 3.3V ± 5% for 8ns
  VDD 2.4V to 3.6V for 10ns
- Fully static operation: no clock or refresh required
- Three state outputs
- Available in 119-pin Ball Grid Array (BGA) and 100-pin QFP packages.
- Industrial temperature available
- Lead-free available

DESCRIPTION

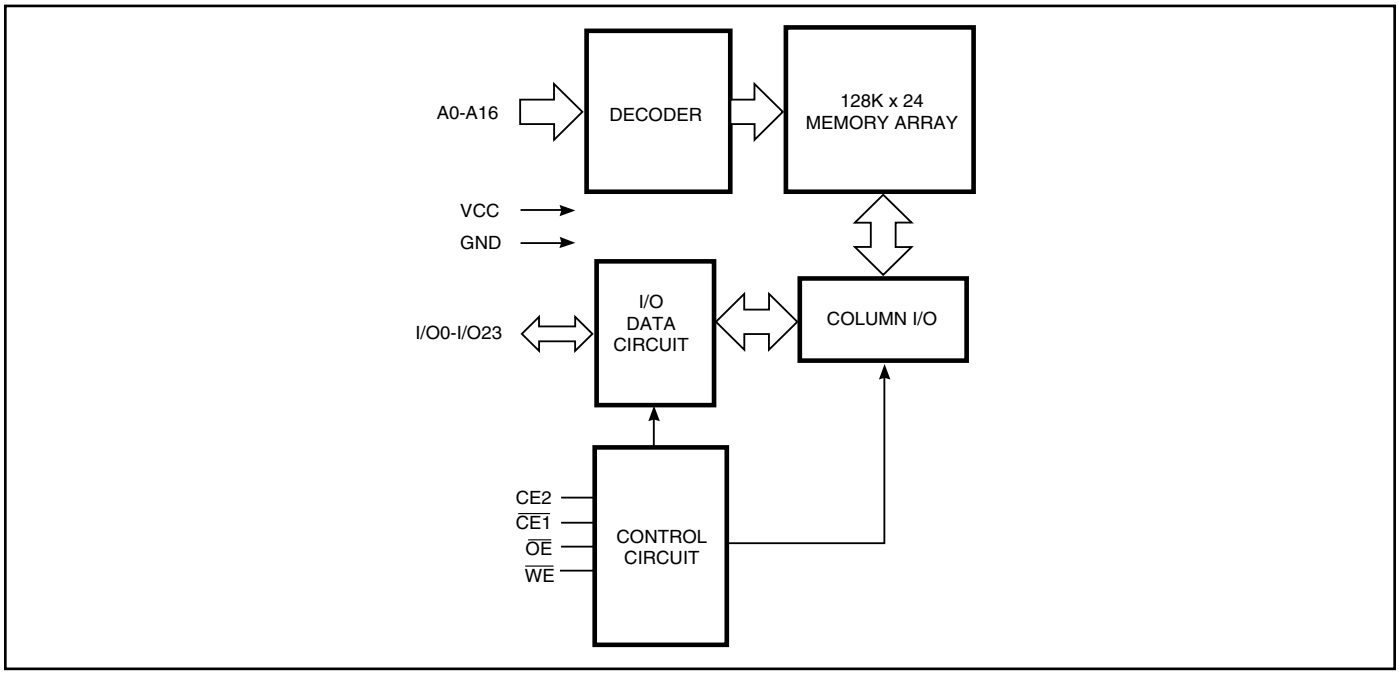
The *ISSI* IS61WV12824 is a high-speed, static RAM organized as 131,072 words by 24 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When $\overline{CE1}$ is HIGH and CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE1}$, CE2 and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61WV12824 is packaged in the JEDEC standard 119-pin BGA and 100-pin QFP.

FUNCTIONAL BLOCK DIAGRAM



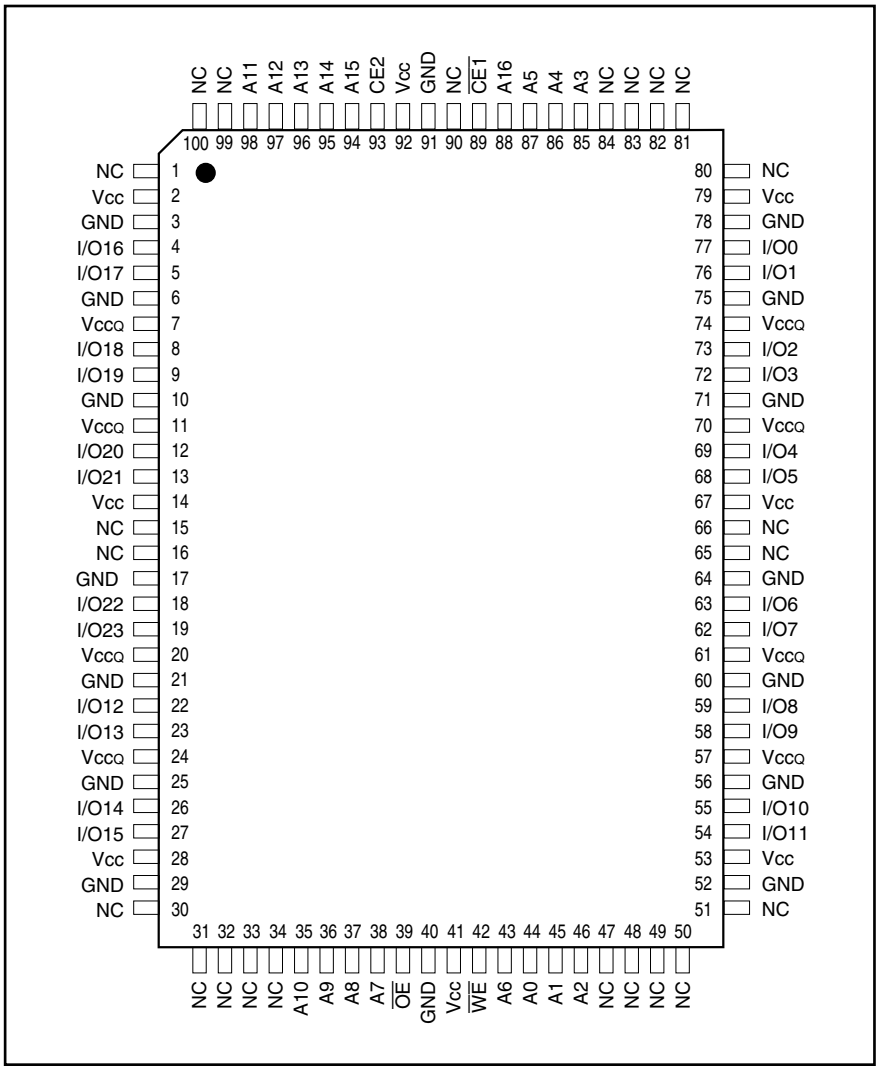
PIN CONFIGURATION - 119-pin BGA

	1	2	3	4	5	6	7
A	NC	A11	A14	A15	A16	A4	NC
B	NC	A12	A13	$\overline{CE1}$	A5	A3	NC
C	I/O16	NC	CE2	NC	NC	NC	I/O0
D	I/O17	Vcc	GND	GND	GND	Vcc	I/O1
E	I/O18	GND	Vcc	GND	Vcc	GND	I/O2
F	I/O19	Vcc	GND	GND	GND	Vcc	I/O3
G	I/O20	GND	Vcc	GND	Vcc	GND	I/O4
H	I/O21	Vcc	GND	GND	GND	Vcc	I/O5
J	Vcc	GND	Vcc	GND	Vcc	GND	Vcc
K	I/O22	Vcc	GND	GND	GND	Vcc	I/O6
L	I/O23	GND	Vcc	GND	Vcc	GND	I/O7
M	I/O12	Vcc	GND	GND	GND	Vcc	I/O8
N	I/O13	GND	Vcc	GND	Vcc	GND	I/O9
P	I/O14	Vcc	GND	GND	GND	Vcc	I/O10
R	I/O15	NC	NC	NC	NC	NC	I/O11
T	NC	A10	A8	$\overline{WE}$	A0	A1	NC
U	NC	A9	A7	$\overline{OE}$	A6	A2	NC

PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O23	Data Inputs/Outputs
$\overline{CE1}$	Chip Enable Input LOW
CE2	Chip Enable Input HIGH
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
NC	No Connection
Vcc	Power
GND	Ground

PIN CONFIGURATION
100-Pin QFP



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$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
NC	No Connection
Vcc	Power
VccQ	I/O Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O0-I/O23	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X		
Output Disabled	H	L	H	H	High-Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter		Value	Unit
V_{CC}	Power Supply Voltage Relative to GND		–0.5 to 5.0	V
V_{TERM}	Terminal Voltage with Respect to GND		–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to + 150	°C
T_{BIAS}	Temperature Under Bias:	Com.	–10 to + 85	°C
		Ind.	–45 to + 90	°C
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current		±20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc (8 ns)	Vcc (10 ns)
Commercial	0°C to +70°C	3.3V ± 5%	2.4V ~ 3.6V
Industrial	–40°C to +85°C	3.3V ± 5%	2.4V ~ 3.6V

Note:
1. When operated in the range of 2.4V~3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–2	2	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–2	2	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 ns Min.	-8 ns Max.	-10 ns Min.	-10 ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	110	—	90	mA
			Ind.	—	115	—	95	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, f = max. $\overline{CE1} \geq V_{IH}$, CE2 ≤ V_{IL}	Com.	—	30	—	30	mA
			Ind.	—	35	—	35	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1} \geq V_{CC}$ – 0.2V, CE2 ≤ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	20	—	20	mA
			Ind.	—	25	—	25	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)	Unit (3.3V ± 5%)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	V_{DD}/2	V_{DD}/2 + 0.05
Output Load	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

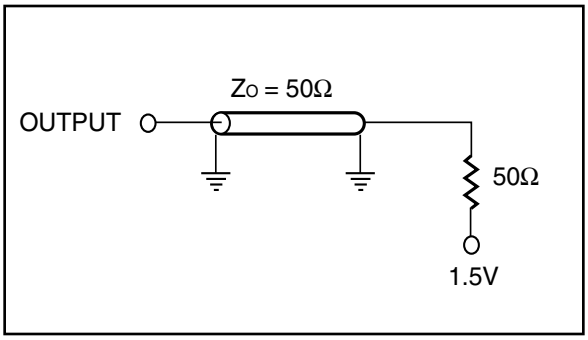


Figure 1

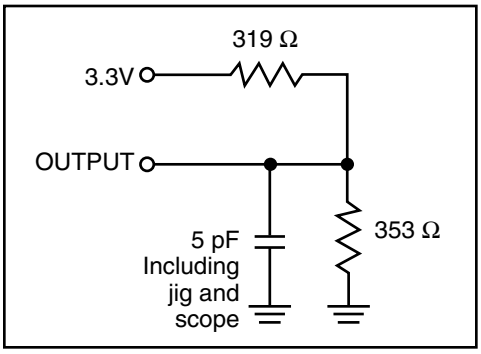


Figure 2

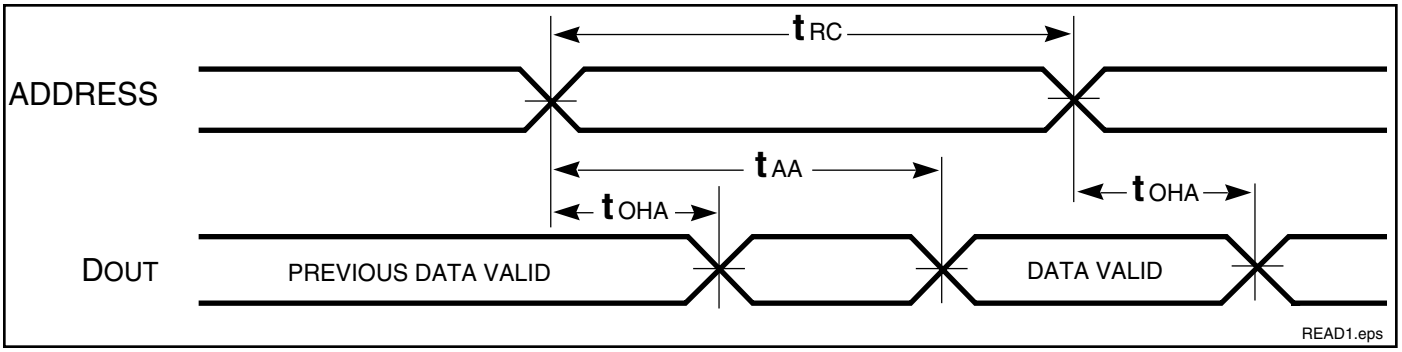
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2.5	—	2.5	—	ns
t_{ACE}	$\overline{CE1}$ Access Time	8	—	—	10	ns
t_{ACE2}	CE2 Access Time					
t_{DOE}	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	3	0	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE1}$ to High-Z Output	0	3	0	4	ns
t_{HZCE2}[2]	CE2 to High-Z Output					
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{LZCE2}[2]	CE2 to Low-Z Output					

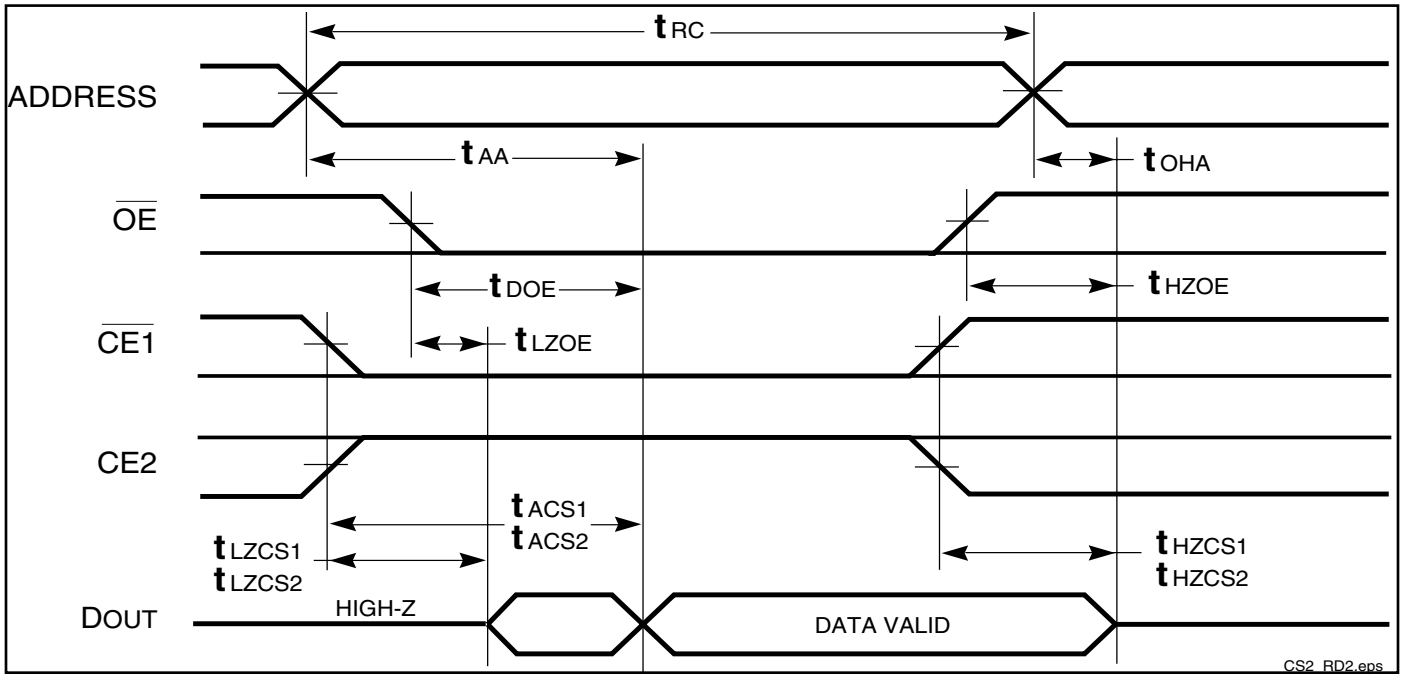
Notes:
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}; CE2 = V_{IH})



READ CYCLE NO. 2[1,3]



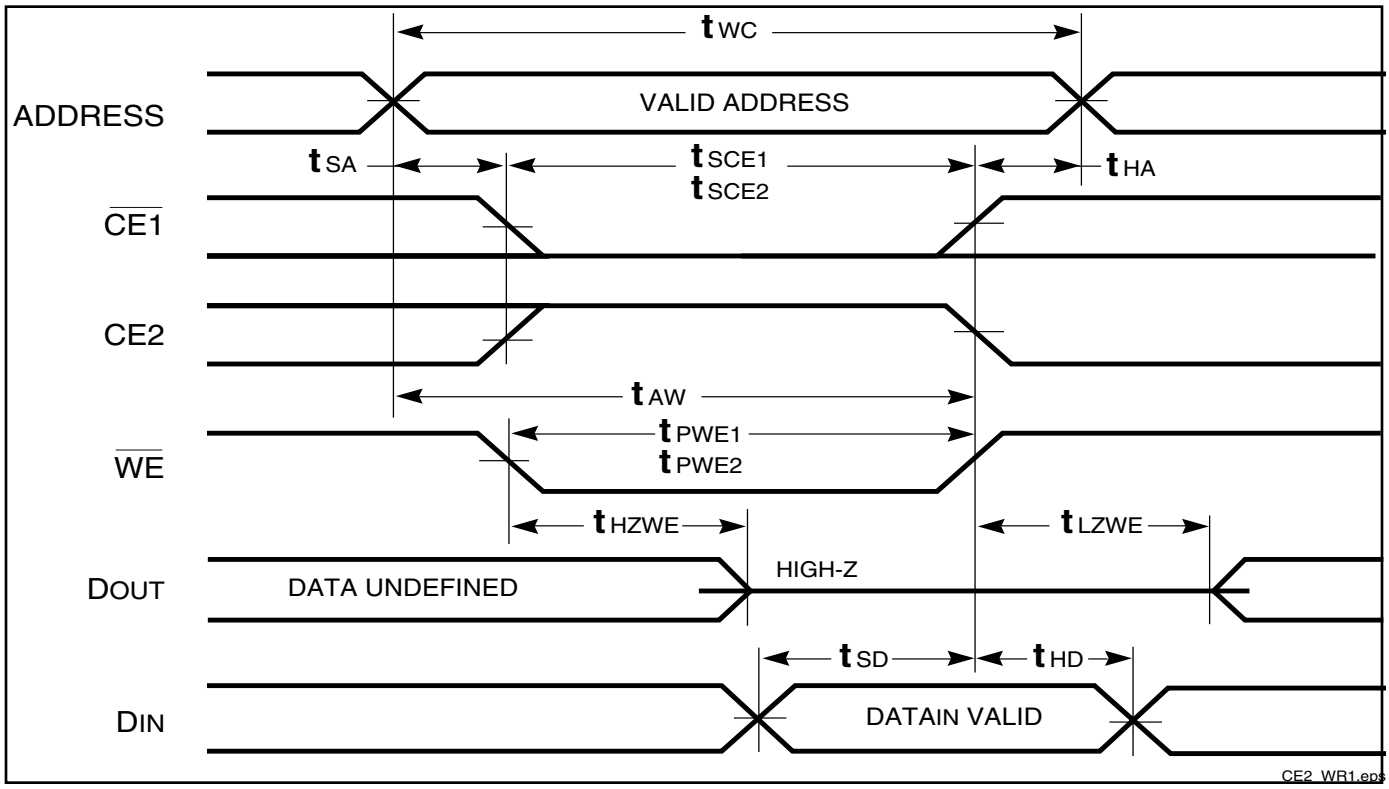
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}. CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

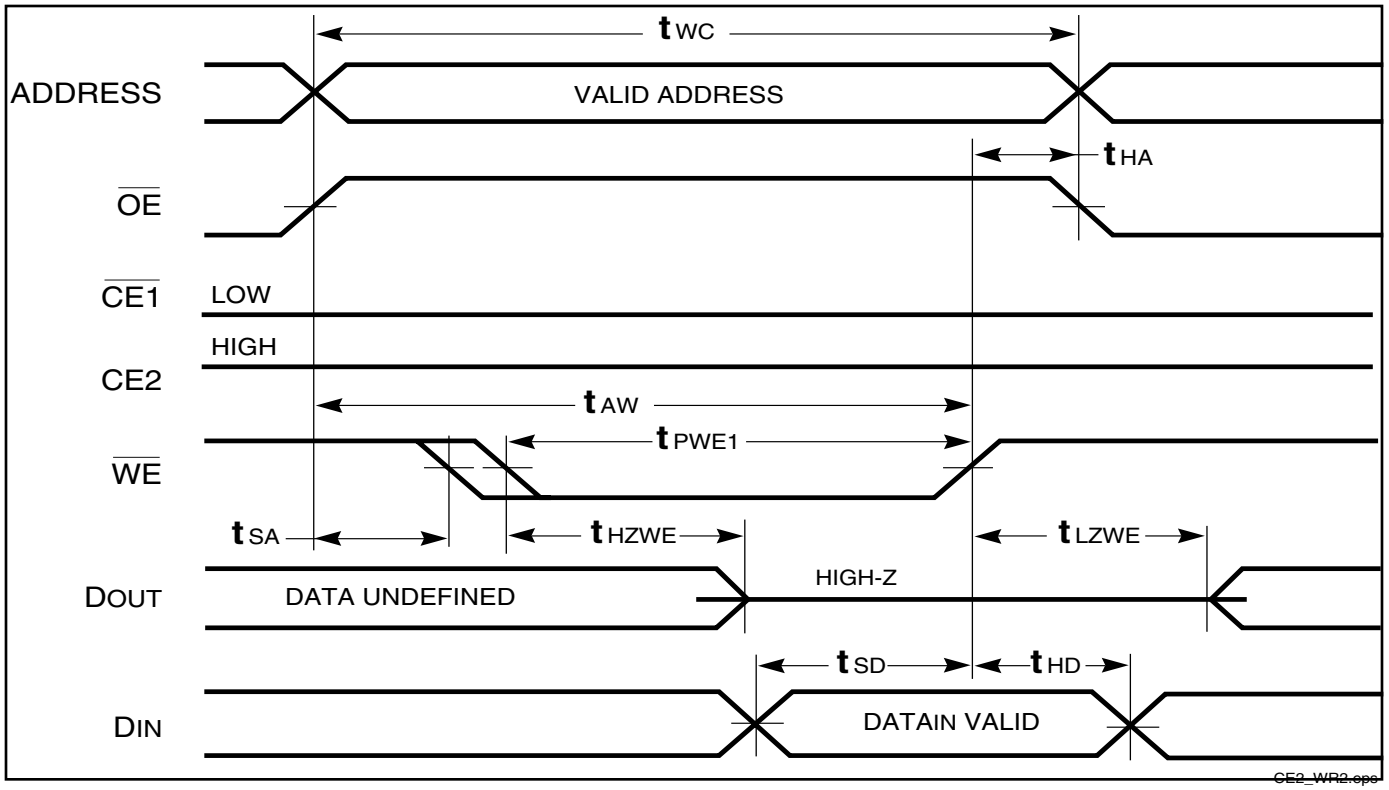
		-8		-10		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE1}$ to Write End	6.5	—	8	—	ns
t_{SCE2}	CE2 to Write End	6.5	—	8	—	
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	6.5	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0.4v to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

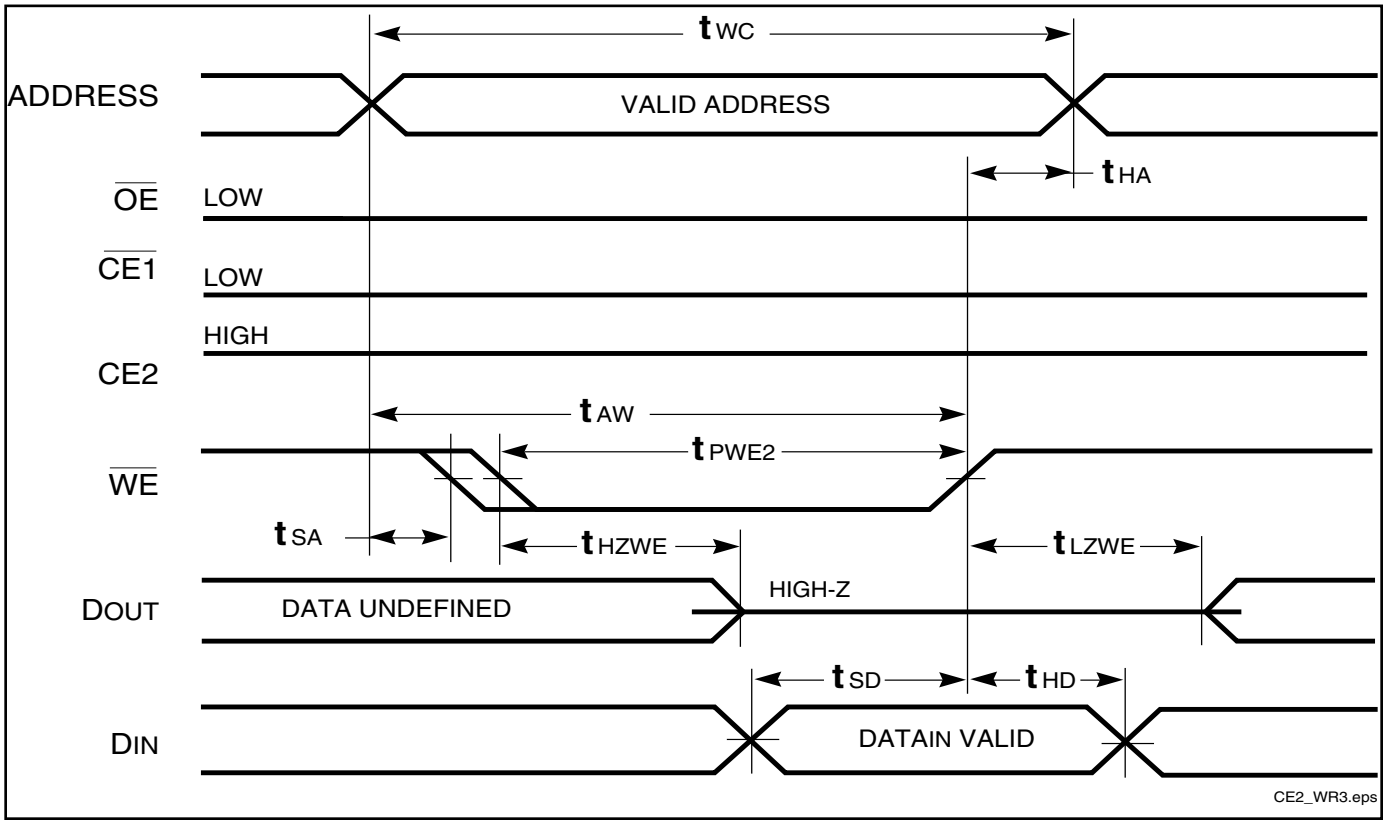
WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled: $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3[1] ($\overline{WE}$ Controlled: $\overline{OE}$ IS LOW DURING WRITE CYLE)



Note:

1. The internal Write time is defined by the overlap of $\overline{CE1}$ = LOW, CE2 = HIGH and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

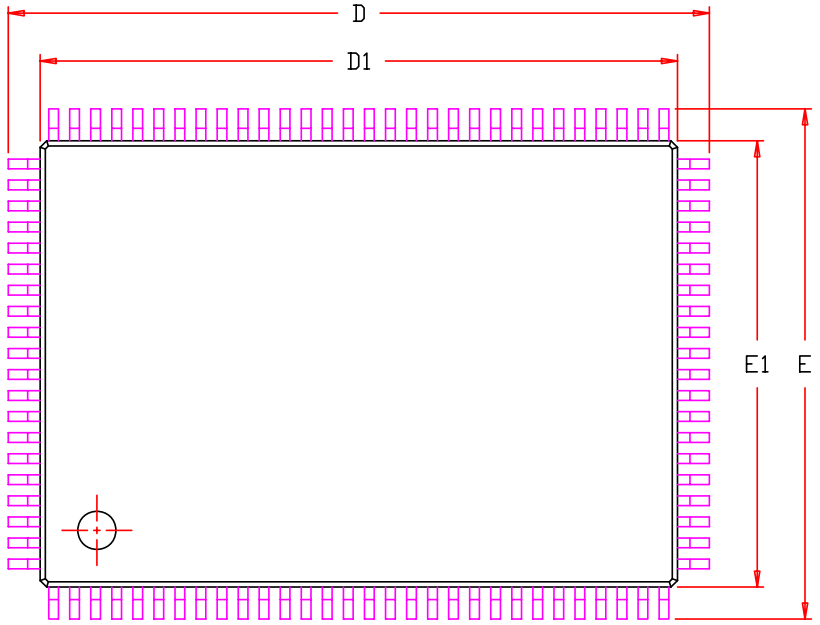
ORDERING INFORMATION

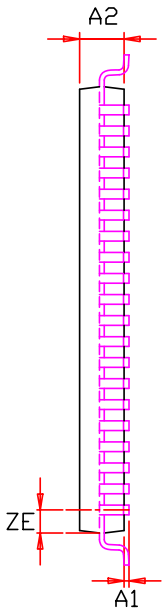
Commercial Range: 0°C to +70°C

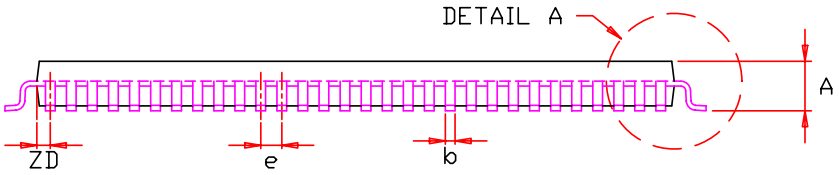
Speed (ns)	Order Part No.	Package
8	IS61WV12824-8B	Ball Grid Array
	IS61WV12824-8BL	Ball Grid Array, Lead-free
	IS61WV12824-8TQL	QFP, Lead-free
10	IS61WV12824-10B	Ball Grid Array
	IS61WV12824-10BL	Ball Grid Array, Lead-free
	IS61WV12824-10TQL	QFP, Lead-free

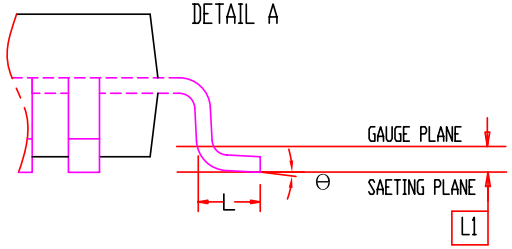
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
8	IS61WV12824-8BI	Ball Grid Array
10	IS61WV12824-10BI	Ball Grid Array
	IS61WV12824-10TQLI	QFP, Lead-free









SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40		1.60	0.055		0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.30	0.38	0.009	0.012	0.015
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.65 BSC.			0.026 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	0.25 BSC.			0.010 BSC.		
ZD	0.575 REF.			0.023 REF.		
ZE	0.825 REF.			0.032 REF.		
θ	0	3.5°	7°	0	3.5°	7°

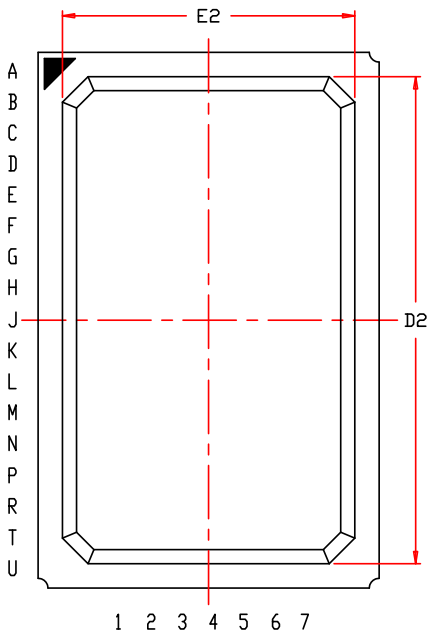
NOTE :

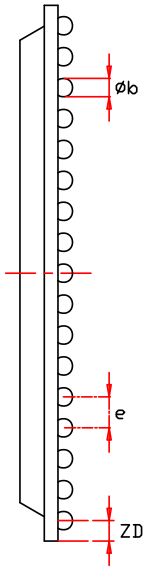
1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

ISSI	TITLE	100L 14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline	REV.	F	DATE	09/01/2009

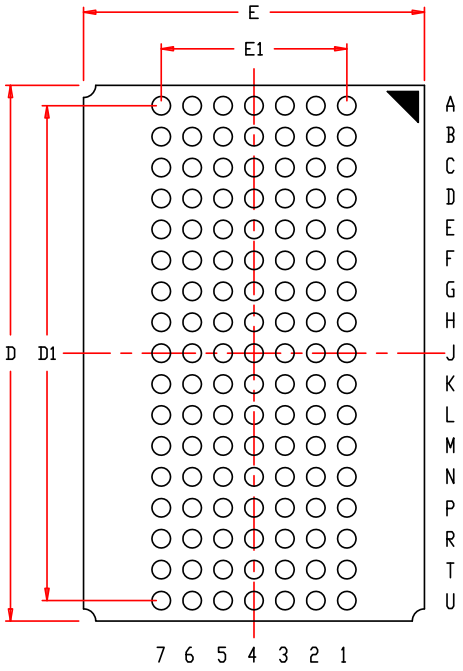
280-600-011 REV. A

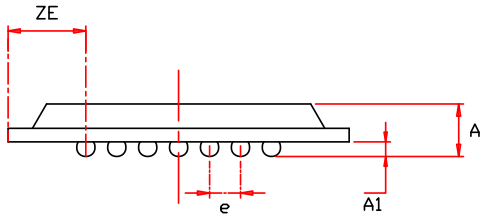
TOP VIEW





BOTTOM VIEW





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	2.15	3.50	-	0.085	0.138
A1	0.50	0.60	0.70	0.020	0.024	0.028
øb	0.66	0.76	0.86	0.026	0.030	0.034
D	21.80	22.00	22.20	0.858	0.866	0.874
D1	20.32 BSC.			0.800 BSC.		
D2	19.40	19.50	19.60	0.764	0.768	0.772
E	13.80	14.00	14.20	0.543	0.551	0.559
E1	7.62 BSC.			0.300 BSC.		
E2	11.90	12.00	12.10	0.468	0.472	0.476
e	1.27 BSC.			0.050 BSC.		
ZD	0.84 REF.			0.033 REF.		
ZE	3.19 REF.			0.126 REF.		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MS-028

ISSI	TITLE	119L 14x22mm PBGA Package Outline	REV.	E	DATE	10/13/2010