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Datasheet

S128 Microcontroller

Datasheet

Renesas Synergy™ Platform

Renesas Synergy™ Microcontrollers

S1 Series

The integrated module for Digital Addressable Lighting Interface (DALI) communications is designed for compliance to IEC 62386 version 2 (DALI 2) when used with suitable software and hardware.

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Rev.1.00 Mar 2017

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(Rev.3.0-1 November 2016)

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Ultra low power 32-MHz ARM® Cortex®-M0+ microcontroller, up to 256-KB code flash memory, 24-KB SRAM, Digital Addressable Lighting Interface, Capacitive Touch Sensing Unit, 14-bit A/D Converter, 8-bit D/A Converter, security and safety features.

Features

■ ARM® Cortex®-M0+ Core
- ARM®v6-M architecture
- Maximum operating frequency: 32 MHz
- ARM® Memory Protection Unit (MPU) with 8 regions
- Debug and Trace: DWT, BPU, CoreSight™ MTB-M0+
- CoreSight Debug Port: SW-DP

■ Memory
- Up to 256-KB code flash memory
- 4-KB data flash memory (up to 100,000 erase/write cycles)
- Up to 24-KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- CAN module (CAN)
- Digital Addressable Lighting Interface (DALI)

■ Analog
- 14-Bit A/D Converter (ADC14)
- 8-Bit D/A Converter (DAC8) × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-Bit (GPT32)
- General PWM Timer 16-Bit High Resolution (GPT16H) × 3
- General PWM Timer 16-Bit (GPT16) × 3
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- ECC in SRAM
- SRAM Parity Error Check
- Flash Area Protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) Calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO Readback Level Detection
- Register Write Protection
- Main Oscillator Stop Detection
- Illegal memory access

■ System and Power Management
- Low-power modes
- RealTime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection with voltage settings

■ Security and Encryption
- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Independent watchdog timer OCO (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 53 input/output pins
  - Up to 3 CMOS input
  - Up to 50 CMOS input/output
    - Up to 5 5-V tolerant input/output (when VCC = 3.6 V)
    - Up to 2 pins high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = –40°C to +85°C
  - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
- Ta = –40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

1. Overview

The S128 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

Based on the energy-efficient ARM Cortex®-M0+ 32-bit core, this MCU is particularly suited for cost-sensitive and low-power applications. The MCU in this series has the following features:

- Up to 256 KB code flash memory
- 24-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8)
- Security features.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M0+	• Maximum operating frequency: up to 32 MHz • ARM Cortex-M0+ - Revision: r0p1-00rel0 - ARMv6-M architecture profile - Single-cycle integer multiplier. • ARM Memory Protection Unit (MPU) - ARMv6 Protected Memory System Architecture - 8 protection regions. • SysTick timer - Driven by LOCO clock.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB code flash memory. See section 42, Flash Memory in User's Manual.
Data flash memory	4 KB data flash memory. See section 42, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 41, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes in User's Manual.

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	13 types of resets: • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • CPU stack pointer error reset • Software reset. See section 5, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual.
Clock	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • Independent watchdog timer on-chip oscillator • Clock out support. See section 8, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy measurement circuit (CAC) checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 9, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls NMI interrupts. See section 12, Interrupt Controller Unit (ICU) in User's Manual.
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 18, Key Interrupt Function (KINT) in User's Manual.
Low Power Mode	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes in User's Manual.
Register Write Protection	The register write protection function protects important registers from being overwritten due to software errors. See section 11, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four MPUs and a CPU stack pointer monitor function are provided for memory protection. See section 14, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 24, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 16, Event Link Controller in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 15, Data Transfer Controller (DTC) in User's Manual.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 1 channel and a 16-bit timer with 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 20, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 19, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 22, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC) in User's Manual.

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI) in User's Manual.
Digital Addressable Lighting Interface (DALI)	A Digital Addressable Lighting Interface (DALI) module is provided. DALI is an international open lighting control communication protocol that includes dimming control of electronic ballasts and LED lights from different manufacturers. The DALI interface module is designed to allow compliance with international standard IEC62386-101 Edition 1.0/2.0 (DALI 2), that includes software control. See section 28, Digital Addressable Lighting Interface (DALI) in User's Manual.

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
I²C Bus interface (IIC)	A 2-channel IIC module conforms with and provides a subset of the NXP I²C bus (Inter-Integrated Circuit bus) interface functions. See section 29, I²C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI) in User's Manual.
CAN Module (CAN)	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) in User's Manual.
USB 2.0 Full-Speed Module (USBFS)	The USBFS is a USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 5 pipes. PIPE0 and PIPE4 to PIPE7 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging Specification. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply at 3.3 V. See section 26, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 21 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 33, 14-Bit A/D Converter (ADC14) in User's Manual.
8-bit D/A Converter (DAC8)	An 8-bit D/A converter (DAC8) is provided. See section 34, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC for conversion and can be further used by the end application. See section 35, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The analog comparator compares a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 37, High-Speed Analog Comparator (ACMPHS) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The analog comparator compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin, an output from internal D/A converter, or from the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 38, Low-Power Analog Comparator (ACMPLP) in User's Manual.
Operational Amplifier (OPAMP)	The operational amplifier amplifies small analog input voltages and outputs the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 36, Operational Amplifier (OPAMP) in User's Manual.

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode. See section 39, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) Calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 40, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
AES Engine	See section 43, AES Engine in User's Manual
True Random Number Generator (TRNG)	See section 44, True Random Number Generator (TRNG) in User's Manual

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group may have a subset of the features.

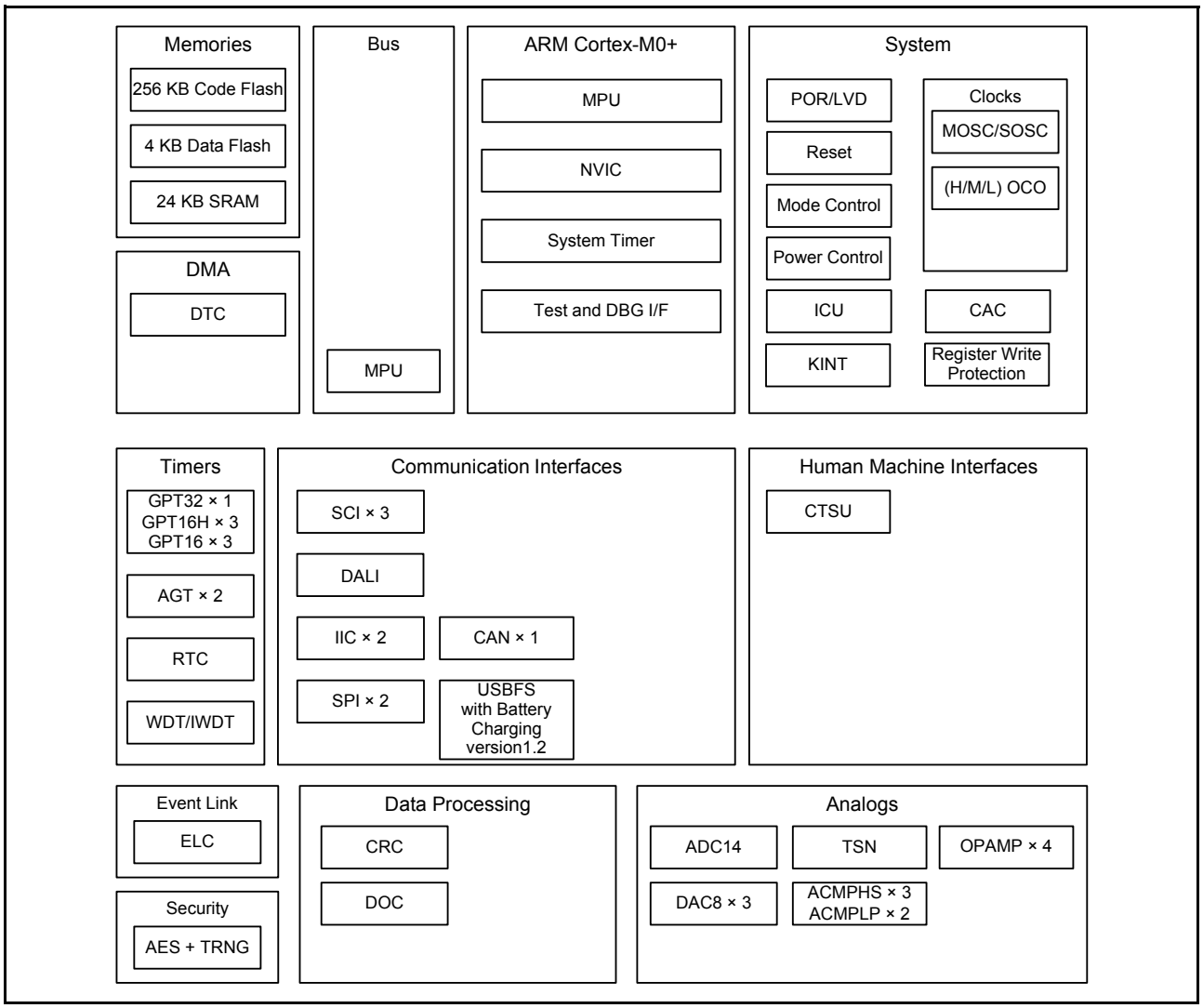

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity, and package type. Table 1.12 shows a product list.

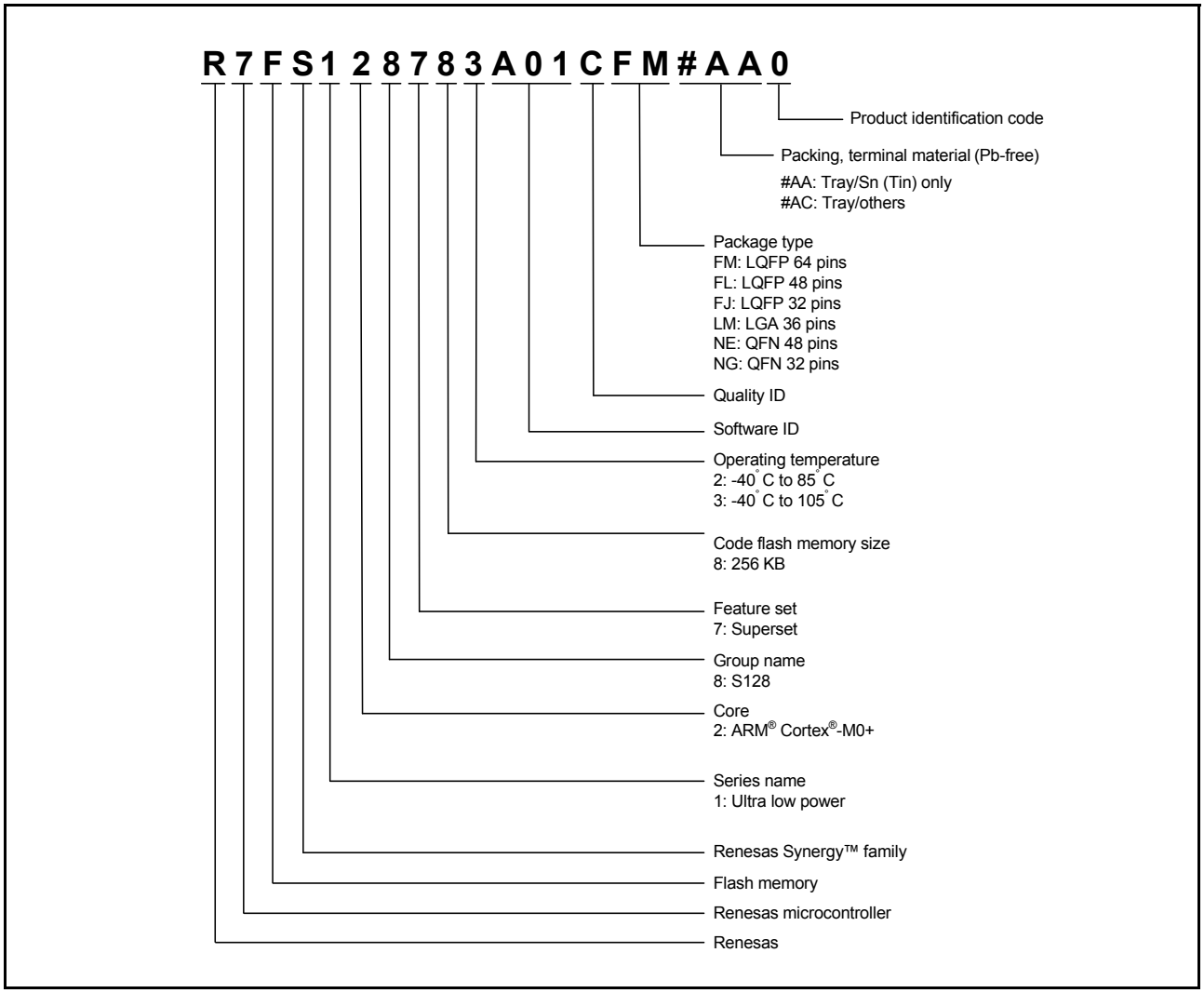

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS128783A01CFM	R7FS128783A01CFM#AA0	PLQP0064KB-C	256 KB	4 KB	24 KB	–40 to +105°C
R7FS128783A01CFL	R7FS128783A01CFL#AA0	PLQP0048KB-B				–40 to +105°C
R7FS128783A01CNE	R7FS128783A01CNE#AC0	PWQN0048KB-A				–40 to +105°C
R7FS128782A01CLM	R7FS128782A01CLM#AC0	PWLG0036KA-A				–40 to +85°C
R7FS128783A01CFJ	R7FS128783A01CFJ#AA0	PLQP0032GB-A				–40 to +105°C
R7FS128783A01CNG	R7FS128783A01CNG#AC0	PWQN0032KB-A				–40 to +105°C

1.4 Function Comparison

Table 1.13 Function comparison (1 of 2)

Parts number	R7FS128783A01CFM	R7FS128783A01CFL R7FS128783A01CNE	R7FS128782A01CLM	R7FS128783A01CFJ R7FS128783A01CNG
Pin count	64	48	36	32
Package	LQFP	LQFP/QFN	LGA	LQFP/QFN
Code flash memory	256 KB			

Table 1.13 Function comparison (2 of 2)

Parts number		R7FS128783A01CFM	R7FS128783A01CFL R7FS128783A01CNE	R7FS128782A01CLM	R7FS128783A01CFJ R7FS128783A01CNG
Data flash memory		4 KB			
SRAM		24 KB			
	Parity	8 KB			
	ECC	16 KB			
System	CPU clock	32 MHz			
	ICU	Yes			
	KINT	8	5	4	4
Event control	ELC	Yes			
DMA	DTC	Yes			
Timers	GPT32	1			
	GPT16H	3	3	3	2
	GPT16	3	3	1	1
	AGT	2			
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	3			
	DALI	Yes			
	IIC	2	2	1	1
	SPI	2	2	2	1
	CAN	Yes			
	USBFS	Yes			
Analog	ADC14	21	15	13	10
	DAC8	3			
	ACMPHS	3			
	ACMPLP	2			
	OPAMP	4	3	3	2
	TSN	Yes			
HMI	CTSU	28	21	12	9
Data processing	CRC	Yes			
	DOC	Yes			
Security		AES and TRNG			

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pin
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, output compare, or PWM output pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable
	AGTIO0, AGTIO1	I/O	External event input and pulse output
	AGTO0, AGTO1	Output	Pulse output
	AGTOA0, AGTOA1	Output	Output compare match A output
	AGTOB0, AGTOB1	Output	Output compare match B output
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
DALI	DRX0	Input	Input pin for DALI received data
	DTX0	Output	Output pin for DALI transmitted data
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
ADC14	AN000 to AN013, AN016 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
DAC8	DA0 to DA2	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPHS	IVREF0 to IVREF2	Input	Reference voltage input pin
	IVCMP0 to IVCMP2	Input	Analog voltage input pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP3+	Input	Analog voltage input pins
	AMP0- to AMP3-	Input	Analog voltage input pins
	AMP0O to AMP3O	Output	Analog voltage output pins
CTSU	TS00 to TS22, TS25 to TS29	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

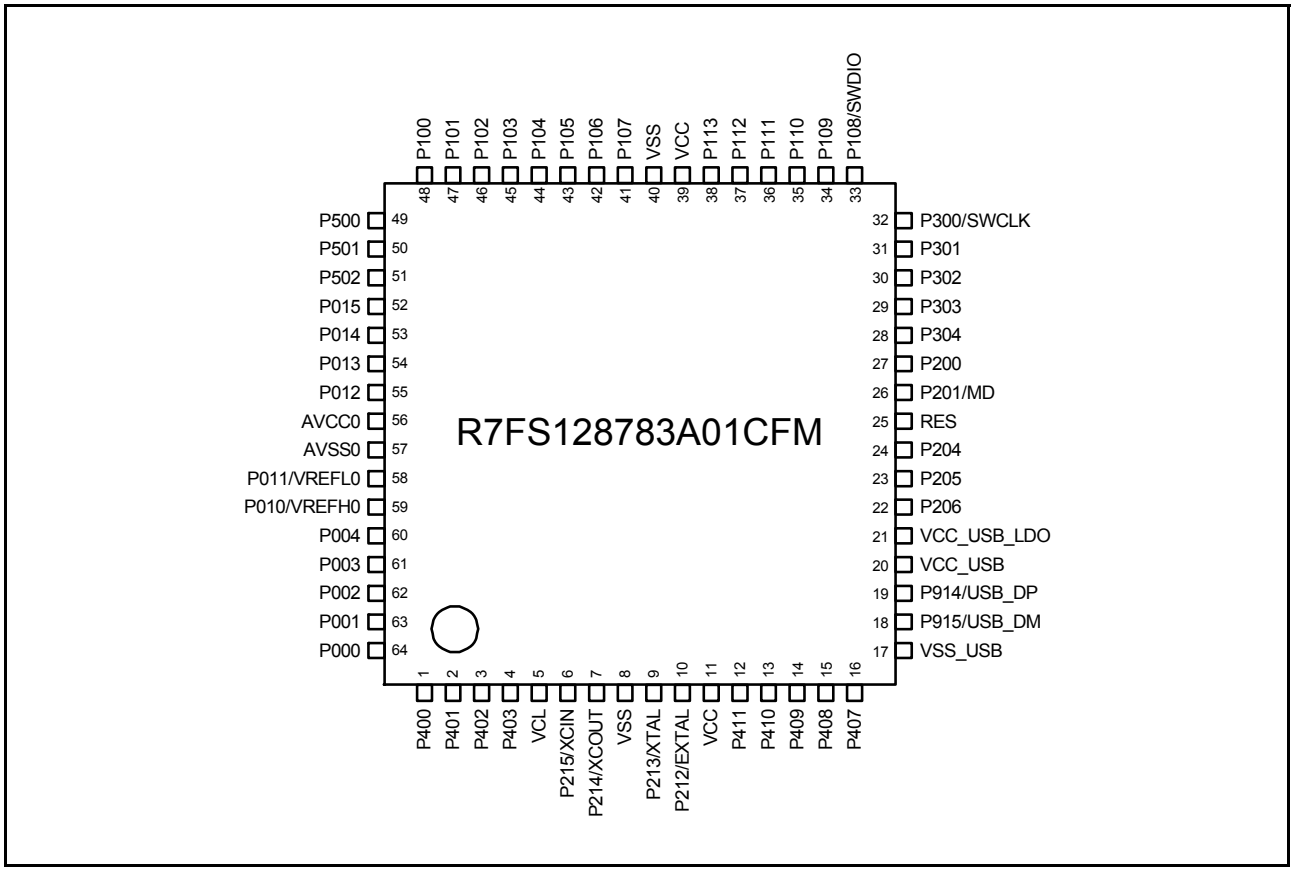

Figure 1.3 Pin assignment for LQFP 64-pin

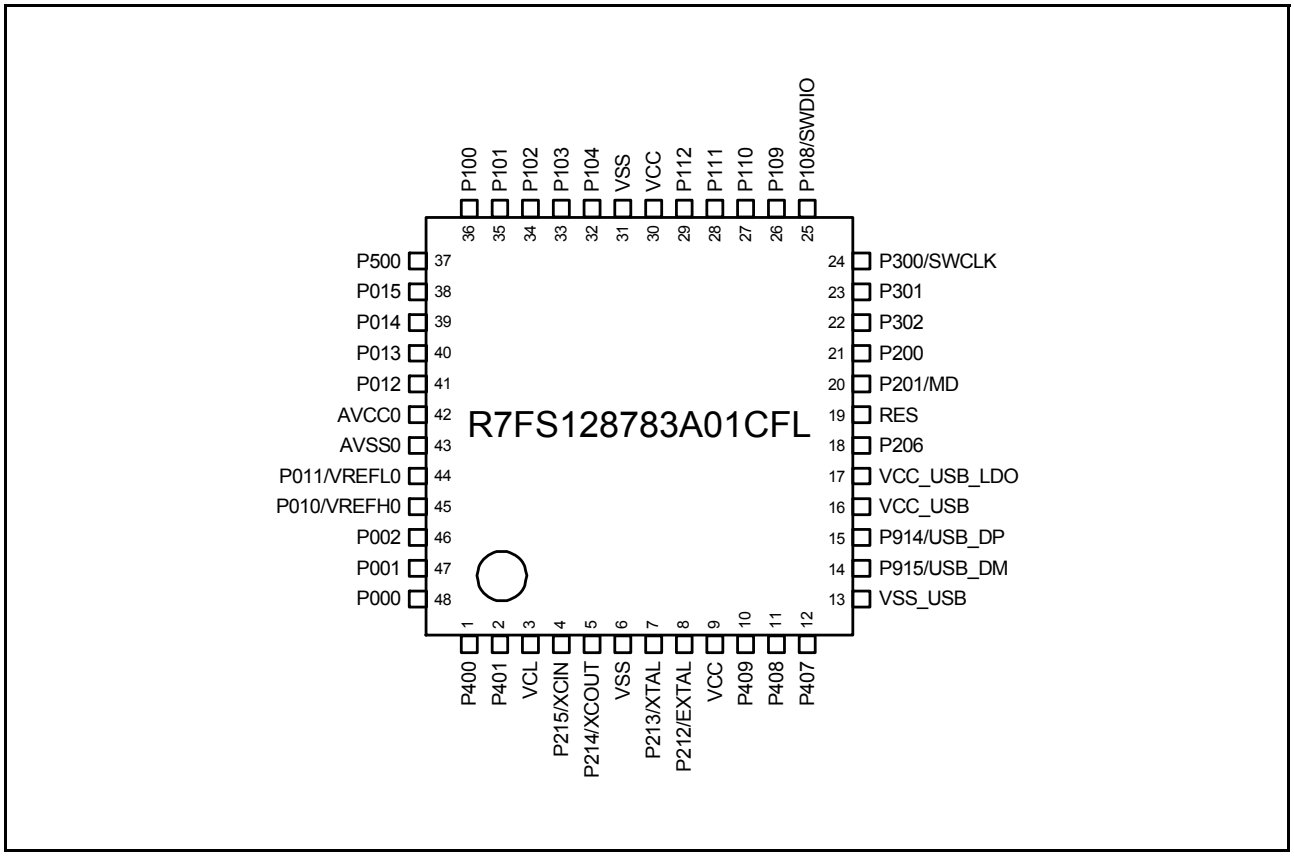

Figure 1.4 Pin assignment for LQFP 48-pin

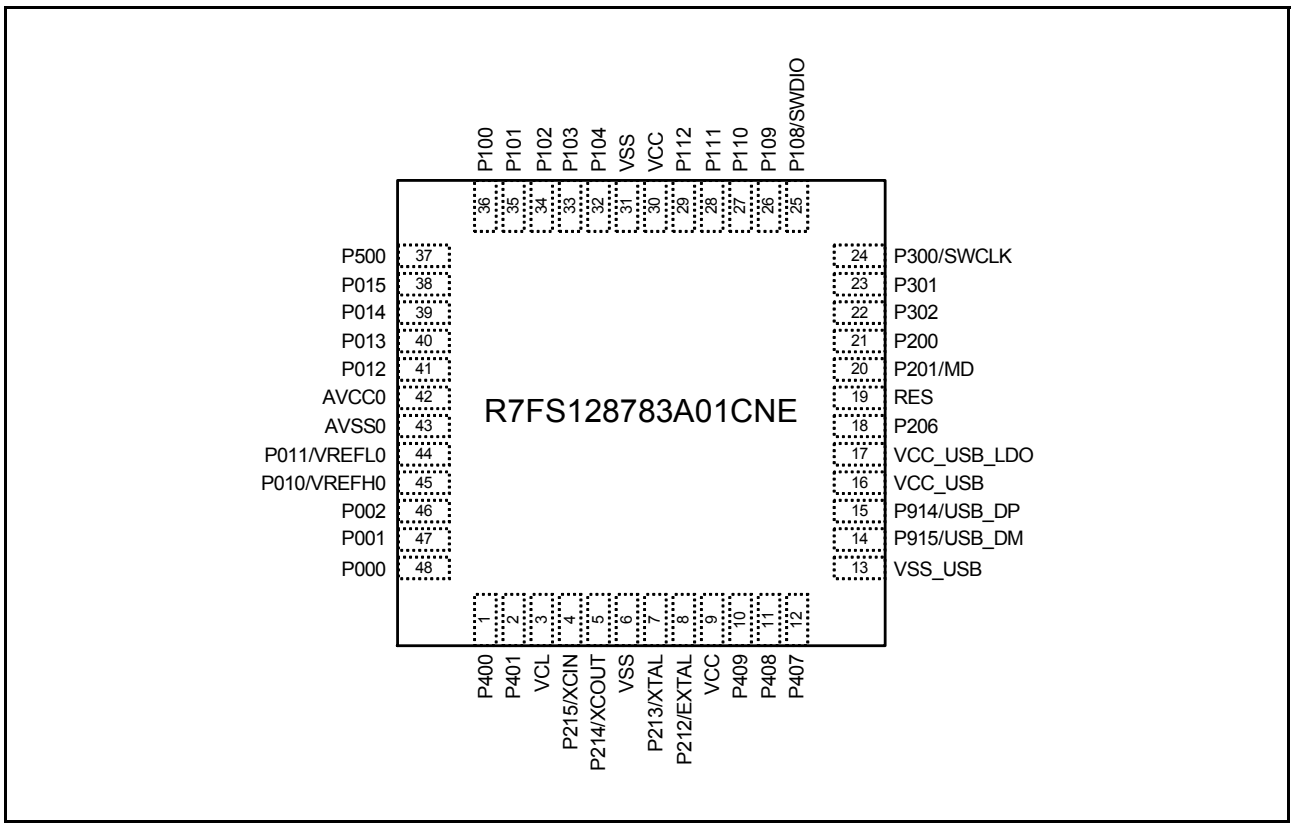

Figure 1.5 Pin assignment for QFN 48-pin

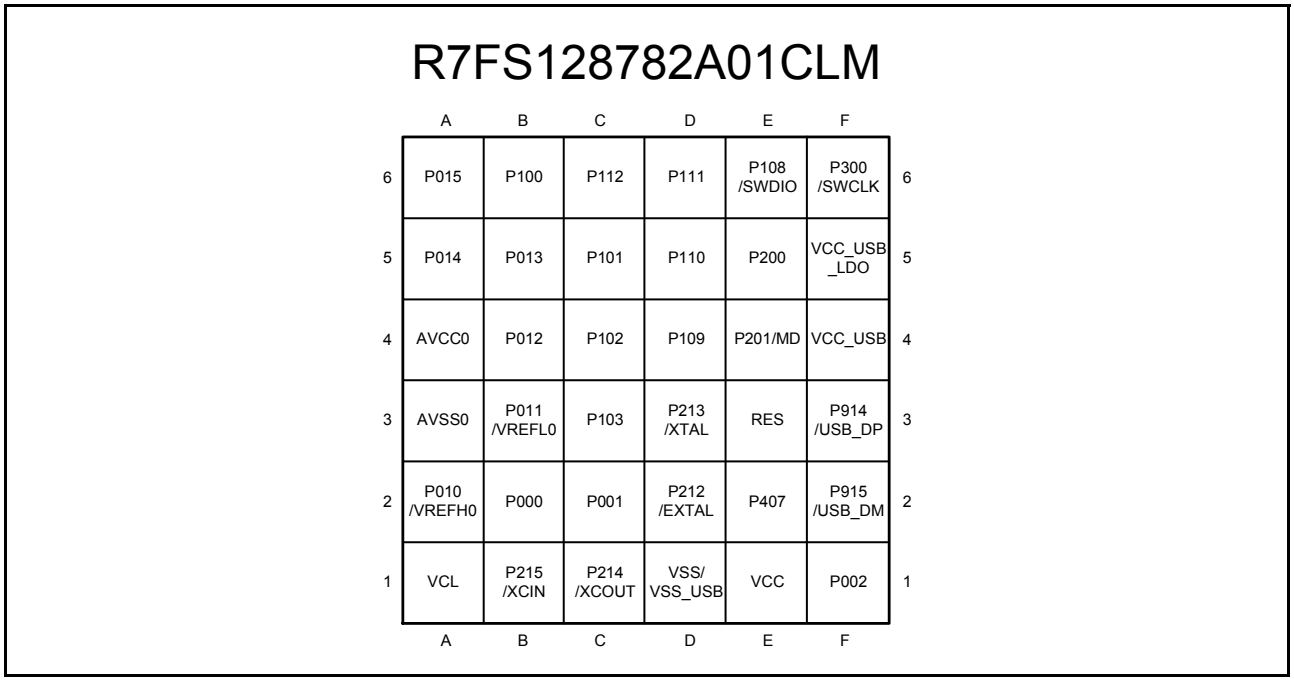

Figure 1.6 Pin assignment for LGA 36-pin (top view, pad side down)

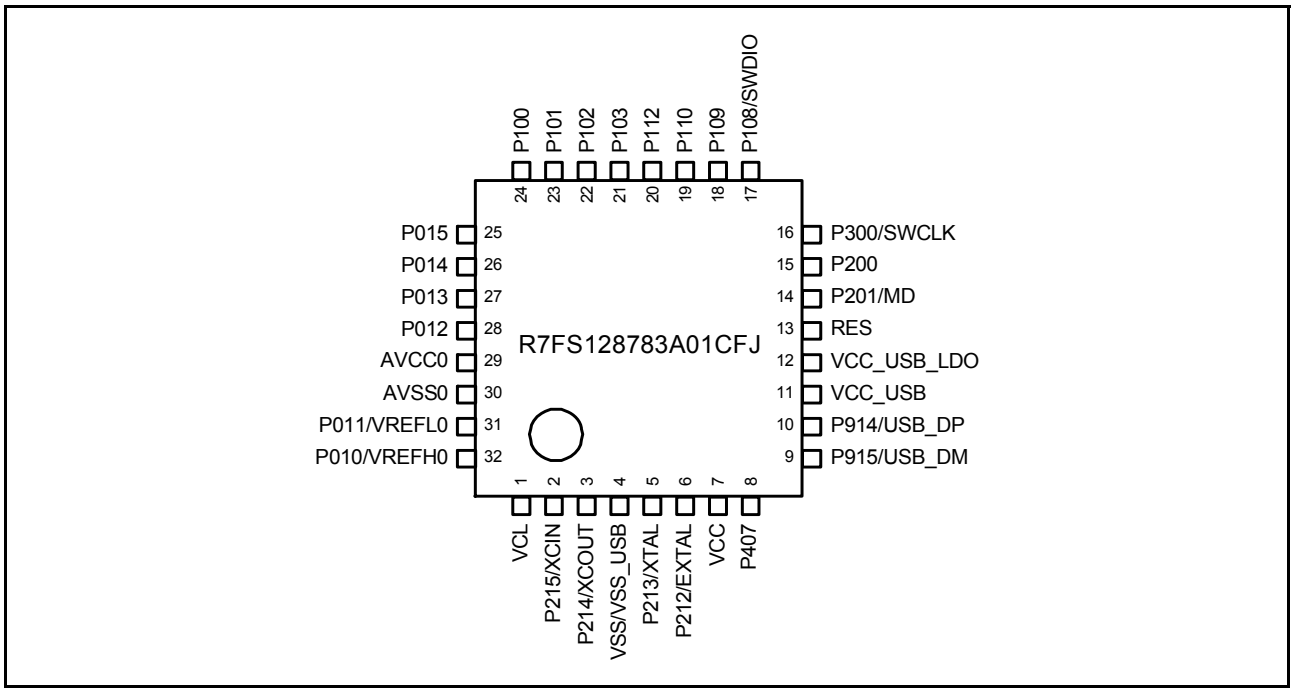

Figure 1.7 Pin assignment for LQFP 32-pin

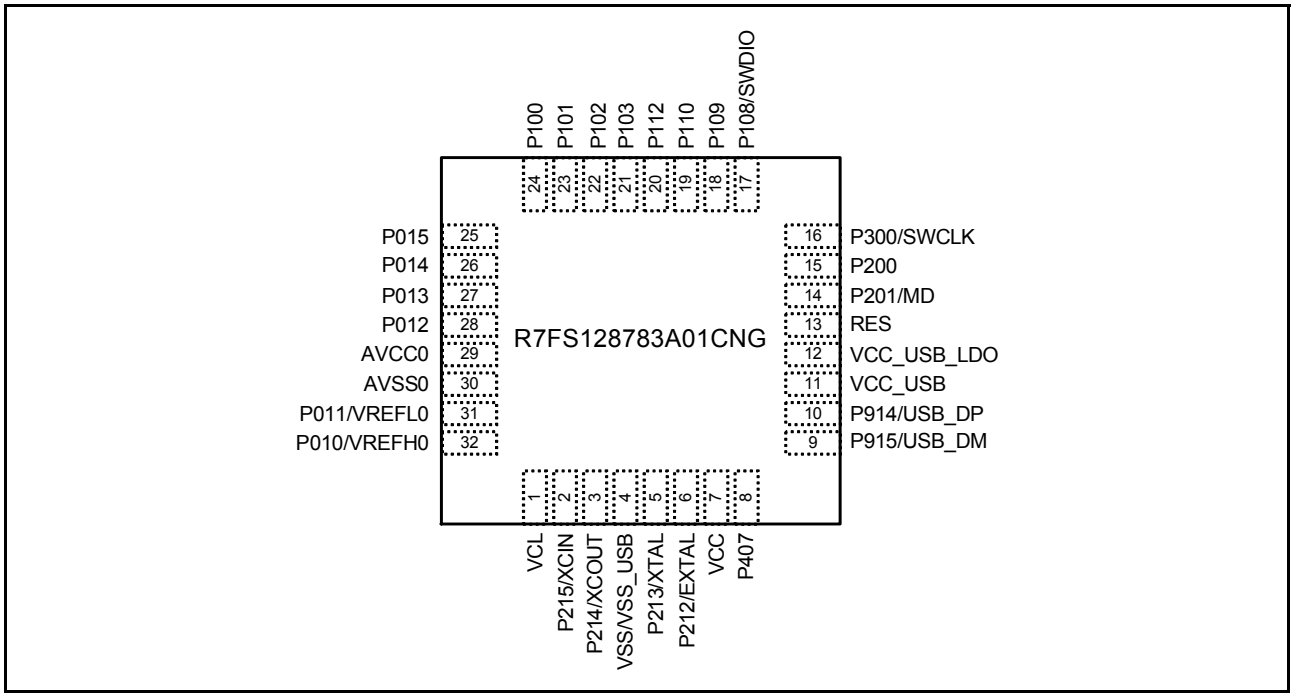

Figure 1.8 Pin assignment for QFN 32-pin

1.7 Pin Lists

Pin number								Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
1	1	1	-	-	-	CACREF_C	P400	AGTIO1_D		GTIOC6A_A			SCK0_B/ SCK1_B	SCL0_A						TS20	IRQ0
2	2	2	-	-	-		P401		GTETRGA_B	GTIOC6B_A		CTX0_B	CTS0_RTS0_B/SS0_B/ TXD1_B/ MOSI1_B/ SDA1_B	SDA0_A						TS19	IRQ5
3	-	-	-	-	-		P402			GTIOC3B_B		CRX0_B	RXD1_B/ MISO1_B/ SCL1_B							TS18	IRQ4
4	-	-	-	-	-		P403			GTIOC3A_B			CTS1_RTS1_B/SS1_B							TS17	
5	3	3	A1	1	1	VCL															
6	4	4	B1	2	2	XCIN	P215														
7	5	5	C1	3	3	XCOUT	P214														
8	6	6	D1	4	4	VSS															
9	7	7	D3	5	5	XTAL	P213		GTETRGA_D	GTIOC0A_D			TXD1_A/ MOSI1_A/ SDA1_A								IRQ2
10	8	8	D2	6	6	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D			RXD1_A/ MISO1_A/ SCL1_A								IRQ3
11	9	9	E1	7	7	VCC															
12	-	-	-	-	-		P411	AGTOA1	GTOVUP_B	GTIOC6A_B			TXD0_B/ MOSI0_B/ SDA0_B		MOSIA_B					TS07	IRQ4
13	-	-	-	-	-		P410	AGTOB1	GTOVLO_B	GTIOC6B_B			RXD0_B/ MISO0_B/ SCL0_B		MISOA_B					TS06	IRQ5
14	10	10	-	-	-		P409		GTOWUP_B	GTIOC5A_B			TXD0_E/ MOSI0_E/ SDA0_E/ TXD9_A/ MOSI9_A/ SDA9_A							TS05	IRQ6
15	11	11	-	-	-		P408		GTOWLO_B	GTIOC5B_B			RXD9_A/ MISO9_A/ SCL9_A	SCL0_C						TS04	IRQ7
16	12	12	E2	8	8		P407	AGTIO0_C		GTIOC0A_E	RTCOUT	USB_VBUS	CTS0_RTS0_D/SS0_D	SDA0_B	SSLB3_A	ADTRG0_B				TS03	
17	13	13	D1	4	4	VSS_USB															

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
18	14	14	F2	9	9		P915					USB_DM									
19	15	15	F3	10	10		P914					USB_DP									
20	16	16	F4	11	11	VCC_USB															
21	17	17	F5	12	12	VCC_USB_LDO															
22	18	18	-	-	-		P206		GTIU_A				RXD0_D/ MISO0_D/ SCL0_D	SDA1_A	SSLB1_A					TS01	IRQ0
23	-	-	-	-	-	CLKOUT_A	P205	AGTO1	GTIV_A	GTIOC4A_B			TXD0_D/ MOSI0_D/ SDA0_D/ CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A					TSCAP_A	IRQ1
24	-	-	-	-	-	CACREF_A	P204	AGTIO1_A	GTIW_A	GTIOC4B_B			SCK0_D/ SCK9_A	SCL0_B	RSPCKB_A					TS00	
25	19	19	E3	13	13	RES															
26	20	20	E4	14	14	MD	P201														
27	21	21	E5	15	15		P200														NMI
28	-	-	-	-	-		P304			GTIOC1A_B											
29	-	-	-	-	-		P303			GTIOC1B_B										TS02	
30	22	22	-	-	-		P302		GTOUUP_A	GTIOC4A_A					SSLB3_B					TS08	IRQ5
31	23	23	-	-	-		P301	AGTIO0_D	GTOULO_A	GTIOC4B_A			CTS9_RTS9_D/ SS9_D		SSLB2_B					TS09	IRQ6
32	24	24	F6	16	16	SWCLK	P300		GTOUUP_C	GTIOC0A_A					SSLB1_B						
33	25	25	E6	17	17	SWDIO	P108		GTOULO_C	GTIOC0B_A			CTS9_RTS9_B/SS9_B		SSLB0_B						
34	26	26	D4	18	18	CLKOUT_B	P109		GTOVUP_A	GTIOC1A_A		CTX0_A	SCK1_E/ TXD9_B/ MOSI9_B/ SDA9_B		MOSIB_B					TS10	
35	27	27	D5	19	19		P110		GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/ SS0_C/ RXD9_B/ MISO9_B/ SCL9_B		MISOB_B			VCOUT		TS11	IRQ3
36	28	28	D6	-	-		P111	AGTOA0		GTIOC3A_A			SCK0_C/ SCK9_B		RSPCKB_B					TS12	IRQ4
37	29	29	C6	20	20		P112	AGTOB0		GTIOC3B_A			TXD0_C/ MOSI0_C/ SDA0_C/ SCK1_D		SSLB0_C					TSCAP_C	
38	-	-	-	-	-		P113			GTIOC2A_C											
39	30	30	-	-	-	VCC															
40	31	31	-	-	-	VSS															
41	-	-	-	-	-		P107			GTIOC0A_B											KR07
42	-	-	-	-	-		P106			GTIOC0B_B					SSLA3_A	AN016					KR06
43	-	-	-	-	-		P105		GTETRGA_C	GTIOC1A_C					SSLA2_A	AN017					KR05/ IRQ0
44	32	32	-	-	-		P104		GTETRGB_B	GTIOC1B_C			RXD0_C/ MISO0_C/ SCL0_C		SSLA1_A	AN018				TS13	KR04/ IRQ1
45	33	33	C3	21	21		P103		GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/SS0_A		SSLA0_A	AN019		CMPREF1		TS14	KR03
46	34	34	C4	22	22		P102	AGTO0	GTOWLO_A	GTIOC2B_A		CRX0_C	SCK0_A		RSPCKA_A	AN020/ ADTRG0_A		CMPIN1		TS15	KR02
47	35	35	C5	23	23		P101	AGTEE0	GTETRGB_A	GTIOC5A_A		DTX0	TXD0_A/ MOSI0_A/ SDA0_A/ CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	AN021		CMPREF0		TS16	KR01/ IRQ1
48	36	36	B6	24	24		P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A		DRX0	RXD0_A/ MISO0_A/ SCL0_A/ SCK1_A	SCL1_B	MISOA_A	AN022		CMPIN0		TS26	KR00/ IRQ2
49	37	37	-	-	-		P500									AN013	DA1_B			TS27	
50	-	-	-	-	-		P501									AN012			AMP3+		
51	-	-	-	-	-		P502									AN011			AMP3-		
52	38	38	A6	25	25		P015									AN010	DA1_A	IVCMP1	AMP2+	TS28	IRQ7
53	39	39	A5	26	26		P014									AN009	DA0	IVREF1	AMP2-	TS29	
54	40	40	B5	27	27		P013									AN008		IVCMP0	AMP1+		
55	41	41	B4	28	28		P012									AN007		IVREF0	AMP1-		

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
56	42	42	A4	29	29	AVCC0															
57	43	43	A3	30	30	AVSS0															
58	44	44	B3	31	31	VREFL0	P011									AN006	DA2_A		AMP2O		
59	45	45	A2	32	32	VREFH0	P010									AN005			AMP1O		
60	-	-	-	-	-		P004									AN004	DA2_B			TS25	IRQ3
61	-	-	-	-	-		P003									AN003			AMP3O		
62	46	46	F1	-	-		P002									AN002			AMP0O		IRQ2
63	47	47	C2	-	-		P001									AN001		IVREF2	AMP0-	TS22	IRQ7
64	48	48	B2	-	-		P000									AN000		IVCMP2	AMP0+	TS21	IRQ6

Note: Several pin names have the added suffix of _A, _B, _C, _D and _E. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

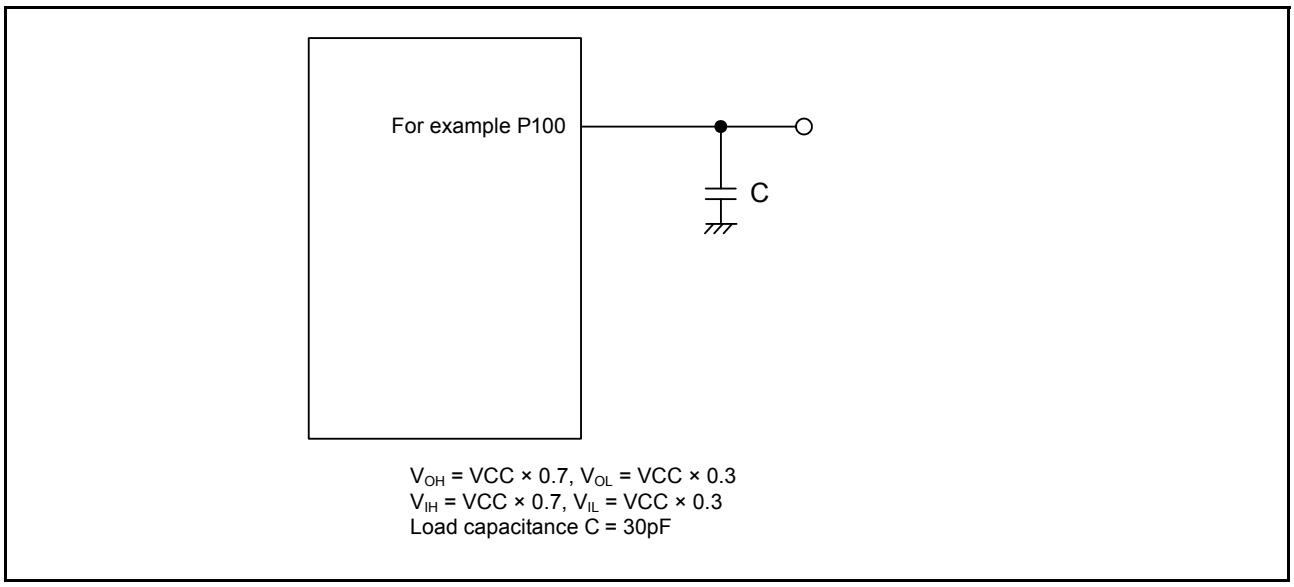

Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	–0.5 to +6.5	V
Input voltage	5 V tolerant ports*1	V_{in}	–0.3 to +6.5	V
	P000 to P004 P010 to P015 P500 to P502	V_{in}	–0.3 to AVCC0 + 0.3	V
	Others	V_{in}	–0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	–0.3 to +6.5	V
Analog power supply voltage		AVCC0	–0.5 to +6.5	V
USB power supply voltage		VCC_USB	–0.5 to +6.5	V
		VCC_USB_LDO	–0.5 to +6.5	V
Analog input voltage	When AN000 to AN013 are used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN022 are used		–0.3 to VCC + 0.3	V
Operating temperature*2 *3		T_{opr}	–40 to +85 –40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Note: Contact Renesas Electronics sales office for information on derating operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Note 1. Ports P205, P206, P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 2. See section 2.2.1, Tj/Ta Definition.

Note 3. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7-µF capacitor. The capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB_LDO	-	5.5	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 and VCC can be set individually within the operating range when VCC ≥ 2.0 V
AVCC0 = VCC when VCC < 2.0 V.

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics
Conditions: Products with operating temperature (T_a) –40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC – V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC =2.7 to 3.6 V
		V_{IL}	–0.3	-	0.8		-
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015 P500 to P502	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A (total 5 pins)
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins)
Note 3. P205, P206, P400, P401, P407 (total 5pins)