Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

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Contact us

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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Product Summary (Typ.@ V_{GS} = 4.5V, T_A = +25°C)

BV_{DSS}	$R_{DS(ON)}$	I_D
12V	38mΩ	4.0A

Description

This new generation MOSFET is engineered to minimize on-state losses and switch ultra-fast, making it ideal for high-efficiency power transfer. It uses Chip-Scale Package (CSP) to increase power density by combining low thermal impedance with minimal $R_{DS(ON)}$ per footprint area.

Applications

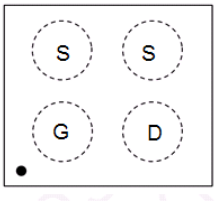
- DC-DC Converters
- Battery Management
- Load Switch

Features

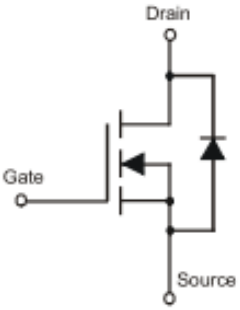
- TR-MOS Technology with the Lowest $R_{DS(ON)}$
- CSP with Footprint 0.81mm × 0.81mm (Typ.)
- Height = 0.29mm for Low Profile
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: X3-DSN0808-4
- Terminal Connections: See Diagram Below
- Terminal Finish: Matte Tin Annealed Over Copper Pillar e3
- UBM: 203µm



Top-View
Pin Configuration



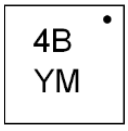
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN1053UCP4-7	X3-DSN0808-4	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



4B = Product Type Marking Code
YM = Date Code Marking
Y or $\overline{Y}$ = Year (ex: E = 2017)
M or $\overline{M}$ = Month (ex: 9 = September)

Date Code Key

Year	2016	2017	2018	2019	2020	2021	2022
Code	D	E	F	G	H	I	J

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	12	V
Gate-Source Voltage		V_{GSS}	±8	V
Continuous Source Current @ V_{GS} = 4.5V (Note 5)	T_A = +25°C T_A = +70°C	I_D	2.7 2.2	A
Continuous Source Current @ V_{GS} = 4.5V (Note 6)	T_A = +25°C T_A = +70°C	I_D	4.0 3.2	A
Pulsed Drain Current (Pulse Duration 10µs, Duty Cycle ≤1%)		I_{DM}	8	A
Continuous Source-Drain Diode Current		I_S	0.74	A
Pulse Diode Forward Current		I_{SM}	15	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.74	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	167	°C/W
Total Power Dissipation (Note 6)	P_D	1.34	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	93	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	-	-	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1.0	µA	V_{DS} = 9.6V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.35	0.5	0.7	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	38 42 45 49 57 82	42 50 53 65 80 110	mΩ	V_{GS} = 4.5V, I_D = 1.0A V_{GS} = 2.5V, I_D = 1.0A V_{GS} = 2.1V, I_D = 1.0A V_{GS} = 1.8V, I_D = 0.5A V_{GS} = 1.5V, I_D = 0.2A V_{GS} = 1.2V, I_D = 0.1A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	6.0	-	S	V_{DS} = 6V, I_S = 1.0A
Body Diode Forward Voltage	V_{SD}	-	0.7	1	V	V_{GS} = 0V, I_S = 1.0A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	612	908	pF	V_{DS} = 6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	91	127	pF	
Reverse Transfer Capacitance	C_{rss}	-	84	126	pF	
Gate Resistance	R_g	-	1.3	2.6	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	-	7.2	15	nC	V_{GS} = 4.5V, V_{DS} = 6V, I_D = 1.0A
Gate-Source Charge	Q_{gs}	-	0.6	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.3	-	nC	
Turn-On Delay Time	$t_{D(ON)}$	-	3.6	10	ns	V_{DD} = 6V, I_D = 1.0A V_{GEN} = 4.5V, R_G = 1Ω, R_L = 6Ω
Turn-On Rise Time	t_R	-	6.0	14	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	-	13.5	32	ns	
Turn-Off Fall Time	t_F	-	2	4	ns	
Reverse Recovery Charge	Q_{RR}	-	0.7	1.5	nC	I_F = 1A, di/dt = 100A/µs
Body Diode Reverse Recovery Time	t_{RR}	-	6.4	14	ns	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

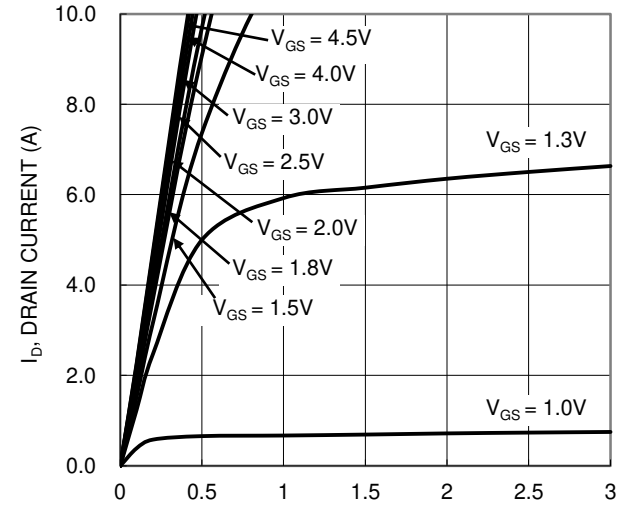


Figure 1. Typical Output Characteristic

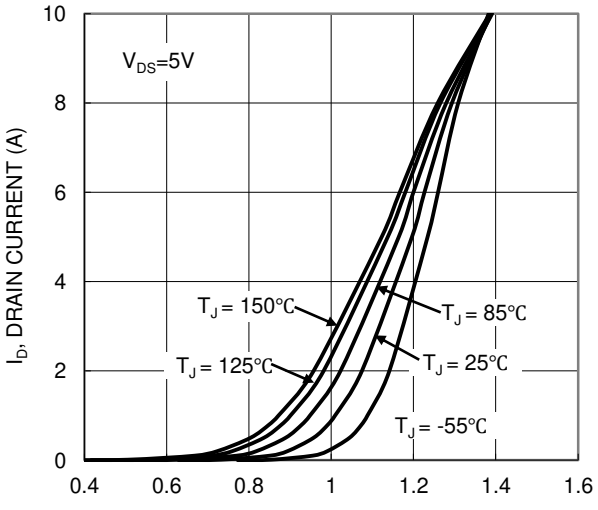


Figure 2. Typical Transfer Characteristic

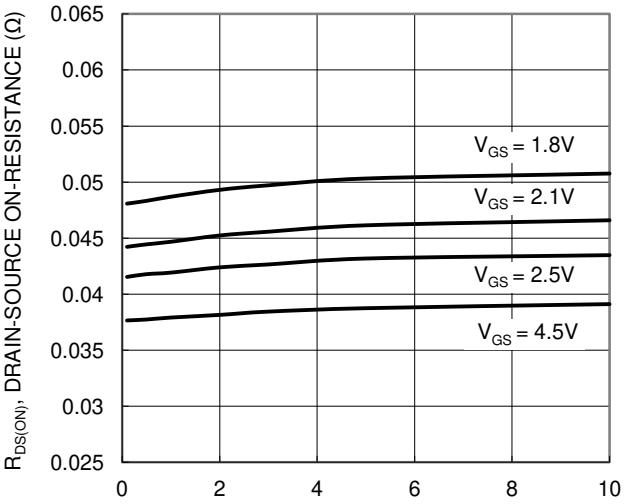


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

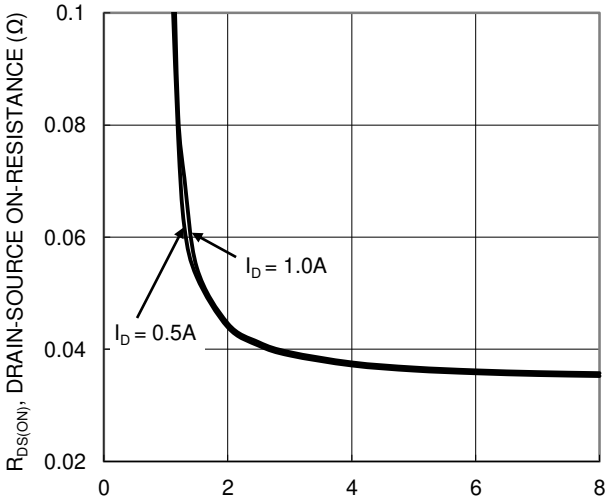


Figure 4. Typical Transfer Characteristic

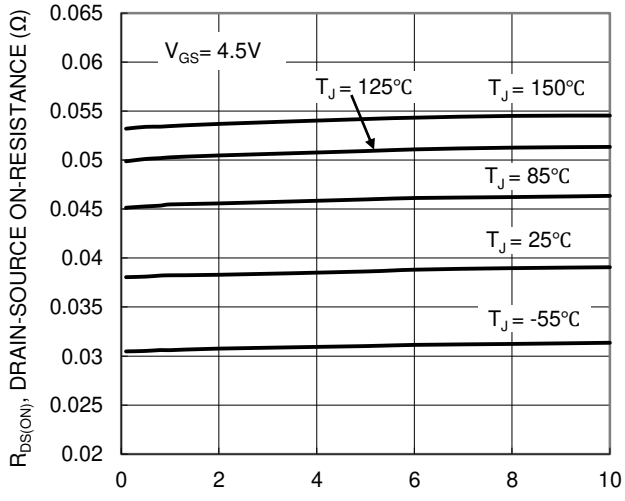


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

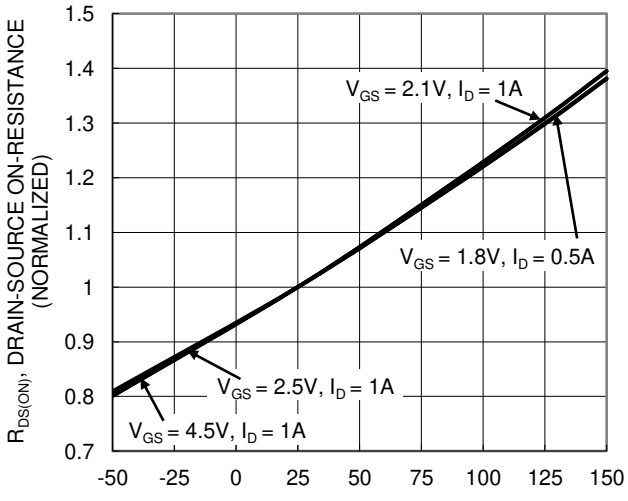


Figure 6. On-Resistance Variation with Junction Temperature

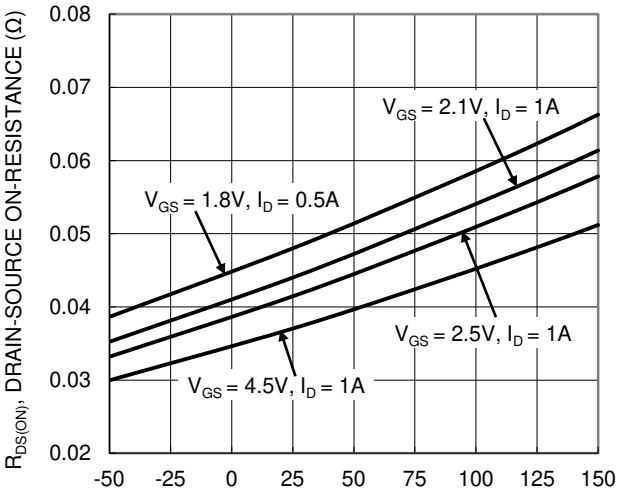


Figure 7. On-Resistance Variation with Junction Temperature

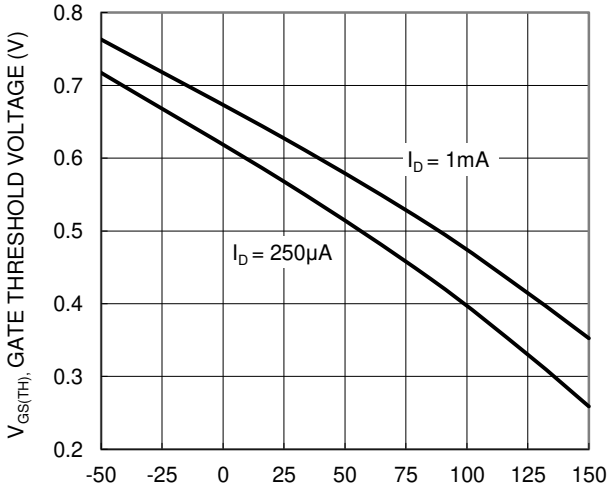


Figure 8. Gate Threshold Variation vs. Junction Temperature

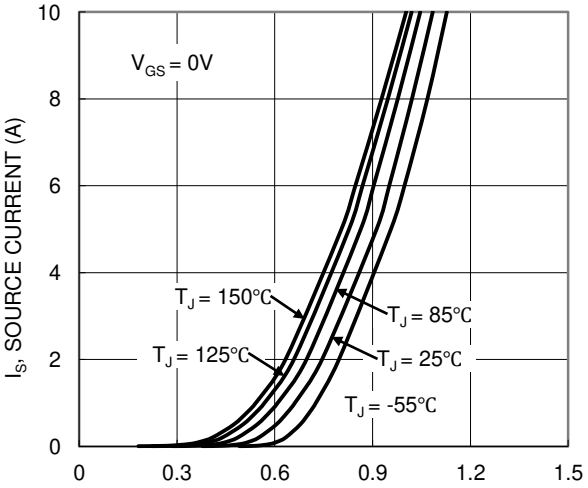


Figure 9. Diode Forward Voltage vs. Current

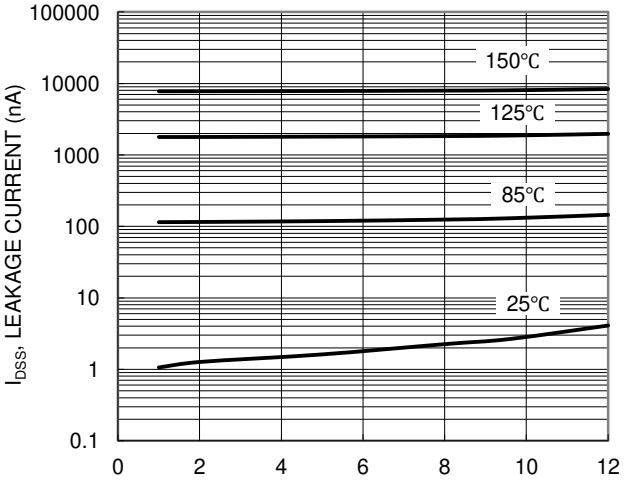


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

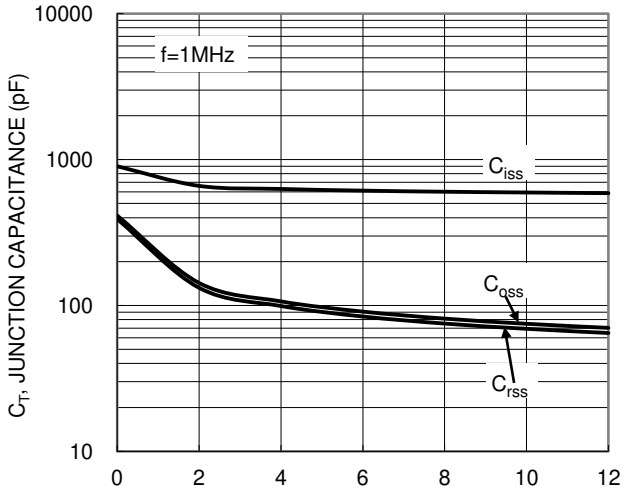


Figure 11. Typical Junction Capacitance

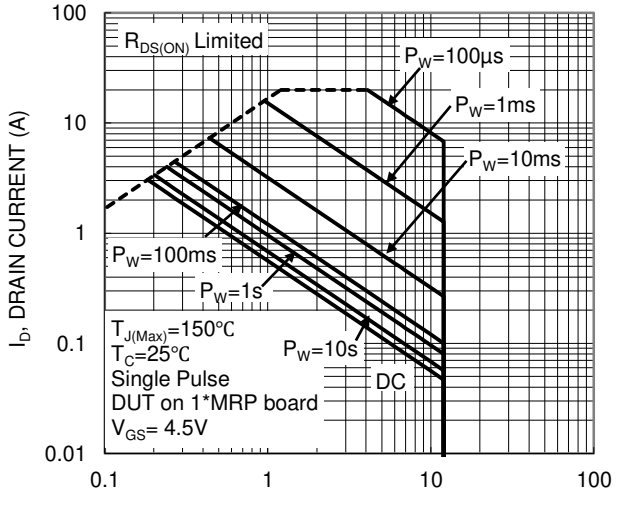


Figure 12. SOA, Safe Operation Area

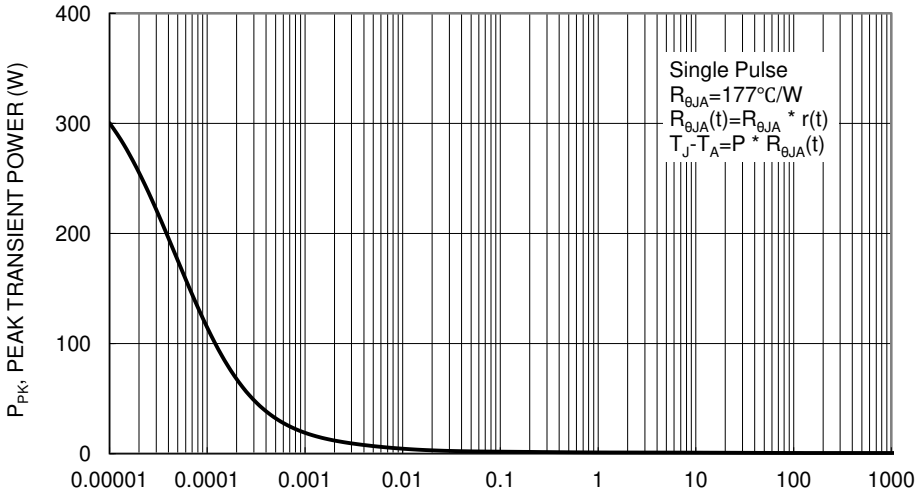


Figure 13. Single Pulse Maximum Power Dissipation

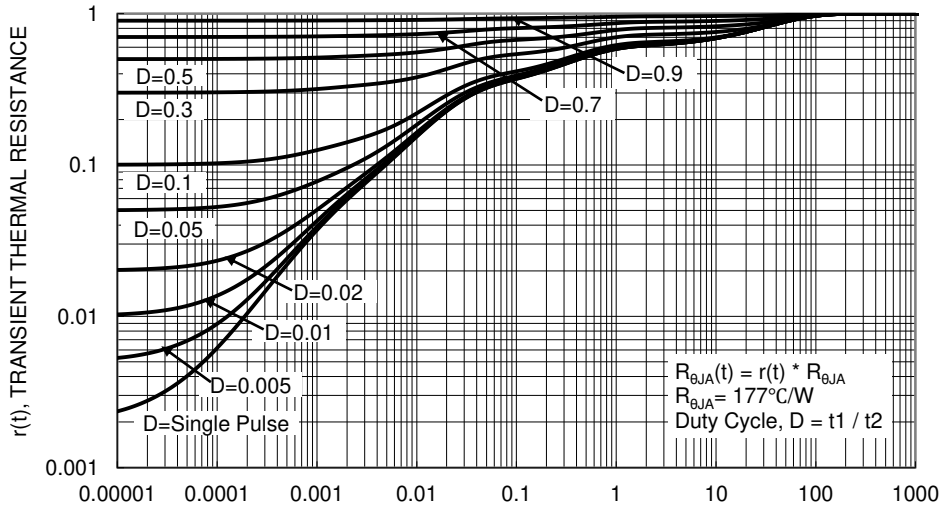
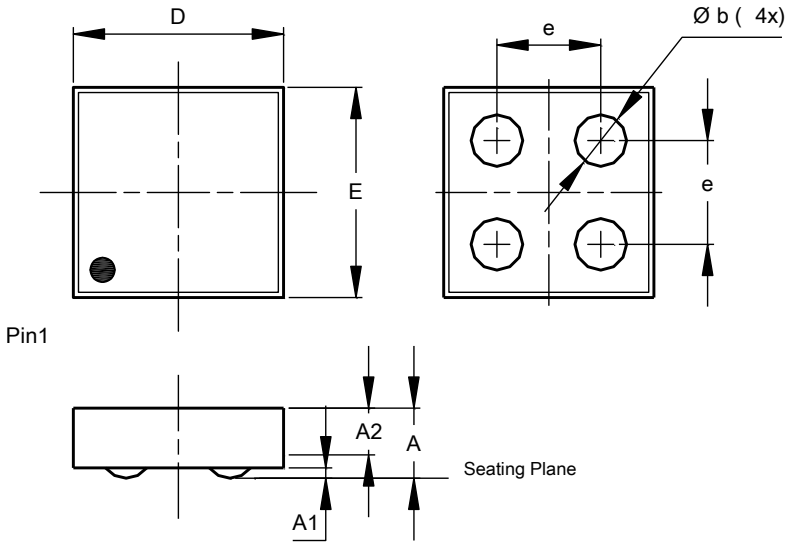


Figure14. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN0808-4

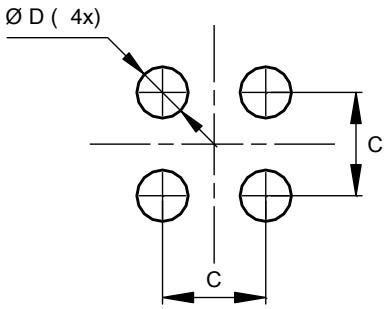


X3-DSN0808-4			
Dim	**Min**	**Max**	**Typ**
A	0.2510	0.2890	0.2700
A1	0.0360	0.0440	0.0400
A2	0.2150	0.2450	0.2300
b	0.1836	0.2244	0.2040
D	0.7900	0.8300	0.810
E	0.7900	0.8300	0.810
e	-	-	0.400
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X3-DSN0808-4



Dimensions	Value (in mm)
C	0.400
D	0.2040

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