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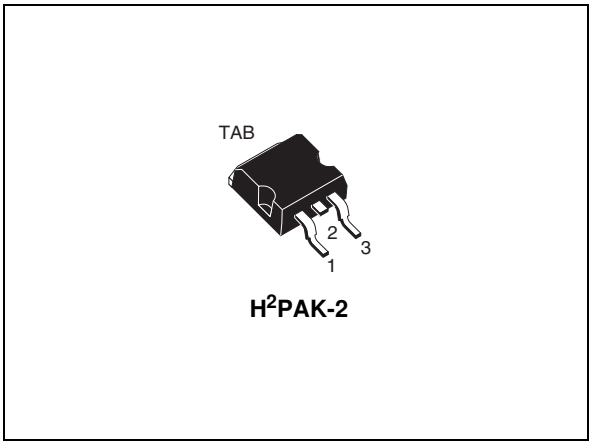
STH160N4LF6-2

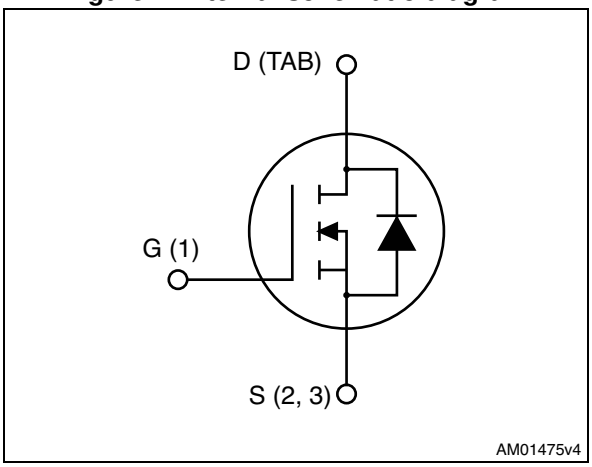
N-channel 40 V, 0.0018 mΩ typ., 120 A, STripFET™ VI DeepGATE™ Power MOSFET in a H²PAK-2 package

Datasheet - production data



H²PAK-2

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STH160N4LF6-2	40 V	0.0022 Ω	120 A	150 W

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Logic level drive
- High avalanche ruggedness
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH160N4LF6-2	160N4LF6	H²PAK-2	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	120	A
I_D	Drain current (continuous) at T_C = 100 °C	100	A
I_{DM}(1)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
	Derating factor	1	W/°C
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	60	A
E_{AS}	Single pulse avalanche energy	323	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

1. Pulse width is limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.0	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 250 µA	40	-		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 20 V		-	1	µA
		V_{DS} = 20 V, Tc = 125 °C			10	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	-		V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		0.0018	0.0022	Ω
		V_{GS} = 5 V, I_D = 60 A		0.002	0.0027	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 20 V, f=1 MHz, V_{GS} = 0 V	-	8130	-	pF
C_{oss}	Output capacitance		-	770	-	pF
C_{rss}	Reverse transfer capacitance		-	670	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 60 A V_{GS} = 10 V *(see Figure 14)*	-	181	-	nC
Q_{gs}	Gate-source charge		-	22	-	nC
Q_{gd}	Gate-drain charge		-	46	-	nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 15)*	-	20	-	ns
t_r	Rise time		-	131	-	ns
$t_{d(off)}$	Turn-off delay time		-	205	-	ns
t_f	Fall time		-	116	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM}(1)	Source-drain current (pulsed)		-		480	A
V_{SD}(2)	Forward on voltage	I_{SD} = 120 A, V_{GS} = 0	-		0.97	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD} = 32 V *(see Figure 17)*	-	57		ns
Q_{rr}	Reverse recovery charge		-	53		nC
I_{RRM}	Reverse recovery current		-	1.86		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

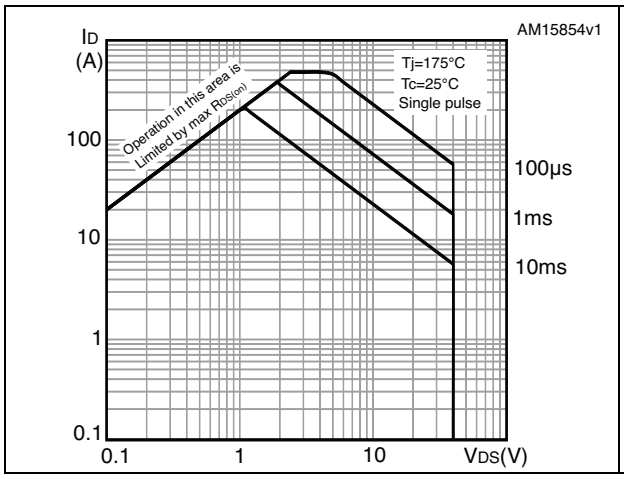


Figure 3. Thermal impedance

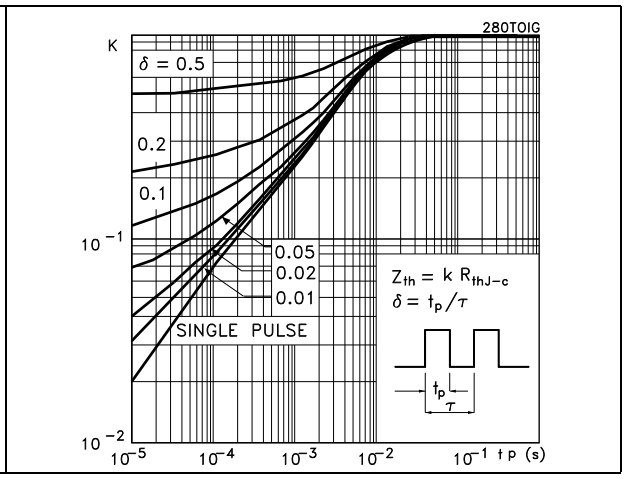


Figure 4. Output characteristics

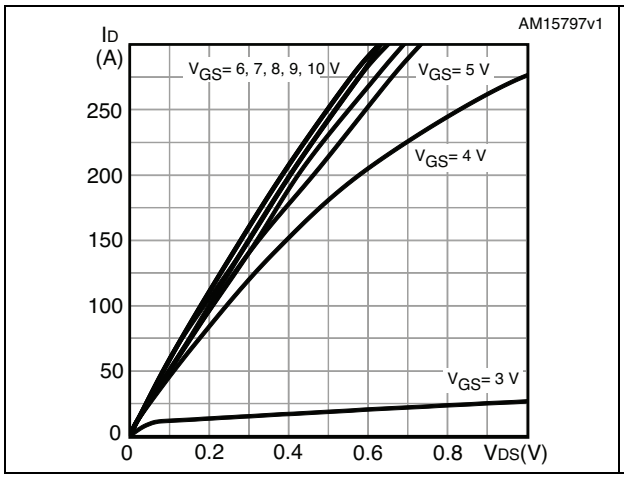


Figure 5. Transfer characteristics

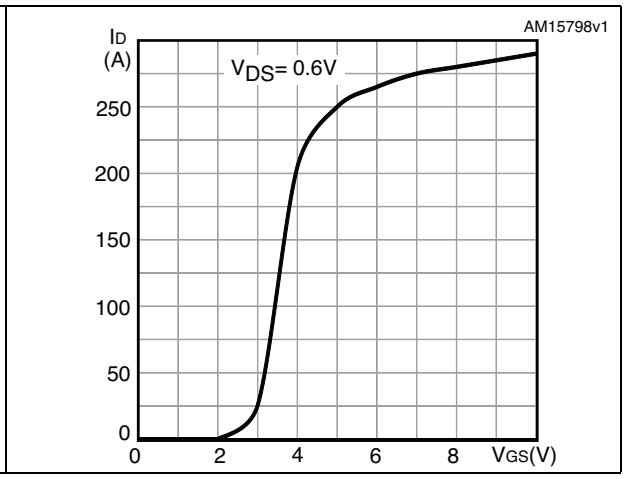


Figure 6. Gate charge vs gate-source voltage

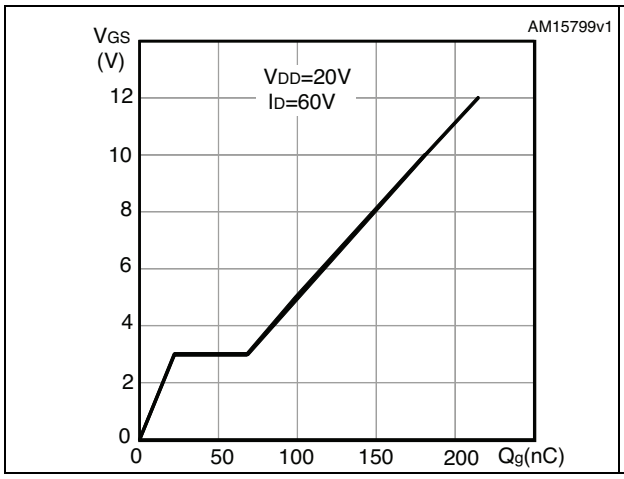


Figure 7. Static drain-source on-resistance

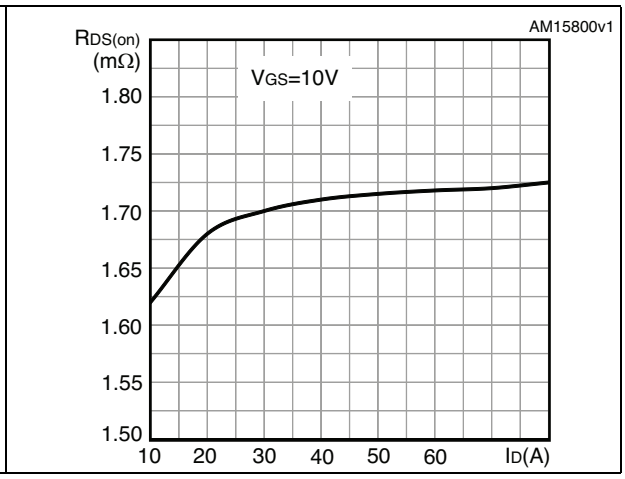


Figure 8. Capacitance variations

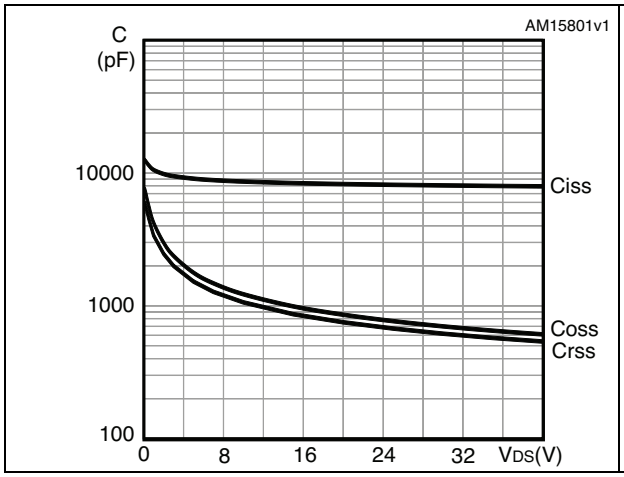


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

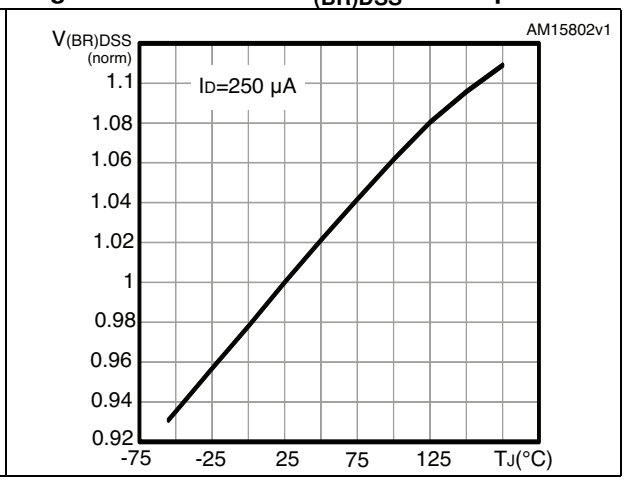


Figure 10. Normalized gate threshold voltage vs temperature

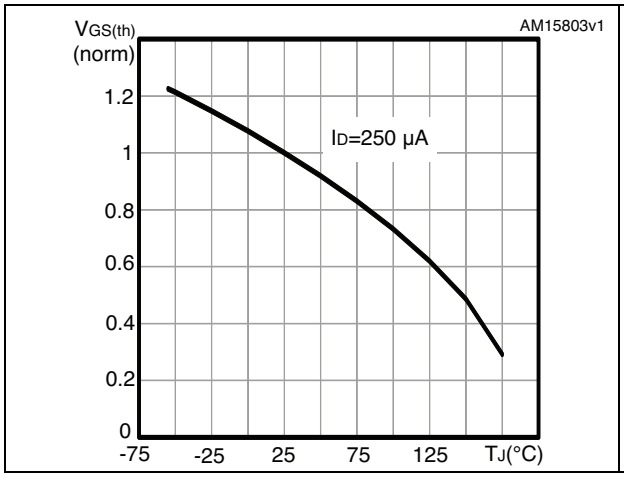


Figure 11. Normalized on-resistance vs temperature

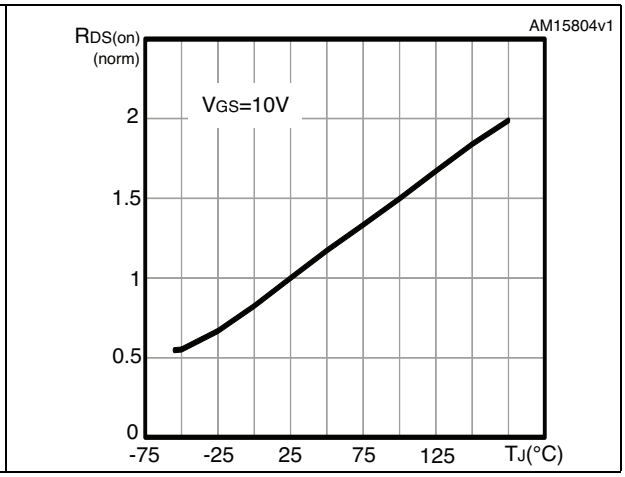
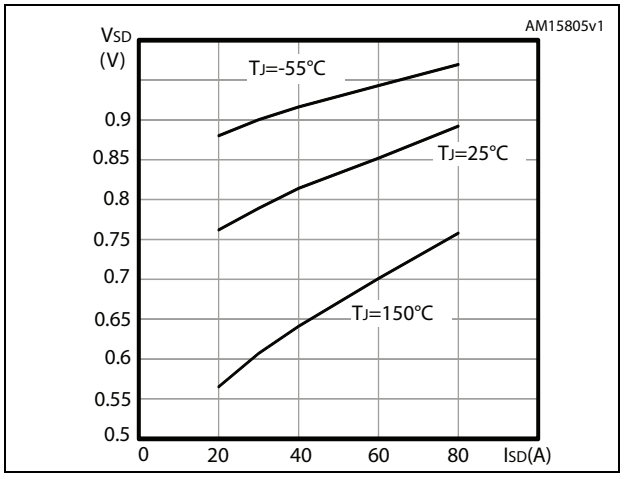


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

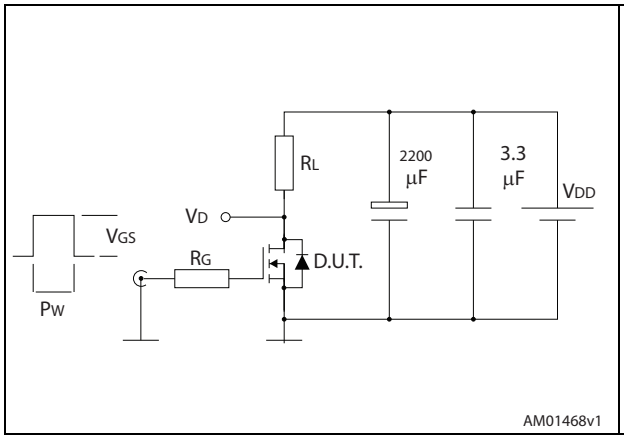


Figure 14. Gate charge test circuit

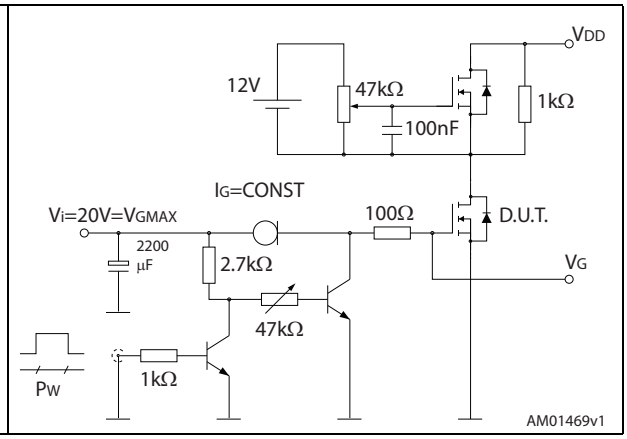


Figure 15. Test circuit for inductive load switching and diode recovery times

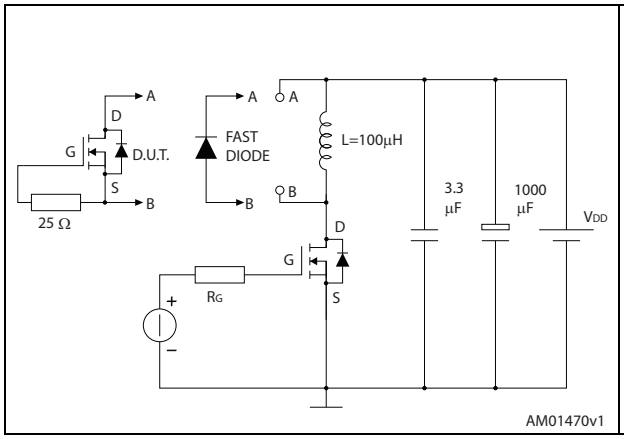


Figure 16. Unclamped inductive load test circuit

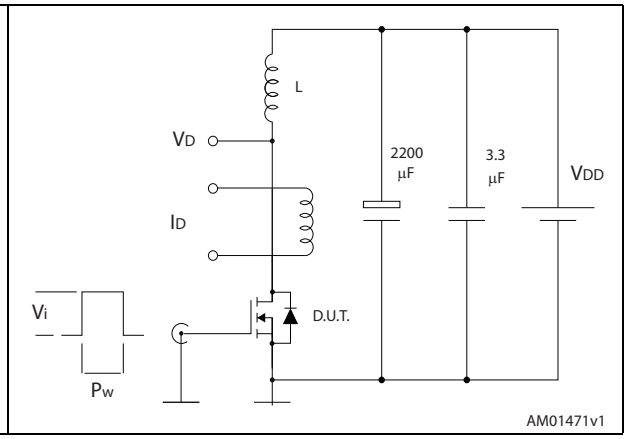


Figure 17. Unclamped inductive waveform

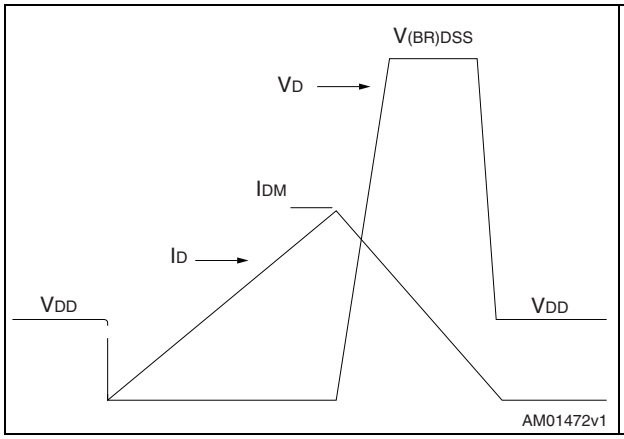


Figure 18. Switching time waveform

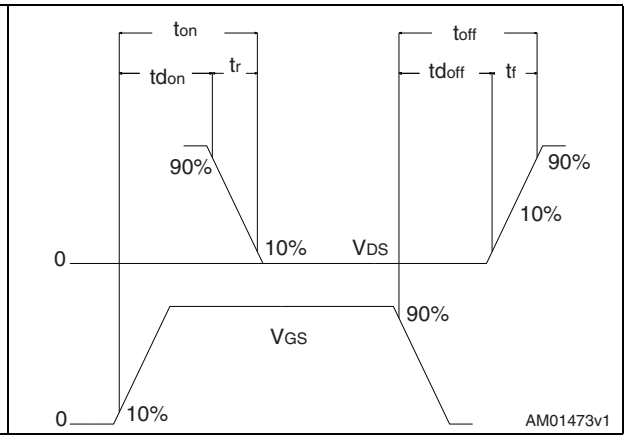
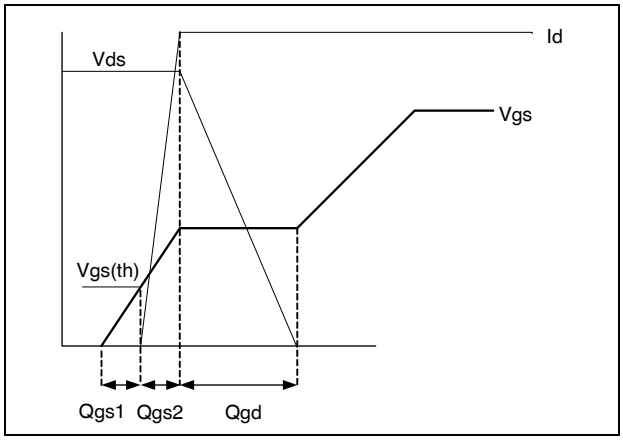


Figure 19. Gate charge waveform



4 Package mechanical data

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Figure 20. H²PAK-2 drawing

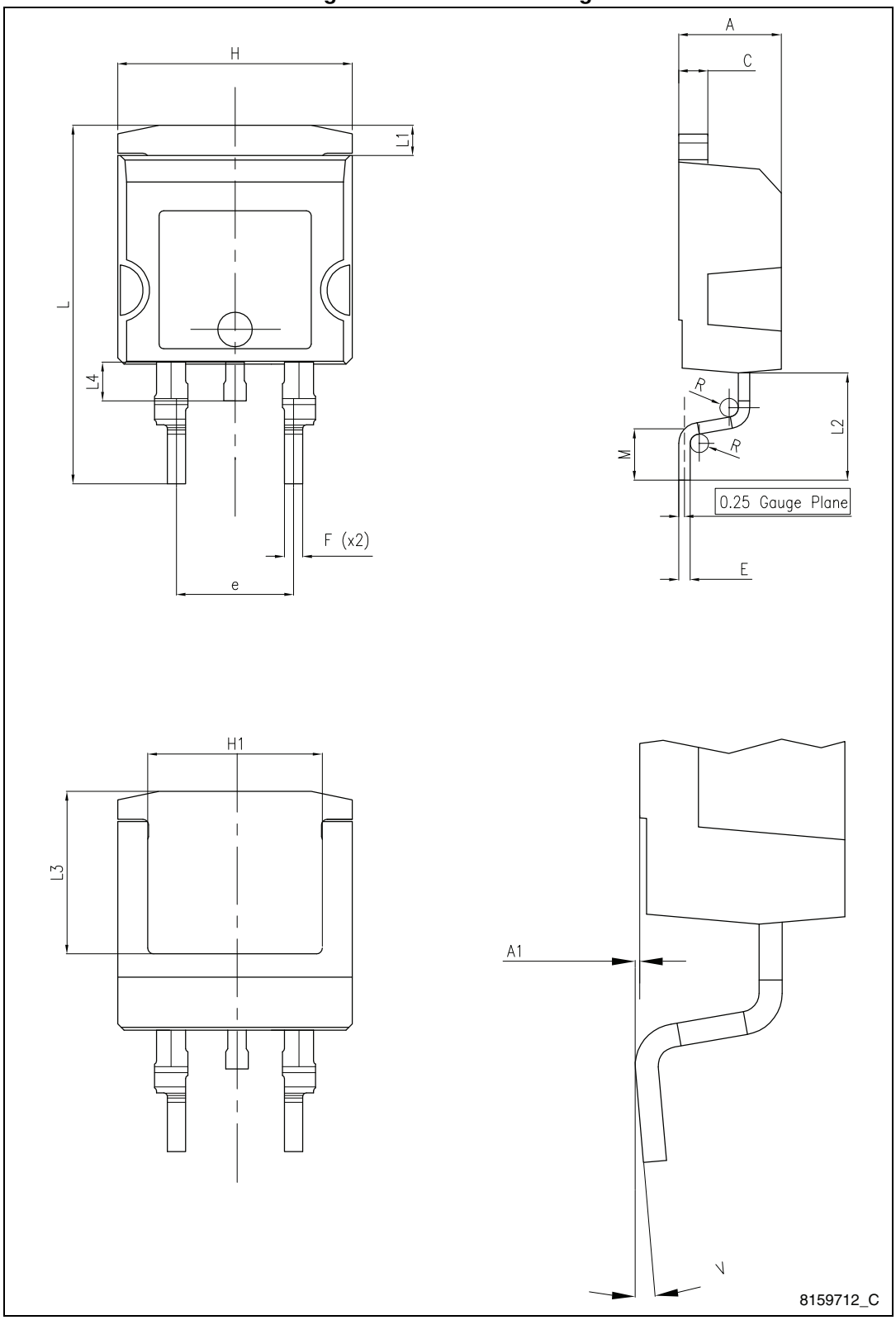
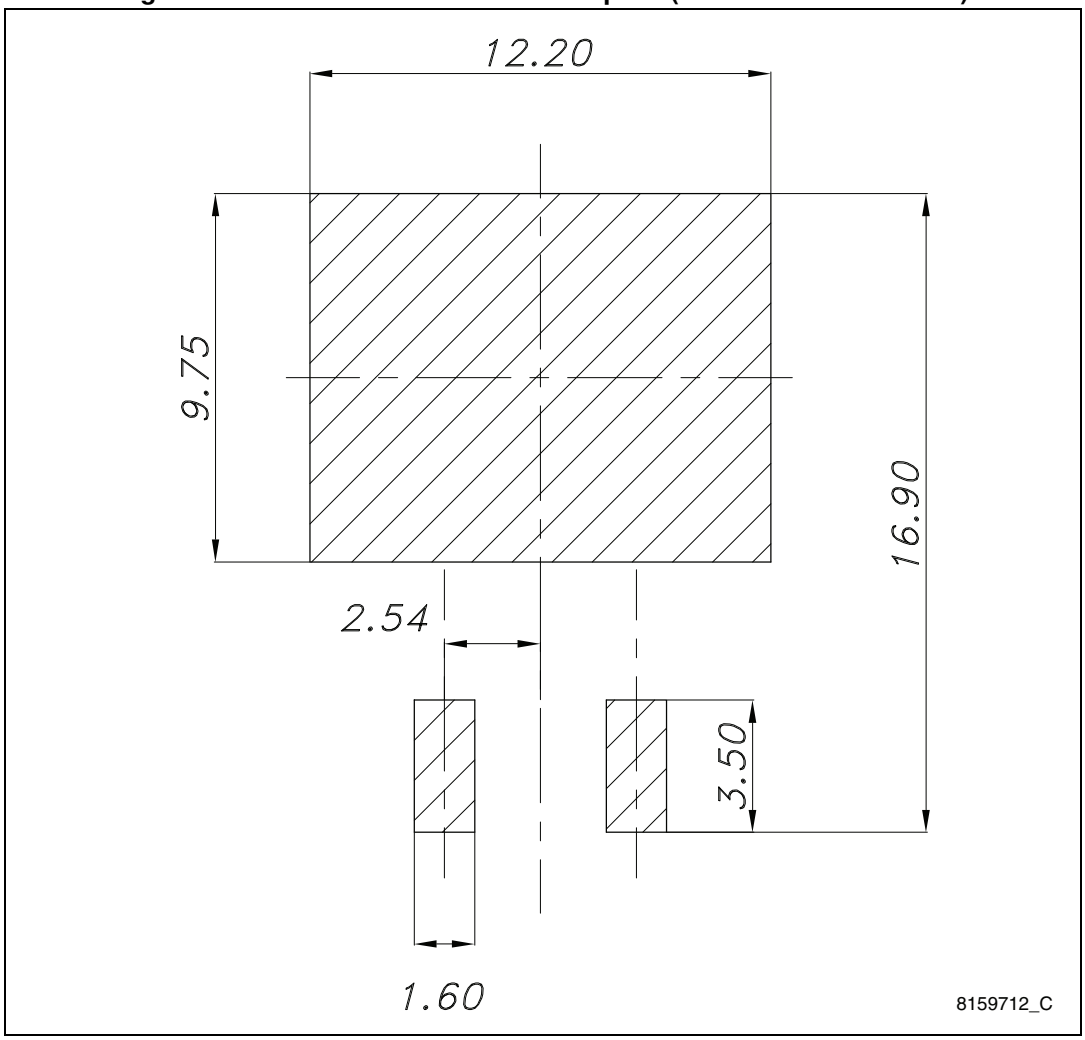


Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 21. H²PAK-2 recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 22. Tape

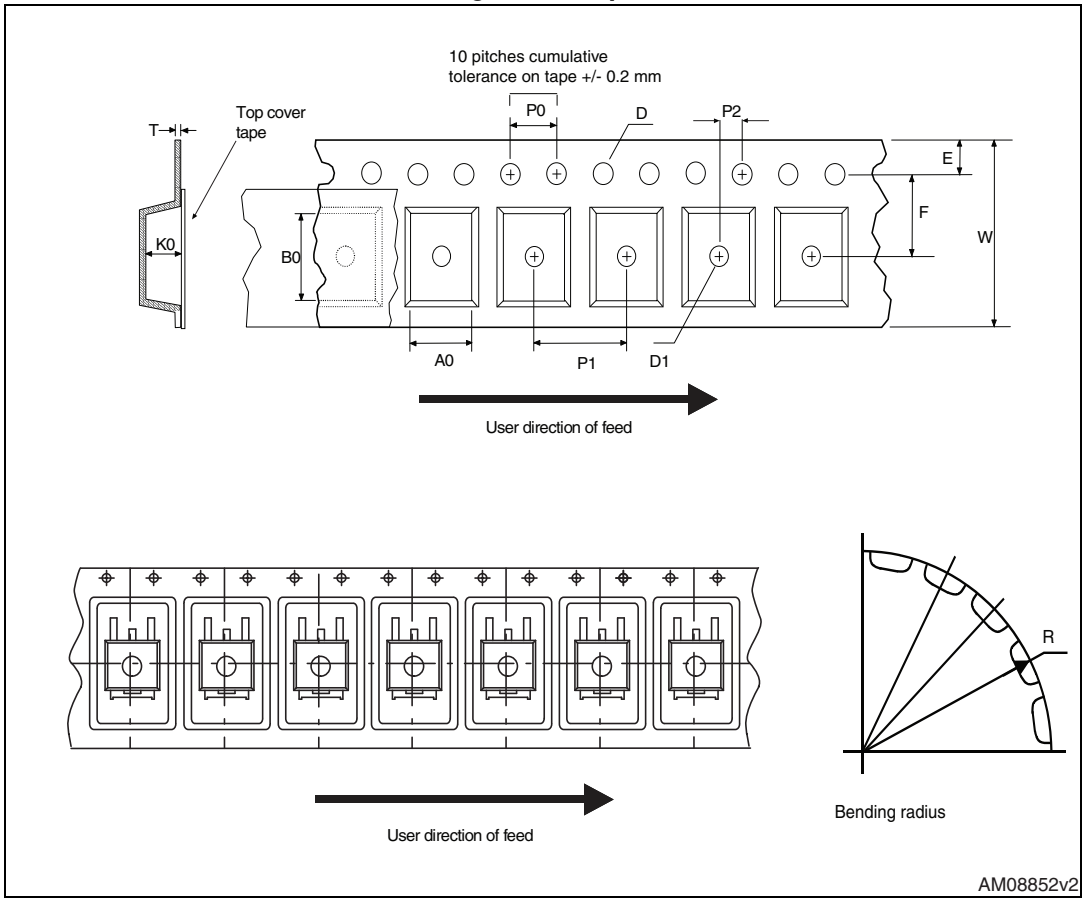


Figure 23. Reel

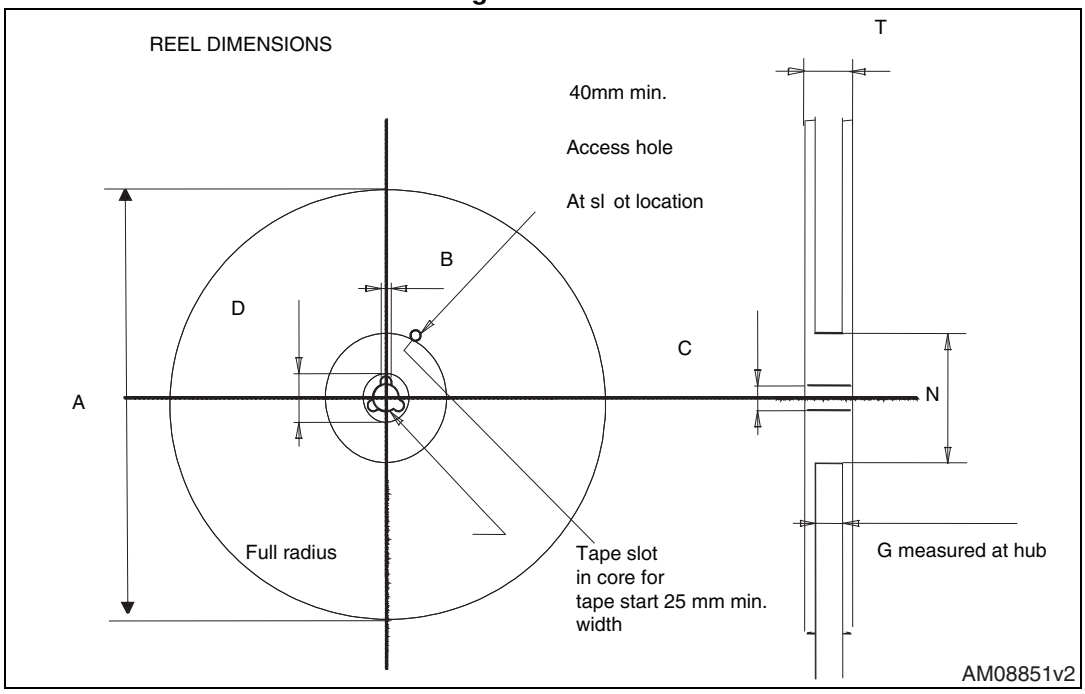


Table 9. H²PAK-2 leads tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Apr-2014	1	First release.

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