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CY14B116L/CY14B116N/CY14B116S
CY14E116L/CY14E116N/CY14E116S

16-Mbit (2048K × 8/1024K × 16/512K × 32) nvSRAM

Features

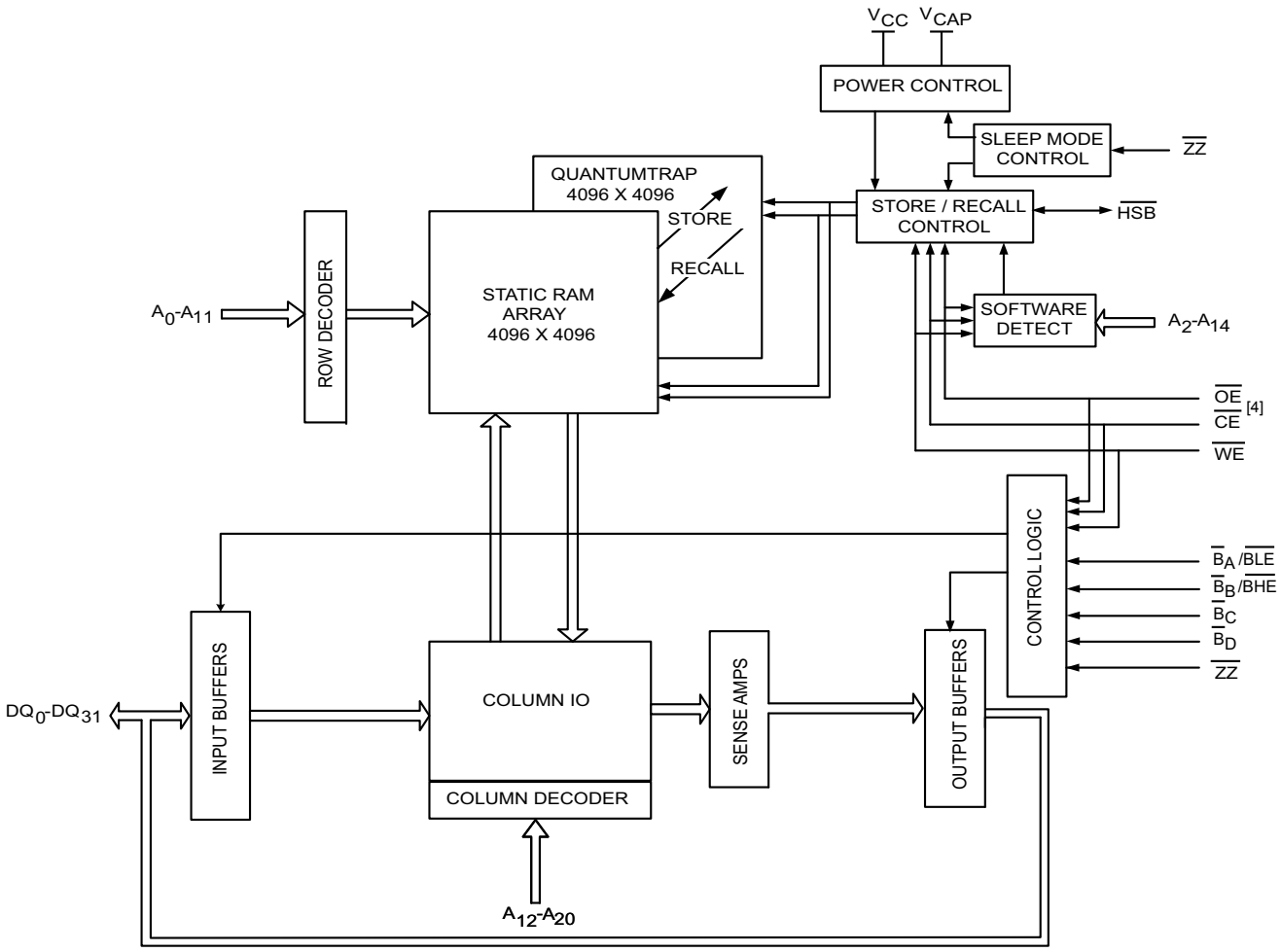
- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - 25-ns, 30-ns and 45-ns access times
  - Internally organized as 2048K × 8 (CY14X116L), 1024K × 16 (CY14X116N), 512K × 32 (CY14X116S)
  - Hands-off automatic STORE on power-down with only a small capacitor
  - STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
  - RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Sleep mode operation
- Low power consumption
  - Active current of 75 mA at 45 ns
  - Standby mode current of 650 μA
  - Sleep mode current of 10 μA
- Operating voltages:
  - CY14B116X: V_{CC} = 2.7 V to 3.6 V
  - CY14E116X: V_{CC} = 4.5 V to 5.5 V
- Industrial temperature: –40 °C to +85 °C
- Packages
  - 44-pin thin small-outline package (TSOP II)
  - 48-pin thin small-outline package (TSOP I)
  - 54-pin thin small-outline package (TSOP II)
  - 60-ball fine-pitch ball grid array (FBGA) package
  - 165-ball fine-pitch ball grid array (FBGA) package
- Restriction of hazardous substances (RoHS) compliant
- Offered speeds
  - 44-pin TSOP II: 25 ns and 45 ns
  - 48-pin TSOP I: 30 ns and 45 ns
  - 54-pin TSOP II: 25 ns and 45 ns
  - 60-ball FBGA: 25 ns
  - 165-ball FBGA: 25 ns and 45 ns

Functional Description

The Cypress CY14X116L/CY14X116N/CY14X116S is a fast SRAM, with a nonvolatile element in each memory cell. The memory is organized as 2048K bytes of 8 bits each or 1024K words of 16 bits each or 512K words of 32 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data residing in the nonvolatile elements do not change when data is written to the SRAM. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related documentation, click here.

Logic Block Diagram[1, 2, 3]



Notes

1. Address A_0–A_{20} for ×8 configuration, address A_0–A_{19} for ×16 configuration and address A_0–A_{18} for ×32 configuration.
2. Data DQ_0–DQ_7 for ×8 configuration, data DQ_0–DQ_{15} for ×16 configuration and data DQ_0–DQ_{31} for ×32 configuration.
3. $\overline{BLE}$, $\overline{BHE}$ are applicable for ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for ×32 configuration only.
4. TSOP II package is offered in single $\overline{CE}$. TSOP I and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

Contents

Pinouts

Figure 1. Pin Diagram: 44-Pin TSOP II (×8)

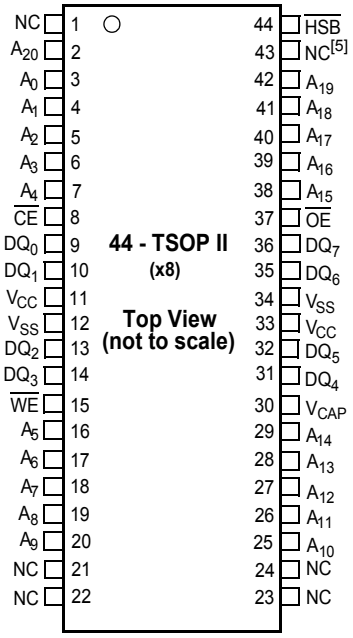


Figure 2. Pin Diagram: 54-Pin TSOP II (×16)

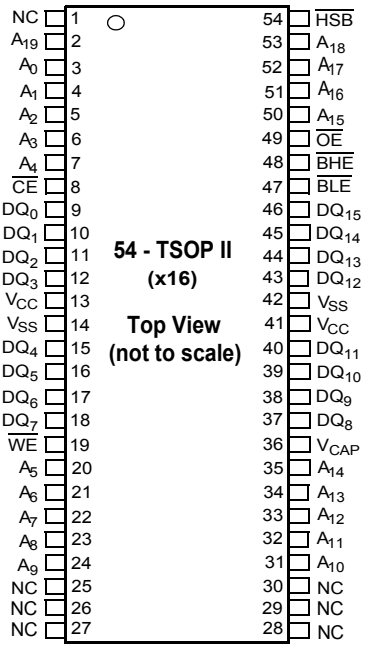
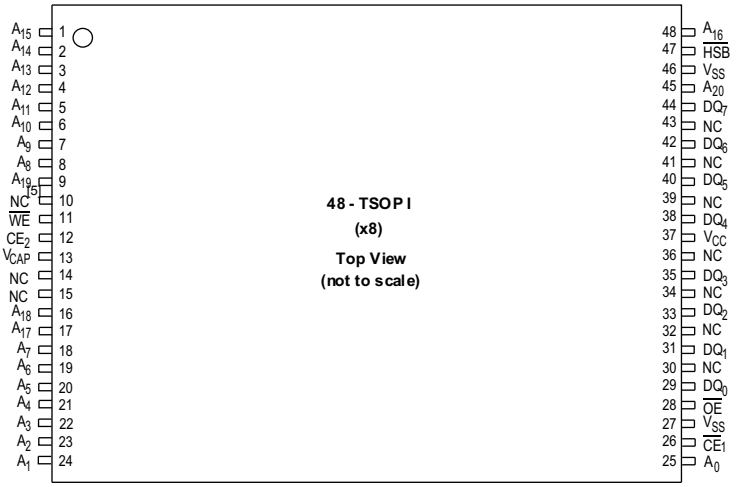


Figure 3. Pin Diagram: 48-Pin TSOP I (×8)



Note
5. Address expansion for 32-Mbit. NC pin not connected to die.

Pinouts (continued)

Figure 4. Pin Diagram: 48-Pin TSOP I (×16)

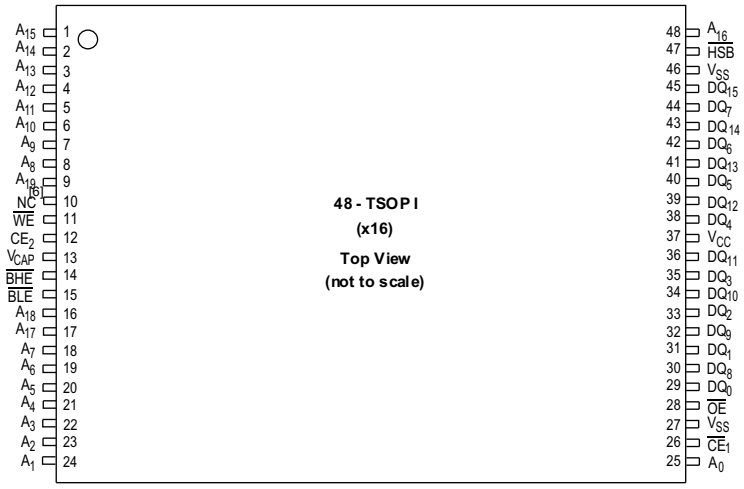
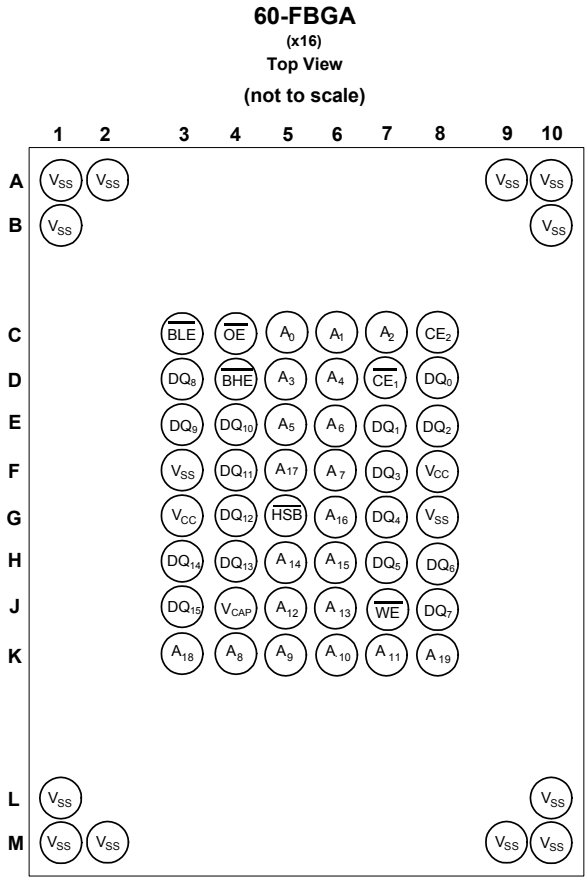


Figure 5. 60-ball FBGA pinout (× 16)



Note
6. Address expansion for 32-Mbit. NC pin not connected to die.

Pinouts (continued)

Figure 6. Pin Diagram: 165-Ball FBGA (×16)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A_6	A_8	$\overline{WE}$	$\overline{BLE}$	$\overline{CE_1}$	NC	$\overline{OE}$	A_5	A_3	NC
B	NC	DQ_0	DQ_1	A_4	$\overline{BHE}$	CE_2	NC	A_2	NC	NC	NC
C	$\overline{ZZ}$	NC	NC	V_{SS}	A_0	A_7	A_1	V_{SS}	NC	DQ_{15}	DQ_{14}
D	NC	DQ_2	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	V_{CAP}	NC	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	NC	DQ_{13}	NC
F	NC	DQ_3	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	DQ_{12}
G	$\overline{HSB}$	NC	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	NC
H	NC	NC	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	NC	NC
J	NC	NC	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	DQ_8	NC
K	NC	NC	DQ_4	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	NC
L	NC	DQ_5	NC	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	NC	NC	DQ_9
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_{10}	NC
N	NC	DQ_6	DQ_7	V_{SS}	A_{11}	A_{10}	A_9	V_{SS}	NC	NC	NC
P	NC	NC	NC	A_{13}	A_{19}	NC	A_{18}	A_{12}	NC	DQ_{11}	NC
R	NC	NC	A_{15}	NC	A_{17}	NC	A_{16}	NC[7]	A_{14}	NC	NC

Figure 7. Pin Diagram: 165-Ball FBGA (×32)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A_6	A_8	$\overline{WE}$	$\overline{B_A}$	$\overline{CE_1}$	$\overline{B_C}$	$\overline{OE}$	A_5	A_3	NC
B	NC	DQ_0	DQ_1	A_4	$\overline{B_B}$	CE_2	$\overline{B_D}$	A_2	NC	NC	DQ_{31}
C	$\overline{ZZ}$	NC	DQ_4	V_{SS}	A_0	A_7	A_1	V_{SS}	NC	DQ_{27}	DQ_{26}
D	NC	DQ_2	DQ_5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ_{30}
E	NC	V_{CAP}	DQ_6	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	NC	DQ_{25}	DQ_{29}
F	NC	DQ_3	DQ_7	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	DQ_{24}
G	$\overline{HSB}$	NC	DQ_{12}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	DQ_{28}
H	NC	NC	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	NC	NC
J	NC	NC	DQ_{13}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	DQ_{20}	DQ_{19}
K	NC	NC	DQ_8	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	DQ_{18}
L	NC	DQ_9	DQ_{14}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	NC	NC	DQ_{21}
M	NC	NC	DQ_{15}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_{22}	DQ_{17}
N	NC	DQ_{10}	DQ_{11}	V_{SS}	A_{11}	A_{10}	A_9	V_{SS}	NC	NC	DQ_{16}
P	NC	NC	NC	A_{13}	NC	NC	A_{18}	A_{12}	NC	DQ_{23}	NC
R	NC	NC	A_{15}	NC	A_{17}	NC	A_{16}	NC[7]	A_{14}	NC	NC

Note
7. Address expansion for 32-Mbit. NC pin not connected to die.

Pin Definitions

Pin Name	I/O Type	Description
$A_0 – A_{20}$	Input	Address inputs. Used to select one of the 2,097,152 bytes of the nvSRAM for the ×8 configuration.
$A_0 – A_{19}$		Address inputs. Used to select one of the 1,048,576 words of the nvSRAM for the ×16 configuration.
$A_0 – A_{18}$		Address inputs. Used to select one of the 524,288 words of the nvSRAM for the ×32 configuration.
$DQ_0 – DQ_7$	Input/Output	**Bidirectional data I/O lines for the ×8 configuration**. Used as input or output lines depending on operation.
$DQ_0 – DQ_{15}$		**Bidirectional data I/O lines for the ×16 configuration**. Used as input or output lines depending on operation.
$DQ_0 – DQ_{31}$		**Bidirectional data I/O lines for ×32 configuration**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable input, Active LOW**. When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	**Chip Enable input in TSOP II package, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{CE}_1$, CE_2		**Chip Enable input in FBGA package.** The device is selected and a memory access begins on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH) or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW).
$\overline{OE}$	Input	**Output Enable, Active LOW.** The Active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
$\overline{BLE}/\overline{B}_A$[8]	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_7–DQ_0.
$\overline{BHE}/\overline{B}_B$[8]	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_{15}–DQ_8.
$\overline{B}_C$[8]	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_{23}–DQ_{16}.
$\overline{B}_D$[8]	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_{31}–DQ_{24}.
$\overline{ZZ}$[9]	Input	**Sleep Mode Enable.** When the $\overline{ZZ}$ pin is pulled LOW, the device enters a low-power Sleep mode and consumes the lowest power. Since this input is logically AND'ed with $\overline{CE}$, $\overline{ZZ}$ must be HIGH for normal operation.
V_{CC}	Power Supply	**Power supply inputs to the device**.
V_{SS}	Power Supply	**Ground for the device**. Must be connected to ground of the system.
$\overline{HSB}$	Input/Output	**Hardware STORE Busy ($\overline{HSB}$)**.When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power Supply	**AutoStore capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	NC	**No Connect**. Die pads are not connected to the package pin.

Notes
8. $\overline{BLE}$, $\overline{BHE}$ are applicable for ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for ×32 configuration only.
9. Sleep mode feature is offered in 165-ball FBGA package only.

Device Operation

The CY14X116L/CY14X116N/CY14X116S nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) automatically at power-down, or from the nonvolatile cell to the SRAM (the RECALL operation) on power-up. Both the STORE and RECALL operations are also available under software control. Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14X116L/CY14X116N/CY14X116S supports infinite reads and writes to the SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the Truth Table For SRAM Operations on page 24 for a complete description of read and write modes.

SRAM Read

The CY14X116L/CY14X116N/CY14X116S performs a read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$, $\overline{ZZ}$, and $\overline{HSB}$ are HIGH. The address specified on pins A_0–A_{20} or A_0–A_{19} or A_0–A_{18} determines which of the 2,097,152 data bytes or 1,048,576 words of 16 bits or 524,288 words of 32 bits each are accessed. Byte enables ($\overline{BLE}$, $\overline{BHE}$) determine which bytes are enabled to the output, in the case of 16-bit words and byte enables ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$) determine which bytes are enabled to the output, in the case of 32-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_0–DQ_{31} is written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. The Byte Enable inputs ($\overline{BLE}$, $\overline{BHE}$ determine which bytes are written, in the case of 16-bit words and Byte Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$) determine which bytes are written, in the case of 32-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on the common I/O lines. If $\overline{OE}$ is left LOW, the internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation (Power-Down)

The CY14X116L/CY14X116N/CY14X116S stores data to the nonvolatile QuantumTrap cells using one of the three storage operations. These three operations are: Hardware STORE, activated by the $\overline{HSB}$; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of nvSRAM and is enabled by default on the CY14X116L/CY14X116N/CY14X116S.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and a STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to the V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in the section Preventing AutoStore on page 12. If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM.

Figure 8. AutoStore Mode

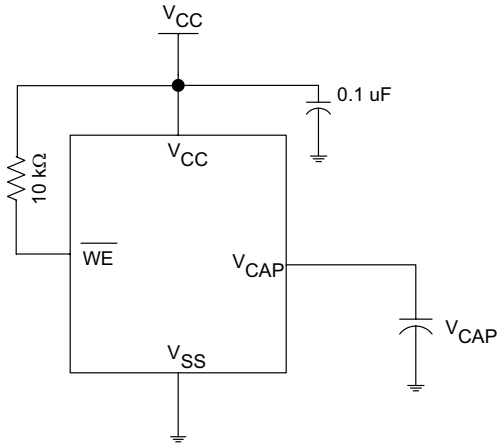


Figure 8 shows the proper connection of the storage capacitor (V_{CAP}) for the automatic STORE operation. Refer to DC Electrical Characteristics on page 13 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{VCAP} by a regulator on the chip. A pull-up resistor should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up resistor is only effective if the $\overline{WE}$ signal is in tristate during power-up. When the nvSRAM comes out of power-up-RECALL, the host microcontroller must be active or the $\overline{WE}$ held inactive until the host microcontroller comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place (which sets a write latch) since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

Hardware STORE ($\overline{HSB}$) Operation

The CY14X116L/CY14X116N/CY14X116S provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. The $\overline{HSB}$ pin is used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the device conditionally initiates a STORE operation after t_{DELAY}. A STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (an internal 100-kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100-kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. If the write latch is not set, $\overline{HSB}$ is not driven LOW by the device. However, any of the SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by the host microcontroller or another external source.

During any STORE operation, regardless of how it is initiated, the device continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up or after any low-power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power-up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the $\overline{HSB}$ pin is driven LOW by the $\overline{HSB}$ driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. A Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle, the previous nonvolatile data is first erased, followed by a store into the nonvolatile elements. After a STORE cycle is initiated, further reads and writes are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Otherwise, the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$-controlled reads or $\overline{OE}$-controlled reads, with $\overline{WE}$ kept HIGH for all the six read sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. $\overline{HSB}$ is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, perform the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Sleep Mode

In Sleep mode, the device consumes the lowest power supply current (I_{ZZ}). The device enters a low-power Sleep mode after asserting the $\overline{ZZ}$ pin LOW. After the Sleep mode is registered, the nvSRAM does a STORE operation to secure the data to the nonvolatile memory and then enters the low-power mode. The device starts consuming I_{ZZ} current after t_{SLEEP} time from the instance when the sleep mode is initiated. When the $\overline{ZZ}$ pin is LOW, all input pins are ignored except the $\overline{ZZ}$ pin. The nvSRAM is not accessible for normal operations while it is in sleep mode.

When the $\overline{ZZ}$ pin is de-asserted (HIGH), there is a delay t_{WAKE} before the user can access the device. If sleep mode is not used, the $\overline{ZZ}$ pin should be tied to V_{CC}.

Note When nvSRAM enters sleep mode, it initiates a nonvolatile STORE cycle, which results in losing one endurance cycle for every Sleep mode entry unless data has not been written to the nvSRAM since the last nonvolatile STORE/RECALL operation.

Note If the $\overline{ZZ}$ pin is LOW during power-up, the device will not be in Sleep mode. However, the I/Os are in tristate until the $\overline{ZZ}$ pin is de-asserted (HIGH).

Figure 9. Sleep Mode ($\overline{ZZ}$) Flow Diagram

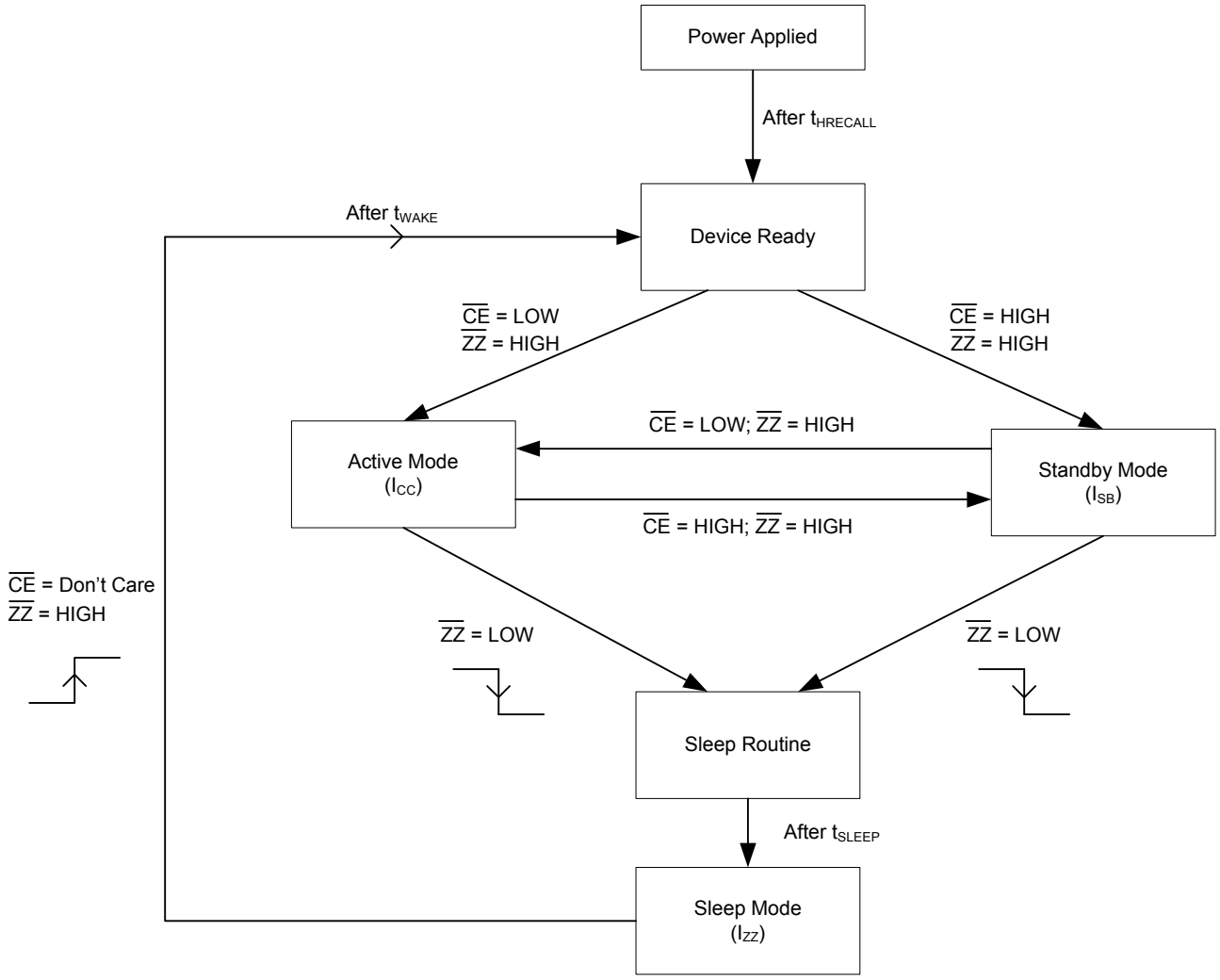


Table 1. Mode Selection

$\overline{CE}$[10]	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$, $\overline{BHE}$ / $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$[11]	A_{15} - A_0[12]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[13]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[13]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[13]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[13]

Notes

10. The TSOP II package is offered in single $\overline{CE}$. TSOP I, and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
11. $\overline{BLE}$, $\overline{BHE}$ are applicable for the ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for the ×32 configuration only.
12. While there are 21 address lines on the CY14X116L (20 address lines on the CY14X116N and 19 address lines on the CY14X116S), only 13 address lines (A_{14}–A_2) are used to control software modes. The remaining address lines are don't care.
13. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile operation.

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual software STORE operation must be performed to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Data Protection

The CY14X116L/CY14X116N/CY14X116S protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and write operations. The low-voltage condition is detected when V_{CC} is less than $V_{SWITCH.}$ If the CY14X116L/CY14X116N/CY14X116S is in a write mode at power-up (both $\overline{CE}$ and $\overline{WE}$ are LOW), after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} ($\overline{HSB}$ to output active). This protects against inadvertent writes during power-up or brownout conditions.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS}

CY14B116X: .....–0.5 V to +4.1 V

CY14E116X: .....–0.5 V to +7.0 V

Voltage applied to outputs in high-Z state.....–0.5 V to V_{CC} + 0.5 V

Input voltage .....–0.5 V to Vcc + 0.5 V

Transient voltage (<20 ns) on any pin to ground potential .....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 Seconds)..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Product	Range	Ambient Temperature (T_A)	V_{CC}
CY14B116X	Industrial	–40 °C to +85 °C	2.7 V to 3.6 V
CY14E116X			4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ[14]	Max	Unit
V_{CC}	Power supply		CY14B116X	2.7	3.0	3.6	V
			CY14E116X	4.5	5.0	5.5	V
I_{CC1}	Average V_{CC} current	Values obtained without output loads (I_{OUT} = 0 mA)	t_{RC} = 25/30 ns	–	–	95	mA
			t_{RC} = 45 ns	–	–	75	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = V_{CC} (max). Average current for duration t_{STORE}		–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, V_{CC} (Typ), 25 °C	All inputs cycling at CMOS Levels. Values obtained without output loads (I_{OUT} = 0 mA).		–	50	–	mA
I_{CC4}[15]	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	6	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CC} - 0.2\ V)$. $V_{IN} \leq 0.2$ V or $\geq (V_{CC} - 0.2\ V)$. 'Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	t_{RC} = 25/30 ns	–	–	650	µA
			t_{RC} = 45 ns	–	–	500	µA
I_{ZZ}	Sleep mode current	All inputs are static at CMOS Level		–	–	10	µA
I_{IX}[16]	Input leakage current (except $\overline{HSB}$)	V_{CC} = V_{CC} (max), $V_{SS} \leq V_{IN} \leq V_{CC}$		–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = V_{CC} (max), $V_{SS} \leq V_{IN} \leq V_{CC}$		–100	–	+1	µA

Notes

14. Typical values are at 25 °C, V_{CC} = V_{CC}(Typ). Not 100% tested.
15. This parameter is only guaranteed by design and is not tested.
16. The $\overline{HSB}$ pin has I_{OUT} = -2 uA for V_{OH} of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ[14]	Max	Unit
I_{OZ}	Off state output leakage current	$V_{CC} = V_{CC}(Max)$, $V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{CE}$ or $\overline{OE} \ge V_{IH}$ or $\overline{BLE}$, $\overline{BHE}/\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D} \ge V_{IH}$ or $\overline{WE} \le V_{IL}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}[17]	Storage capacitor	Between V_{CAP} pin and V_{SS}	19.8	22.0	82.0	µF
V_{VCAP}[18, 19]	Maximum voltage driven on V_{CAP} pin by the device	$V_{CC} = V_{CC}$ (max)	–	–	5.0	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000,000	Cycles

Capacitance

In the following table, the capacitance parameters are listed. [19]

Parameter	Description	Test Conditions	Max (All packages except 60-FBGA and 165-FBGA)	Max (60-FBGA package and 165-FBGA package)	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC}$ (Typ)	8	10	pF
C_{IO}	Input/Output capacitance		8	10	pF
C_{OUT}	Output capacitance		8	10	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed.[19]

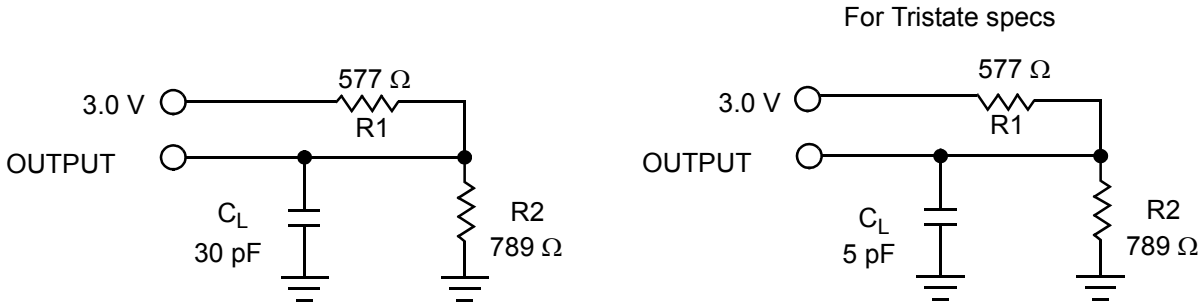
Parameter	Description	Test Conditions	44-TSOP II	48-TSOP I	54-TSOP II	60-FBGA	165-FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	44.6	35.6	41.1	21	15.6	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.4	2.33	4.6	3	2.9	°C/W

Notes

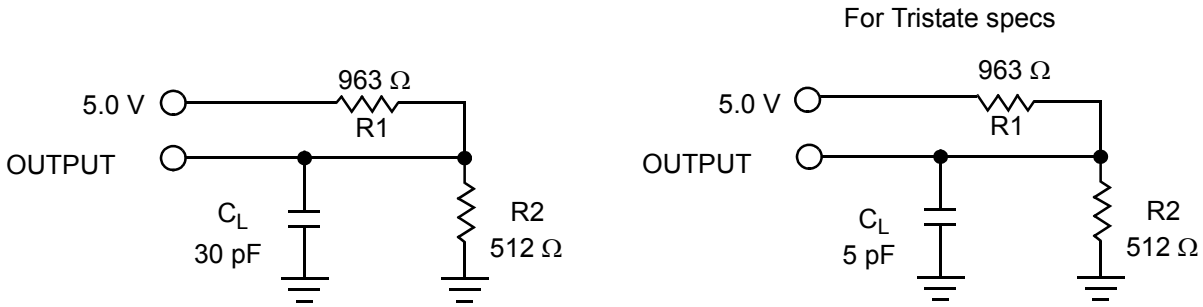
17. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits.
18. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage
19. These parameters are only guaranteed by design and are not tested.

Figure 10. AC Test Loads and Waveforms

For 3 V (CY14B116X):



For 5 V (CY14E116X):



AC Test Conditions

	CY14B116X	CY14E116X
Input pulse levels	0 V to 3 V	0 V to 3 V
Input rise and fall times (10%–90%)	≤3 ns	≤3 ns
Input and output timing reference levels	1.5 V	1.5 V

AC Switching Characteristics

Over the Operating Range[20]

Parameters		Description	25 ns		30 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip enable access time	–	25	–	30	–	45	ns
t_{RC} [22]	t_{RC}	Read cycle time	25	–	30	–	45	-	ns
t_{AA} [23]	t_{AA}	Address access time	–	25	–	30	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	12	–	14	–	20	ns
t_{OHA} [23]	t_{OH}	Output hold after address change	3	–	3	–	3	–	ns
t_{LZCE} [24]	t_{LZ}	Chip enable to output active	3	–	3	–	3	–	ns
t_{HZCE} [21, 24]	t_{HZ}	Chip disable to output inactive	–	10	–	12	–	15	ns
t_{LZOE} [24]	t_{OLZ}	Output enable to output active	0	–	0	–	0	–	ns
t_{HZOE} [21, 24]	t_{OHZ}	Output disable to output inactive	–	10	–	12	–	15	ns
t_{PU} [24]	t_{PA}	Chip enable to power active	0	–	0	–	0	–	ns
t_{PD} [24]	t_{PS}	Chip disable to power standby	–	25	–	30	–	45	ns
t_{DBE}		Byte enable to data valid	–	12	–	14	–	20	ns
t_{LZBE} [24]		Byte enable to output active	0	–	0	–	0	–	ns
t_{HZBE} [21, 24]		Byte disable to output inactive	–	10	–	12	–	15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write cycle time	25	–	30	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	20	–	24	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	20	–	24	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	10	–	14	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	20	–	24	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	0	–	ns
t_{HZWE} [21, 24, 25]	t_{WZ}	Write enable to output disable	–	10	–	12	-	15	ns
t_{LZWE} [24]	t_{OW}	Output active after end of write	3	–	3	–	3	–	ns
t_{BW}		Byte enable to end of write	20	–	24	–	30	–	ns

Notes

20. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC}(Typ), and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as shown in Figure 10.
21. t_{HZCE}, t_{HZOE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF. Transition is measured ±200 mV from the steady state output voltage.
22. $\overline{WE}$ must be HIGH during SRAM read cycles.
23. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}/\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ LOW.
24. These parameters are only guaranteed by design and are not tested.
25. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.

Figure 11. SRAM Read Cycle 1: Address Controlled[26, 27, 28]

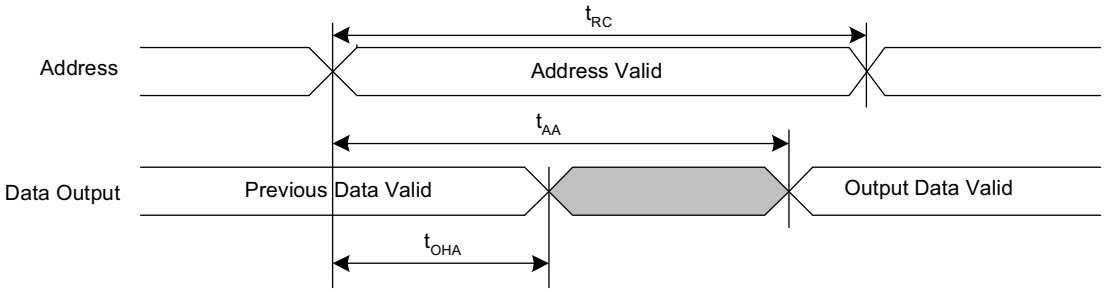
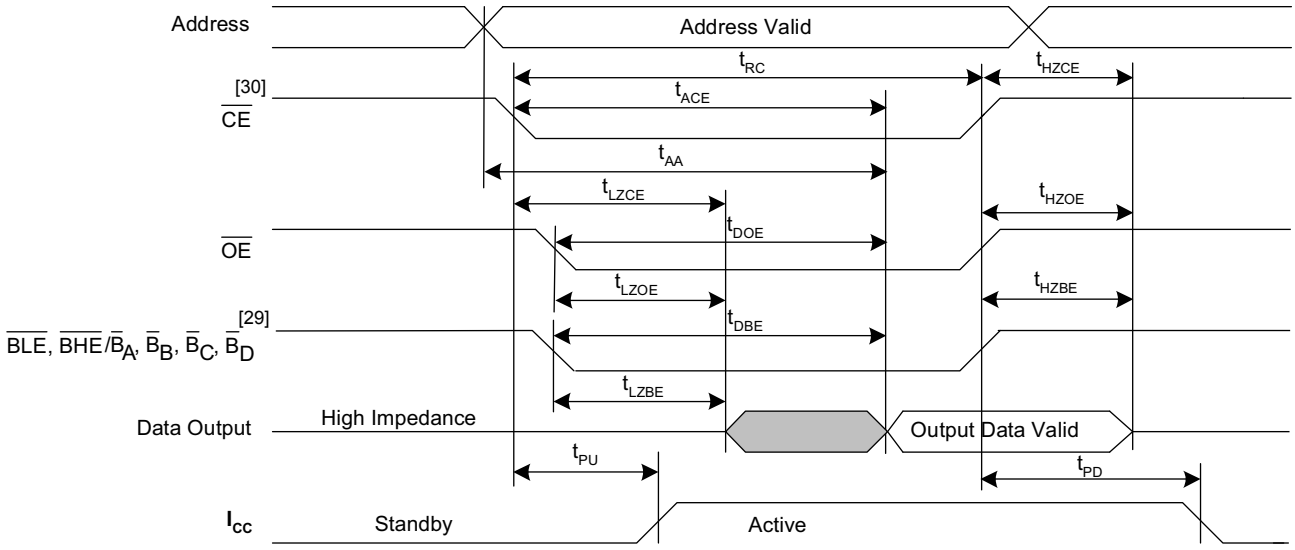


Figure 12. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled[26, 28]



Notes

26. $\overline{WE}$ must be HIGH during SRAM read cycles.
27. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}/\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ LOW.
28. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
29. $\overline{BLE}$, $\overline{BHE}$ are applicable for the ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for the ×32 configuration only.
30. TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).

Figure 13. SRAM Write Cycle 1: $\overline{WE}$ Controlled[32, 34, 36]

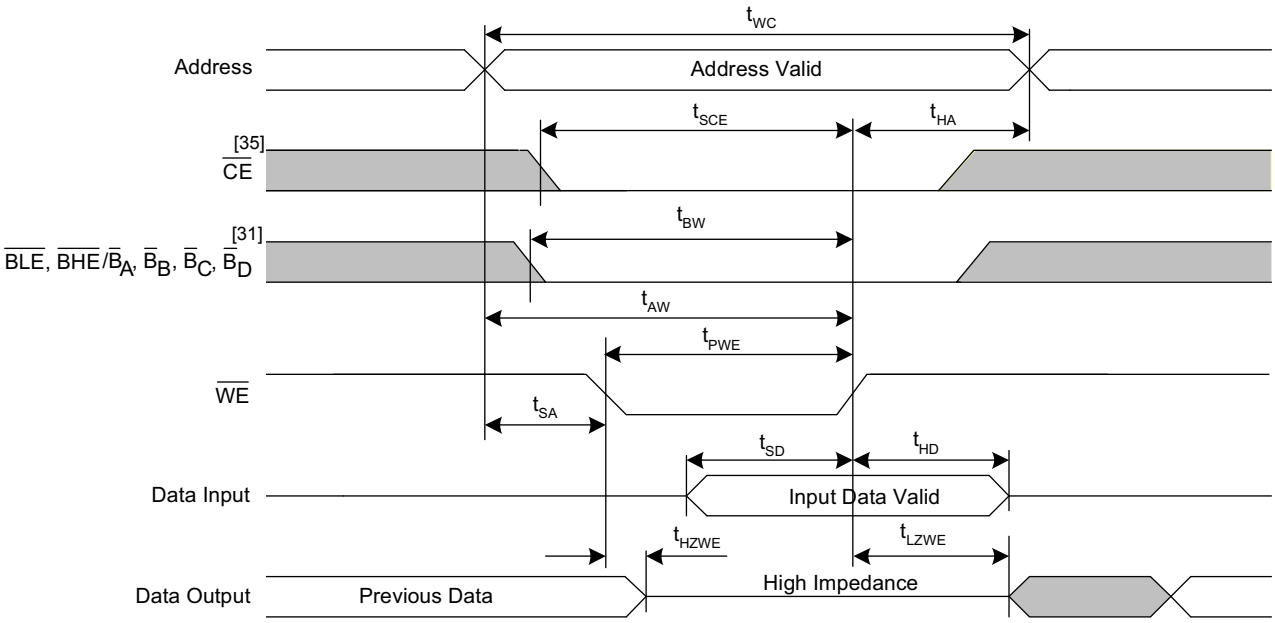
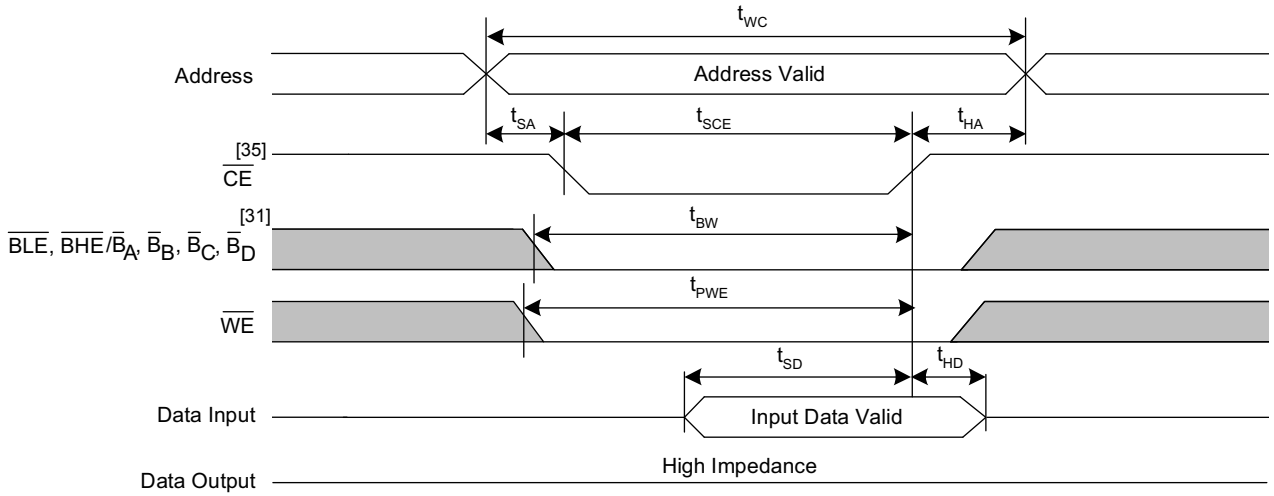


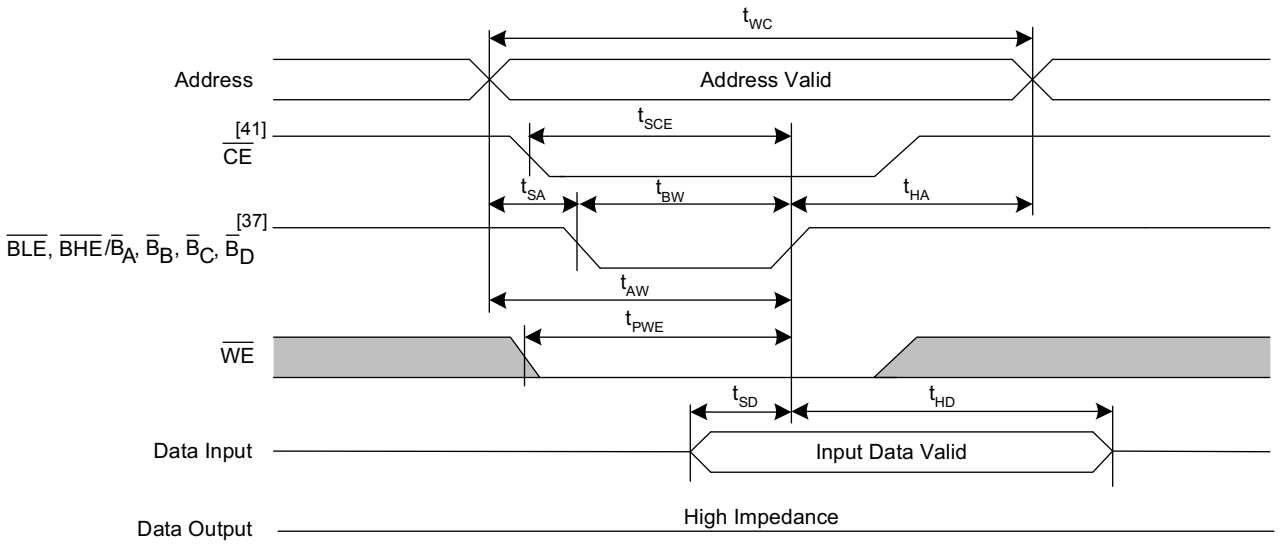
Figure 14. SRAM Write Cycle 2: $\overline{CE}$ Controlled[32, 34, 36]



Notes

31. $\overline{BLE}$, $\overline{BHE}$ are applicable for the ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for the ×32 configuration only.
32. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
33. $\overline{WE}$ must be HIGH during SRAM read cycles.
34. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
35. TSOP II package is offered in single $\overline{CE}$. TSOP I and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
36. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

Figure 15. SRAM Write Cycle 3: $\overline{BHE}$, $\overline{BLE}$/ $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$Controlled[38, 39, 40]



Notes

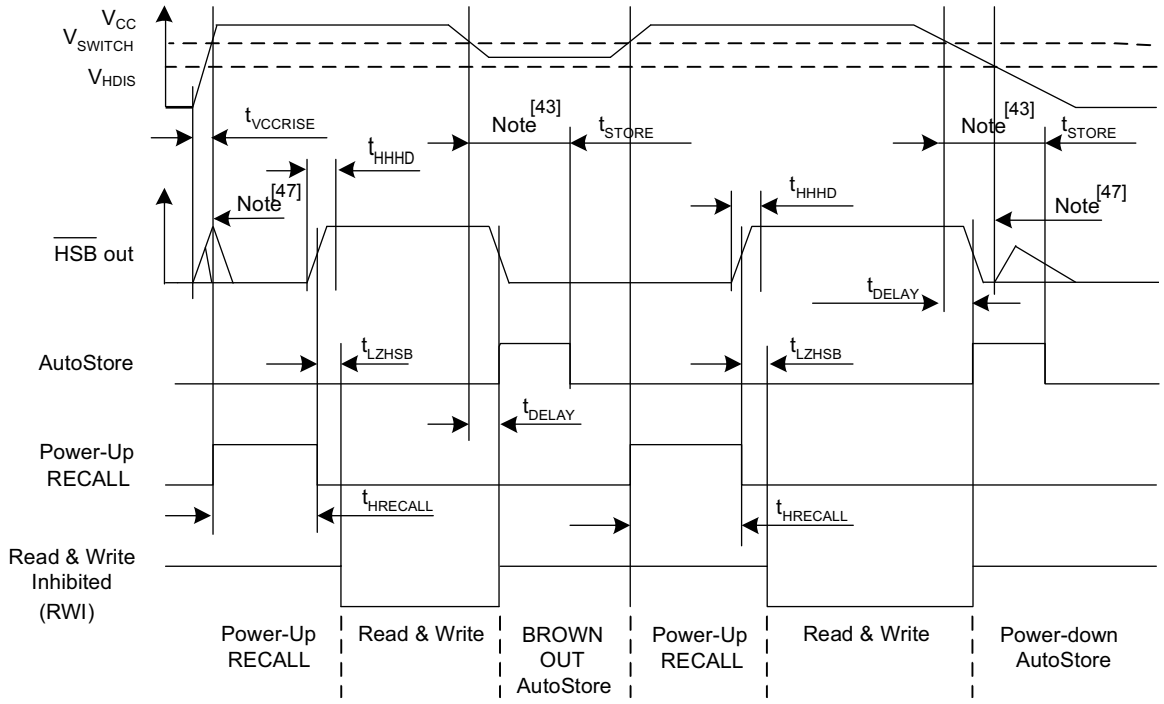
37. $\overline{BLE}$, $\overline{BHE}$ are applicable for the ×16 configuration and $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$ are applicable for the ×32 configuration only.
38. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
39. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
40. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.
41. TSOP II package is offered in single $\overline{CE}$. TSOP I and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).

AutoStore/Power-Up RECALL Characteristics

Over the Operating Range

Parameter	Description		Min	Max	Unit
$t_{HRECALL}$ [42]	Power-Up RECALL duration		–	30	ms
t_{STORE} [43]	STORE cycle duration		–	8	ms
t_{DELAY} [44, 45]	Time allowed to complete SRAM write cycle		–	25	ns
V_{SWITCH}	Low-voltage trigger level	CY14B116X	–	2.65	V
		CY14E116X	–	4.40	V
$t_{VCCRISE}$[45]	V_{CC} rise time		150	–	µs
V_{HDIS}[45]	$\overline{HSB}$ output disable voltage		–	1.9	V
t_{LZHSB}[45]	$\overline{HSB}$ to output active time		–	5	µs
t_{HHHD}[45]	$\overline{HSB}$ HIGH active time		–	500	ns

Figure 16. AutoStore or Power-Up RECALL[46]



Notes

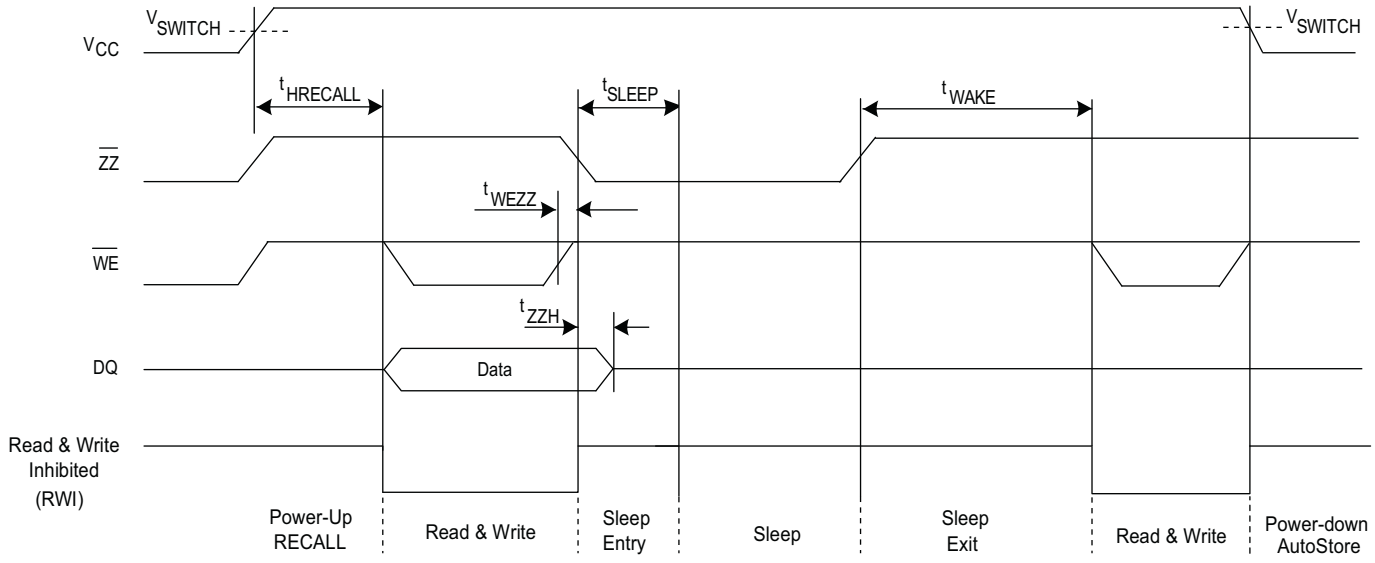
42. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
43. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
44. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
45. These parameters are only guaranteed by design and are not tested.
46. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
47. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Sleep Mode Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{WAKE}	Sleep mode exit time ($\overline{ZZ}$ HIGH to first access after wakeup)	–	30	ms
t_{SLEEP}	Sleep mode enter time ($\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	8	ms
t_{ZZL}	$\overline{ZZ}$ active LOW time	50	–	ns
t_{WEZZ}	Last write to sleep mode entry time	0	–	µs
t_{ZZH}	$\overline{ZZ}$ active to DQ Hi-Z time	–	70	ns

Figure 17. Sleep Mode[48]



Note
48. Device initiates sleep routine and enters into Sleep mode after t_{SLEEP} duration.

Software Controlled STORE and RECALL Characteristics

Over the Operating Range[49, 50]

Parameter	Description	25 ns		30 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	25	–	30	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	0	–	ns
t_{CW}	Clock pulse width	20	–	24	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	600	–	600	–	600	µs
t_{SS} [51, 52]	Soft sequence processing time	–	500	–	500	–	500	µs

Figure 18. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE and RECALL Cycle[50]

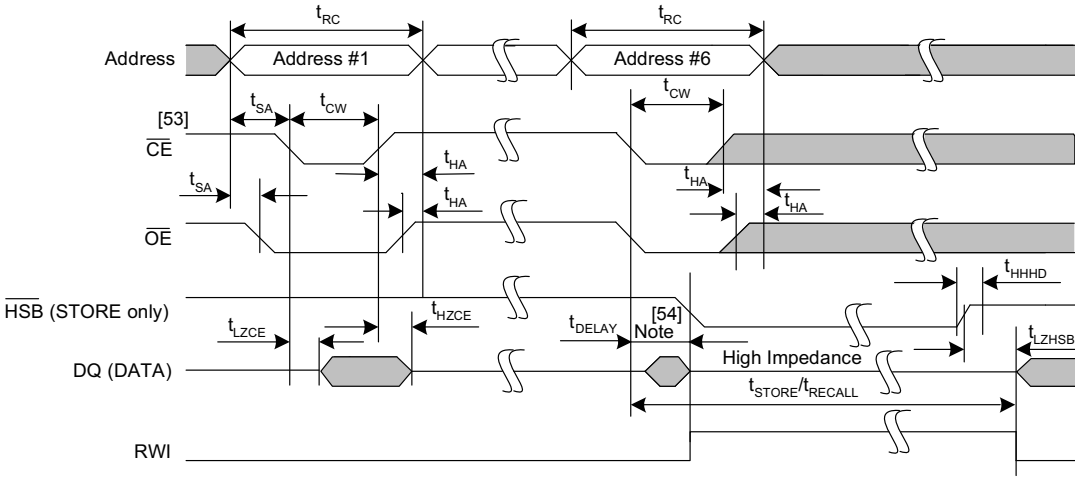
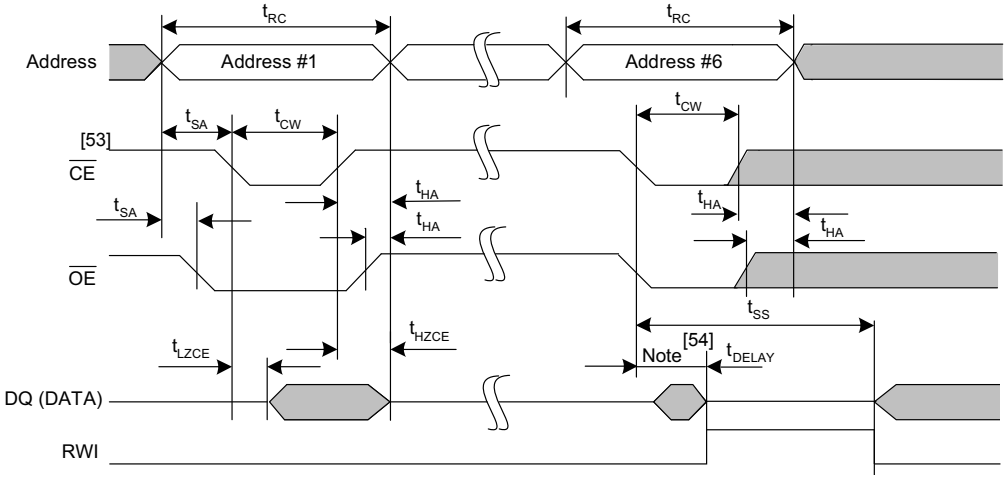


Figure 19. AutoStore Enable and Disable Cycle



Notes

49. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
50. The six consecutive addresses must be read in the order listed in Table 1. $\overline{WE}$ must be HIGH during all six consecutive cycles.
51. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
52. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
53. TSOP II package is offered in single $\overline{CE}$. TSOP I and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
54. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Characteristics

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Figure 20. Hardware STORE Cycle[55]

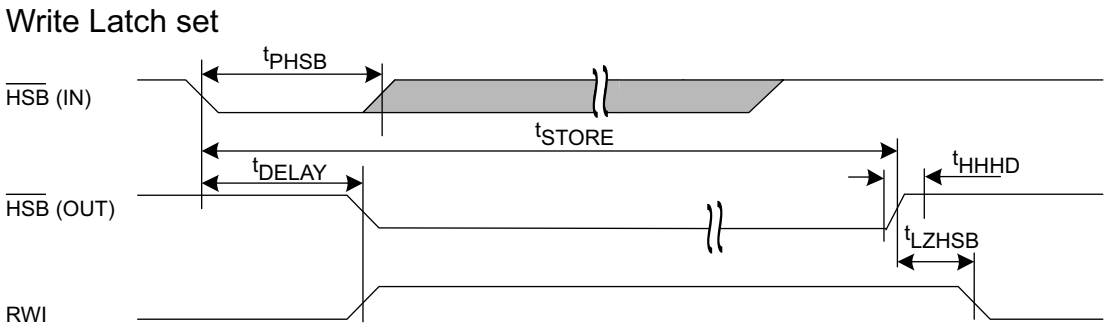
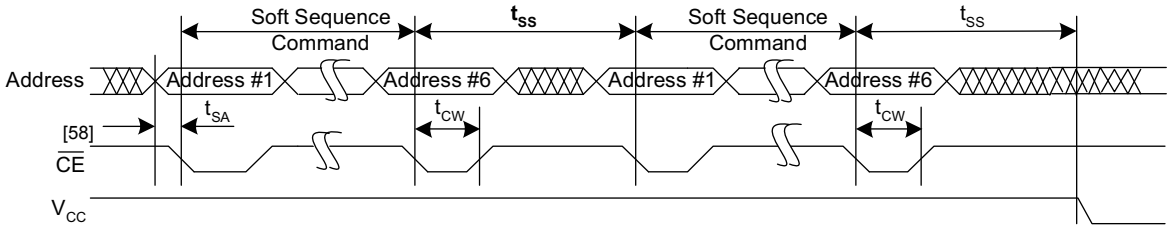


Figure 21. Soft Sequence Processing[56, 57]



Notes

55. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
56. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register command.
57. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
58. TSOP II package is offered in single $\overline{CE}$. TSOP I and BGA packages are offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

For ×8 Configuration

Single chip enable option (44-pin TSOP II package)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs and Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ_0–DQ_7)	Read	Active
L	H	H	High-Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7)	Write	Active

For ×8 Configuration

Dual chip enable option (48-pin TSOP I package)

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs and Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	High-Z	Deselect/Power-down	Standby
L	H	H	L	Data out (DQ_0–DQ_7)	Read	Active
L	H	H	H	High-Z	Output disabled	Active
L	H	L	X	Data in (DQ_0–DQ_7)	Write	Active

For ×16 Configuration

Single chip enable option (54-pin TSOP II package)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	X	X	H	H	High-Z	Output disabled	Active
L	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	L	L	H	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	L	H	L	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	X	X	High-Z	Output disabled	Active
L	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	L	X	L	H	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	L	X	H	L	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

For ×16 Configuration

Dual chip enable option (48-pin TSOP I package and 165-ball FBGA package)

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	H	X	X	H	H	High-Z	Output disabled	Active
L	H	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	H	L	L	H	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	H	L	H	L	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	H	X	X	High-Z	Output disabled	Active
L	H	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	H	L	X	L	H	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	H	L	X	H	L	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

For ×32 Configuration

Dual chip enable option (165-ball FBGA package)

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	DQ_0–DQ_7	DQ_8–DQ_{15}	DQ_{16}–DQ_{23}	DQ_{24}–DQ_{31}	Mode	Power
H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	deselect/ Power down	Standby
X	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	deselect/ Power down	Standby
L	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected	Active
L	H	H	L	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	Active
L	H	H	L	L	H	H	H	Data out	High-Z	High-Z	High-Z	Read	Active
L	H	H	L	H	L	H	H	High-Z	Data out	High-Z	High-Z	Read	Active
L	H	H	L	H	H	L	H	High-Z	High-Z	Data out	High-Z	Read	Active
L	H	H	L	H	H	H	L	High-Z	High-Z	High-Z	Data out	Read	Active
L	H	L	X	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	Active
L	H	L	X	L	H	H	H	Data in	High-Z	High-Z	High-Z	Write	Active
L	H	L	X	H	L	H	H	High-Z	Data in	High-Z	High-Z	Write	Active
L	H	L	X	H	H	L	H	High-Z	High-Z	Data in	High-Z	Write	Active
L	H	L	X	H	H	H	L	High-Z	High-Z	High-Z	Data in	Write	Active
L	H	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Output disabled	Active