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Quad channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	140 mΩ
Current limitation (typ)	I_{LIMH}	12 A
Stand-by current (max)	I_{STBY}	0.5 μA

- General
 - Quad channel smart high-side driver with MultiSense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
 - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation
 - Self limiting of fast thermal transients

- Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
- Loss of ground and loss of V_{CC}
- Reverse battery with external components
- Electrostatic discharge protection

Applications

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps (up to R10W or LED Real Combinations)

Description

The VNQ7140AJ-E is a quad channel high-side driver manufactured using ST proprietary VIPower® technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{FaultRST}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices

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1 Block diagram and pin description

Figure 1. Block diagram

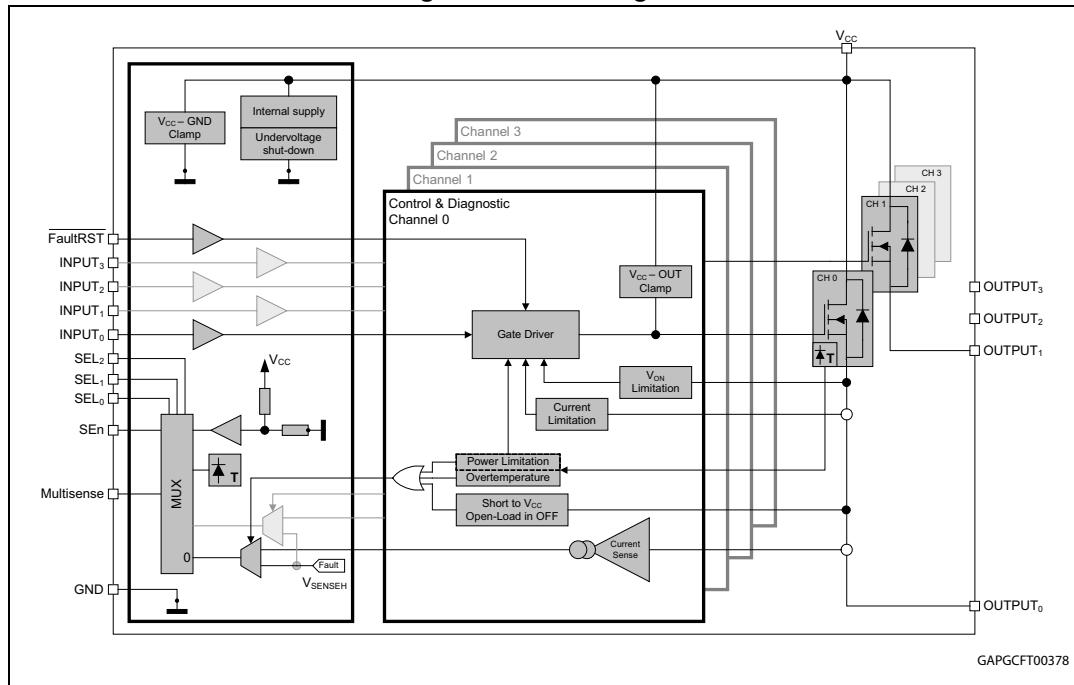
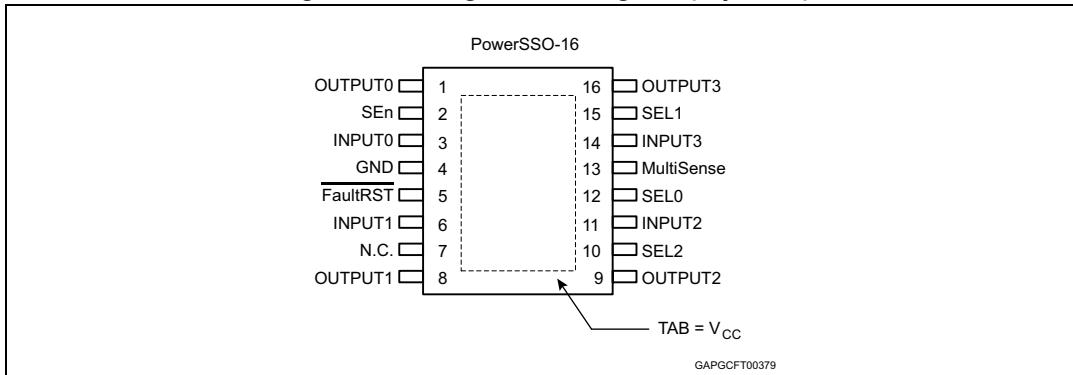


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1,2}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

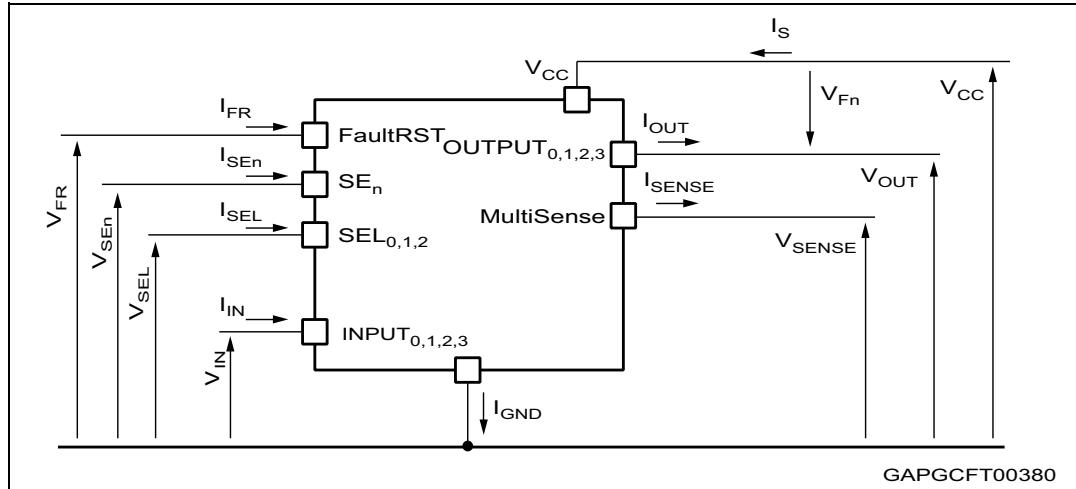
Figure 2. Configuration diagram (top view)**Table 2. Suggested connections for unused and not connected pins**

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELxFaultRST
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40V; $R_L = 4 \Omega$)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1,2,3}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	4	
I_{IN}	$INPUT_{0,1,2,3}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1,2} DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	MultiSense pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150$ °C)	10	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	– INPUT _{0,1,2,3}	4000	V
	– MultiSense	2000	V
	– SEn, SEL _{0,1,2} , FaultRST	4000	V
	– OUTPUT _{0,1,2,3}	4000	V
	– V_{CC}	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾	7.7	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾	61	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	26.8	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB.
3. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace.

2.3 Main electrical characteristics

$7 \text{ V} < V_{CC} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified.

All typical values refer to $V_{CC} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDHyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance ⁽¹⁾	$I_{OUT} = 1 \text{ A}; T_j = 25^\circ\text{C}$	140			$\text{m}\Omega$
		$I_{OUT} = 1 \text{ A}; T_j = 150^\circ\text{C}$			280	
		$I_{OUT} = 1 \text{ A}; V_{CC} = 4 \text{ V}; T_j = 25^\circ\text{C}$			210	
V_{clamp}	Clamp voltage	$I_S = 20 \text{ mA}; T_j = -40^\circ\text{C}$	38			V
		$I_S = 20 \text{ mA}; 25^\circ\text{C} < T_j < 150^\circ\text{C}$	41	46	52	
I_{STBY}	Supply current in standby at $V_{CC} = 13 \text{ V}$ ⁽²⁾	$V_{CC} = 13 \text{ V}; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 25^\circ\text{C}$			0.5	μA
		$V_{CC} = 13 \text{ V}; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 85^\circ\text{C}$ ⁽³⁾			0.5	μA
		$V_{CC} = 13 \text{ V}; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 125^\circ\text{C}$			3	μA
t_{D_STBY}	Standby mode blanking time	$V_{CC} = 13 \text{ V}; V_{IN} = V_{OUT} = V_{FR} = V_{SEL0,1,2} = 0 \text{ V}; V_{SEn} = 5 \text{ V} \text{ to } 0 \text{ V}$	60	300	550	μs
$I_{S(ON)}$	Supply current	$V_{CC} = 13 \text{ V}; V_{SEn} = V_{FR} = V_{SEL0,1,2} = 0 \text{ V}; V_{IN0,1,2,3} = 5 \text{ V}; I_{OUT0,1,2,3} = 0 \text{ A}$		10	16	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	$V_{CC} = 13 \text{ V}; V_{SEn} = 5 \text{ V}; V_{FR} = V_{SEL0,1,2} = 0 \text{ V}; V_{IN0,1,2,3} = 5 \text{ V}; I_{OUT0,1,2,3} = 1 \text{ A}$			20	mA
$I_{L(off)}$	Off-state output current at $V_{CC} = 13 \text{ V}$ ⁽¹⁾	$V_{IN} = V_{OUT} = 0 \text{ V}; V_{CC} = 13 \text{ V}; T_j = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0 \text{ V}; V_{CC} = 13 \text{ V}; T_j = 125^\circ\text{C}$	0		3	
V_F	Output - V_{CC} diode voltage ⁽¹⁾	$I_{OUT} = -1 \text{ A}; T_j = 150^\circ\text{C}$			0.7	V

1. For each channel.
2. PowerMOS leakage included.
3. Parameter specified by design; not subject to production test.

Table 6. Switching ($V_{CC} = 13$ V; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time at $T_j = 25^\circ\text{C}$	$R_L = 13 \Omega$	10	70	120	μs
$t_{d(off)}^{(1)}$	Turn-off delay time at $T_j = 25^\circ\text{C}$		10	40	100	
$(dV_{OUT}/dt)_{on}^{(1)}$	Turn-on voltage slope at $T_j = 25^\circ\text{C}$	$R_L = 13 \Omega$	0.1	0.29	0.7	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off}^{(1)}$	Turn-off voltage slope at $T_j = 25^\circ\text{C}$		0.1	0.35	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 13 \Omega$	—	0.15	0.2 ⁽²⁾	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	$R_L = 13 \Omega$	—	0.1	0.18 ⁽²⁾	mJ
$t_{SKew}^{(1)}$	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 13 \Omega$	-90	-40	10	μs

1. See [Figure 6: Switching time and Pulse skew](#).

2. Parameter guaranteed by design and characterization; not subject to production test.

Table 7. Logic Inputs (7 V < $V_{CC} < 28$ V; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT_{0,1,2,3} characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9$ V	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1$ V			10	μA
$V_{I(\text{hyst})}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1$ mA	5.3		7.2	V
		$I_{IN} = -1$ mA		-0.7		
FaultRST characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	$V_{IN} = 0.9$ V	1			μA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	$V_{IN} = 2.1$ V			10	μA
$V_{FR(\text{hyst})}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	$I_{IN} = 1$ mA	5.3		7.5	V
		$I_{IN} = -1$ mA		-0.7		
SEL_{0,1,2} characteristics (7 V < $V_{CC} < 18$ V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	$V_{IN} = 0.9$ V	1			μA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	$V_{IN} = 2.1$ V			10	μA

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH}	DC short circuit current	V _{CC} = 13 V	8	12	16	A
		4 V < V _{CC} < 18 V ⁽¹⁾			16	
I _{LIML}	Short circuit current during thermal cycling	V _{CC} = 13 V; T _R < T _j < T _{TSD}		4		
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 7		
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R) ⁽¹⁾			7		
ΔT _{J_SD}	Dynamic temperature	T _j = -40°C; V _{CC} = 13 V		60		K
t _{LATCH_RST} ⁽¹⁾	Fault reset time for output unlatch	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V - E.g. Ch ₀ V _{IN0} = 5 V; V _{SEL0,1,2} = 0 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 1 A; L = 6 mH; T _j = -40°C	V _{CC} - 38			V
		I _{OUT} = 1 A; L = 6 mH; T _j = 25°C to 150°C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V
V _{ON}	Output voltage drop limitation	I _{OUT} = 0.07 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. MultiSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	MultiSense clamp voltage	V _{SENSE} = 0 V; I _{SENSE} = 1 mA	-17		-12	V
		V _{SENSE} = 0 V; I _{SENSE} = -1 mA		7		
Current Sense characteristics						
K _{OL}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	330			
dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾	Current sense ratio drift at calibration point	I _{OUT} = 0.01 A to 0.025 A; I _{cal} = 17.5 mA; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	-30		30	%
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	330	580	830	
dK _{LED} /K _{LED} ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	-25		25	%
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.070 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	375	550	720	
dK ₀ /K ₀ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.070 A; V _{SENSE} = 0.5 V; V _{SEN} = 5 V	-20		20	%
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	365	520	675	
dK ₁ /K ₁ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-15		15	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	380	475	570	
dK ₂ /K ₂ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-10		10	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	420	470	520	
dK ₃ /K ₃ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 2 A; V _{SENSE} = 4 V; V _{SEN} = 5 V	-5		5	%

Table 9. MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: $V_{SEN} = 0 \text{ V}$	0		0.5	μA
		MultiSense disabled: $-1 \text{ V} < V_{SENSE} < 5 \text{ V}^{(1)}$	-0.5		0.5	
		MultiSense enabled: $V_{SEN} = 5 \text{ V}$ All channels ON; $I_{OUTX} = 0 \text{ A}$; Ch _x diagnostic selected: – E.g. Ch ₀ : $V_{IN0,1,2,3} = 5 \text{ V}$; $V_{SEL0} = 0 \text{ V}$; $V_{SEL1,2} = 0 \text{ V}$; $I_{OUT0} = 0 \text{ A}$; $I_{OUT1,2,3} = 1 \text{ A}$	0		2	
		MultiSense enabled: $V_{SEN} = 5 \text{ V}$; Ch _x OFF; Ch _x diagnostic selected: – E.g. Ch ₀ : $V_{IN0} = 0 \text{ V}$; $V_{IN1,2,3} = 0 \text{ V}$; $V_{SEL0} = 5 \text{ V}$; $V_{SEL1,2} = 0 \text{ V}$; $I_{OUT1,2,3} = 1 \text{ A}$	0		2	
$V_{OUT_MSD}^{(1)}$	Output Voltage for MultiSense shutdown	$V_{SEN} = 5 \text{ V}$; $R_{SENSE} = 2.7 \text{ k}\Omega$.E.g. Ch ₀ : $V_{IN0} = 5 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $I_{OUT0} = 1 \text{ A}$		5		V
V_{SENSE_SAT}	Multisense saturation voltage	$V_{CC} = 7 \text{ V}$; $R_{SENSE} = 2.7 \text{ k}\Omega$; $V_{SEN} = 5 \text{ V}$; $V_{IN0} = 5 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $I_{OUT0} = 2 \text{ A}$; $T_j = 150^\circ\text{C}$	5			V
$I_{SENSE_SAT}^{(1)}$	CS saturation current	$V_{CC} = 7 \text{ V}$; $V_{SENSE} = 4 \text{ V}$; $V_{IN0} = 5 \text{ V}$; $V_{SEN} = 5 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $T_j = 150^\circ\text{C}$	4			mA
$I_{OUT_SAT}^{(1)}$	Output saturation current	$V_{CC} = 7 \text{ V}$; $V_{SENSE} = 4 \text{ V}$; $V_{IN0} = 5 \text{ V}$; $V_{SEN} = 5 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $T_j = 150^\circ\text{C}$	2.2			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	$V_{SEN} = 5 \text{ V}$; Ch _x OFF; Ch _x diagnostic selected – E.g: Ch ₀ $V_{IN0} = 0 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	$V_{IN} = 0 \text{ V}$; $V_{OUT} = V_{OL}$; $T_j = -40^\circ\text{C}$ to 125°C	-100		-15	μA

Table 9. MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see <i>Figure 9</i>)	$V_{SEN} = 5 \text{ V}$; Ch_X ON to OFF transition; Ch_X diagnostic selected: – E.g: Ch_0 $V_{IN0} = 5 \text{ V}$ to 0 V ; $V_{SEL0,1,2} = 0 \text{ V}$; $V_{OUT0} = 4 \text{ V}$; $I_{OUT0} = 0 \text{ A}$	100	350	700	μs
$t_{D_OL_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	$V_{IN0,1,2,3} = 0 \text{ V}$; $V_{FR} = 0 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $V_{OUT0} = 4 \text{ V}$; $V_{SEN} = 0 \text{ V}$ to 5 V			60	μs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	$V_{SEN} = 5 \text{ V}$; Ch_X OFF; Ch_X diagnostic selected: – E.g: Ch_0 $V_{IN0} = 0 \text{ V}$; $V_{SEL0,1,2} = 0 \text{ V}$; $V_{OUT0} = 0 \text{ V}$ to 4 V		5	30	μs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature all channels off	$V_{SEN} = 5 \text{ V}$; $V_{SEL0} = 0 \text{ V}$; $V_{SEL1,2} = 5 \text{ V}$; $V_{IN0,1,2,3} = 0 \text{ V}$; $R_{SENSE} = 1 \text{ k}\Omega$; $T_j = -40^\circ\text{C}$	2.325	2.41	2.495	V
		$V_{SEN} = 5 \text{ V}$; $V_{SEL0} = 0 \text{ V}$; $V_{SEL1,2} = 5 \text{ V}$; $V_{IN0,1,2,3} = 0 \text{ V}$; $R_{SENSE} = 1 \text{ k}\Omega$; $T_j = 25^\circ\text{C}$	1.985	2.07	2.155	V
		$V_{SEN} = 5 \text{ V}$; $V_{SEL0} = 0 \text{ V}$; $V_{SEL1,2} = 5 \text{ V}$; $V_{IN0,1,2,3} = 0 \text{ V}$; $R_{SENSE} = 1 \text{ k}\Omega$; $T_j = 125^\circ\text{C}$	1.435	1.52	1.605	V
$dV_{SENSE_TC}/dT^{(1)}$	Temperature coefficient	$T_j = -40^\circ\text{C}$ to 150°C		-5.5		mV/K
Transfer function	$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC}/dT * (T - T_0)$					
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	$V_{CC} = 13 \text{ V}$; $V_{SEN} = 5 \text{ V}$; $V_{IN0,1,2,3} = 0 \text{ V}$; $V_{SEL0,1,2} = 5 \text{ V}$; $R_{SENSE} = 1 \text{ k}\Omega$	3.16	3.23	3.3	V
Transfer function ⁽³⁾	$V_{SENSE_VCC} = V_{CC} / 4$					

Table 9. MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fault diagnostic feedback (see Table 10)						
V_{SENSEH}	MultiSense output voltage in fault condition	$V_{CC} = 13 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega$ – E.g: Ch_0 in open load $V_{IN0} = 0 \text{ V}; V_{SEN} = 5 \text{ V};$ $V_{SEL0,1,2} = 0 \text{ V};$ $I_{OUT0} = 0 \text{ A}; V_{OUT0} = 4 \text{ V}$	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	$V_{CC} = 13 \text{ V}; V_{SENSE} = 5 \text{ V}$	7	20	30	mA
MultiSense timings (current sense mode - see Figure 7)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	$V_{IN} = 5 \text{ V}; V_{SEN} = 0 \text{ V to } 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega; R_L = 13 \Omega$			60	μs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	$V_{IN} = 5 \text{ V}; V_{SEN} = 0 \text{ V to } 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega; R_L = 13 \Omega$		5	20	μs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	$V_{IN} = 0 \text{ V to } 5 \text{ V}; V_{SEN} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega; R_L = 13 \Omega$		100	250	μs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$V_{IN} = 5 \text{ V}; V_{SEN} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega;$ $I_{SENSE} = 90\% \text{ of } I_{SENSEMAX};$ $R_L = 13 \Omega$			100	μs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	$V_{IN} = 5 \text{ V to } 0 \text{ V}; V_{SEN} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega; R_L = 13 \Omega$		50	250	μs
MultiSense timings (chip temperature sense mode - see Figure 8)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	$V_{SEN} = 0 \text{ V to } 5 \text{ V};$ $V_{SEL0} = 0 \text{ V}; V_{SEL1,2} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega$			60	μs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	$V_{SEN} = 5 \text{ V to } 0 \text{ V};$ $V_{SEL0} = 0 \text{ V}; V_{SEL1,2} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega$			20	μs
MultiSense timings (V_{CC} voltage sense mode - see Figure 8)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	$V_{SEN} = 0 \text{ V to } 5 \text{ V};$ $V_{SEL0,1,2} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega$			60	μs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	$V_{SEN} = 5 \text{ V to } 0 \text{ V};$ $V_{SEL0,1,2} = 5 \text{ V};$ $R_{SENSE} = 1 \text{ k}\Omega$			20	μs

Table 9. MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MultiSense timings (multiplexer transition times)⁽⁴⁾						
t_{D_XtoY}	MultiSense transition delay from Ch_X to Ch_Y	$V_{IN0} = 5 \text{ V}; V_{IN1} = 5 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL1,2} = 0 \text{ V}; V_{SEL0} = 0 \text{ V to } 5 \text{ V}; I_{OUT0} = 0 \text{ A}; I_{OUT1} = 1 \text{ A}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	$V_{IN0} = 5 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL0,1} = 0 \text{ V}; V_{SEL2} = 0 \text{ V to } 5 \text{ V}; I_{OUT0} = 0.5 \text{ A}; R_{SENSE} = 1 \text{ k}\Omega$			60	μs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	$V_{IN0} = 5 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL0,1} = 0 \text{ V}; V_{SEL2} = 5 \text{ V to } 0 \text{ V}; I_{OUT0} = 0.5 \text{ A}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs
$t_{D_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	$V_{IN3} = 5 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL0,1} = 5 \text{ V}; V_{SEL2} = 0 \text{ V to } 5 \text{ V}; I_{OUT3} = 0.5 \text{ A}; R_{SENSE} = 1 \text{ k}\Omega$			60	μs
$t_{D_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense to	$V_{IN3} = 5 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL0,1} = 5 \text{ V}; V_{SEL2} = 5 \text{ V to } 0 \text{ V}; I_{OUT3} = 0.5 \text{ A}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs
$t_{D_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	$V_{CC} = 13 \text{ V}; T_j = 125^\circ\text{C}; V_{SEN} = 5 \text{ V}; V_{SEL1,2} = 5 \text{ V}; V_{SEL0} = 0 \text{ V to } 5 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs
$t_{D_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	$V_{CC} = 13 \text{ V}; T_j = 125^\circ\text{C}; V_{SEN} = 5 \text{ V}; V_{SEL1,2} = 5 \text{ V}; V_{SEL0} = 5 \text{ V to } 0 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs
$t_{D_CStoVSENSEH}$	MultiSense transition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	$V_{IN0} = 5 \text{ V}; V_{IN1} = 0 \text{ V}; V_{SEN} = 5 \text{ V}; V_{SEL1,2} = 0 \text{ V}; V_{SEL0} = 0 \text{ V to } 5 \text{ V}; I_{OUT0} = 1 \text{ A}; V_{OUT1} = 4 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega$			20	μs

1. Parameter specified by design; not subject to production test.
2. All values refer to $V_{CC} = 13 \text{ V}; T_j = 25^\circ\text{C}$, unless otherwise specified.
3. V_{CC} sensing and T_C sensing are referred to GND potential.
4. Transition delays are measured up to +/- 10% of final conditions.

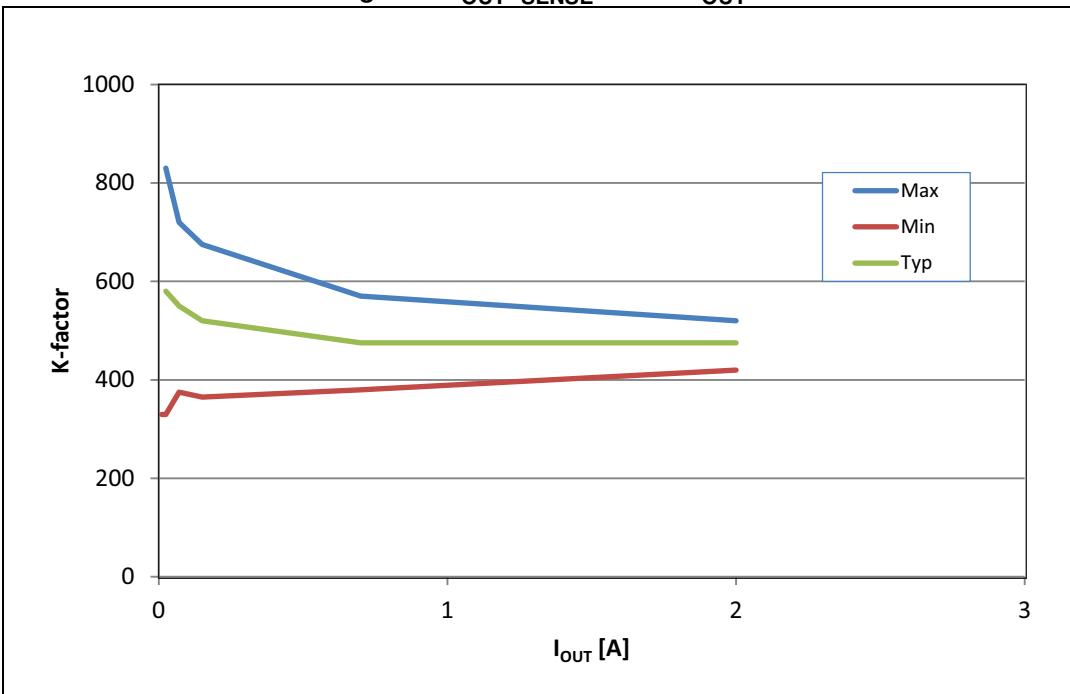
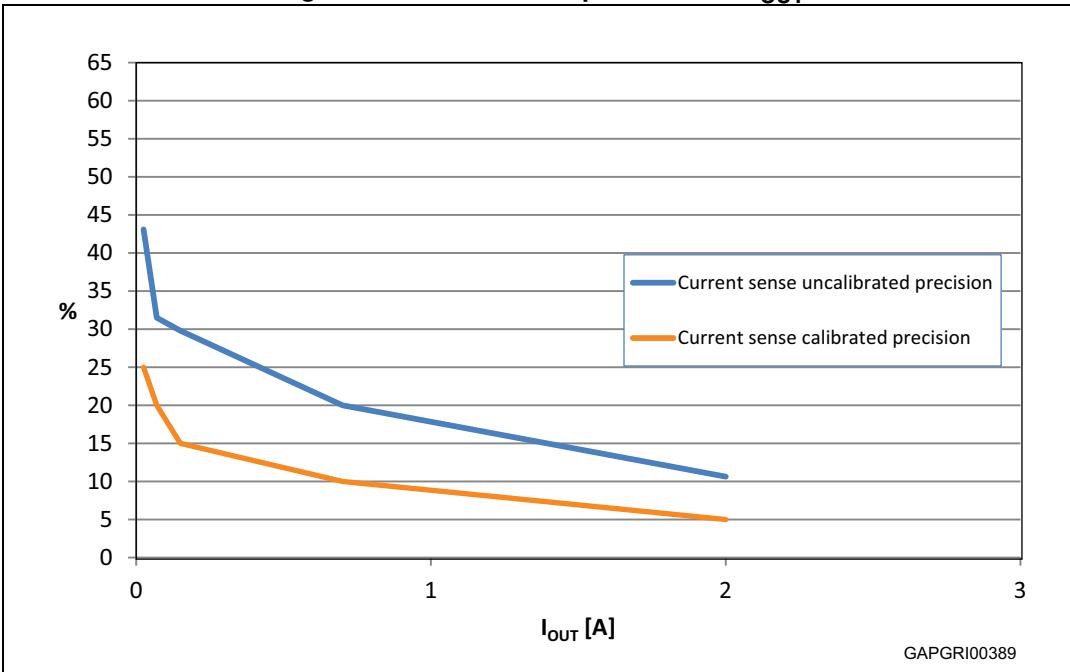
Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT} **Figure 5. Current sense precision vs. I_{OUT}** 

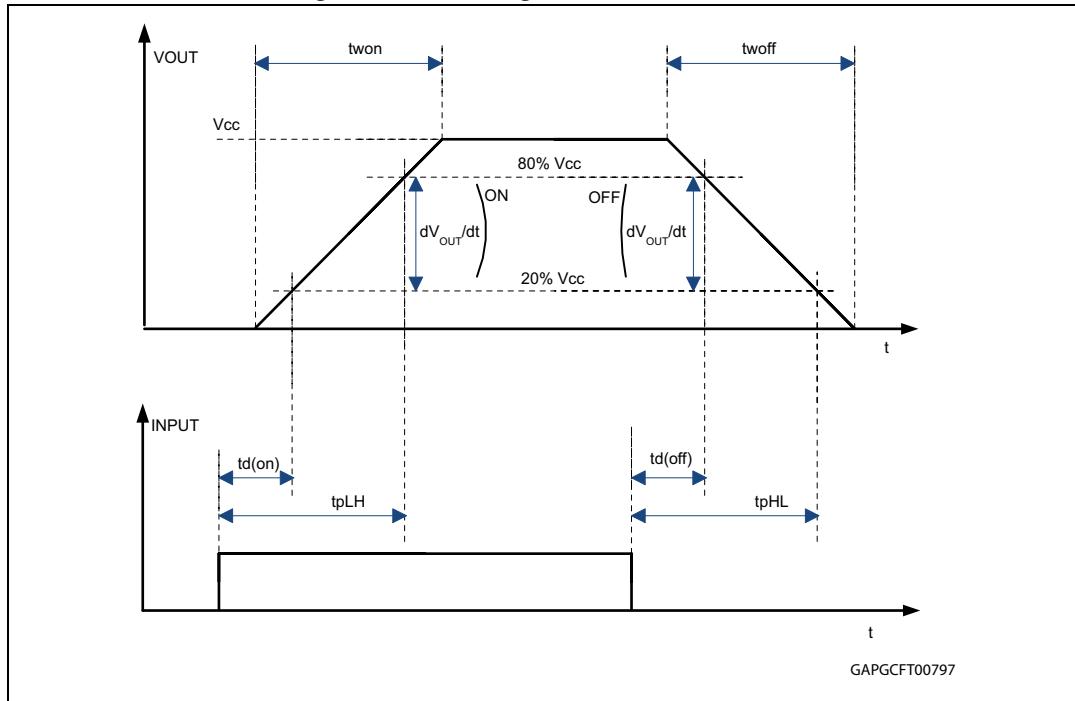
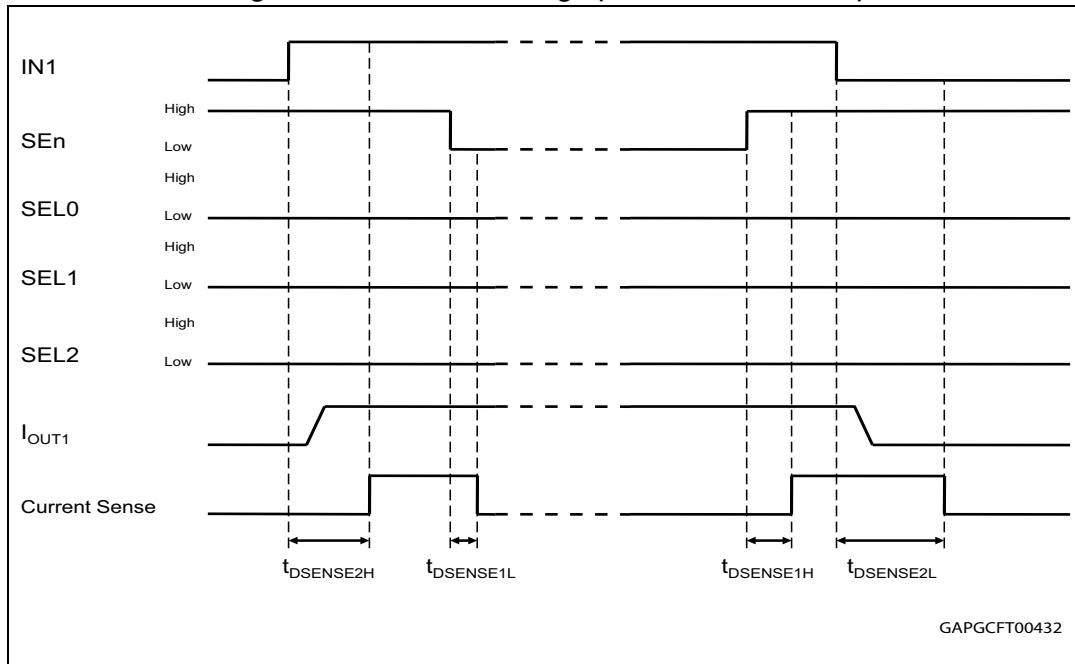
Figure 6. Switching time and Pulse skew**Figure 7. MultiSense timings (current sense mode)**

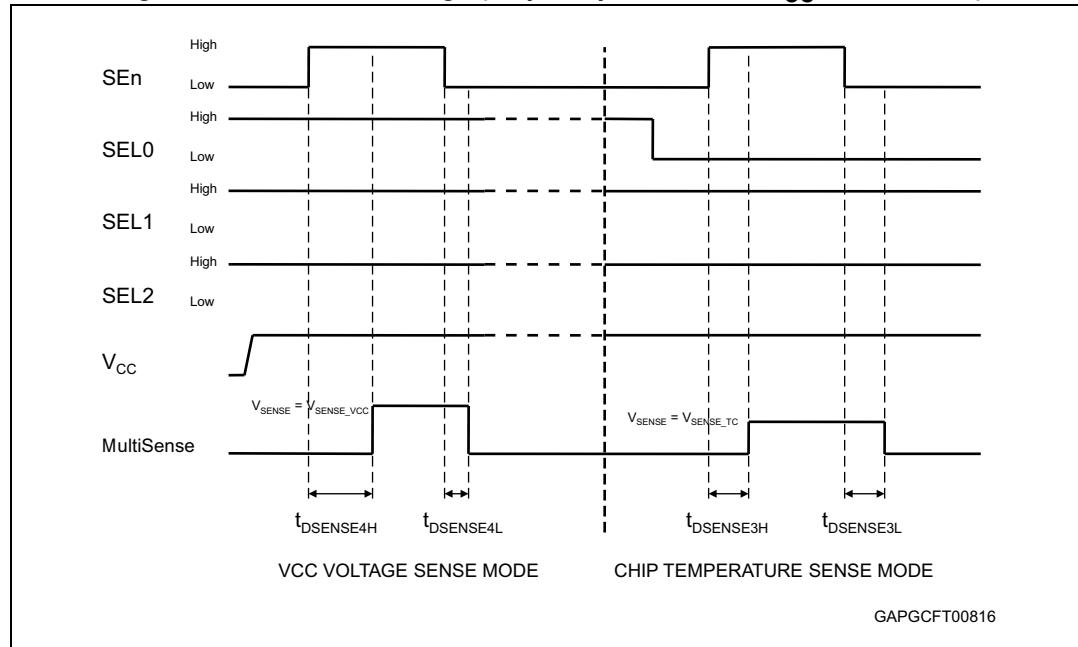
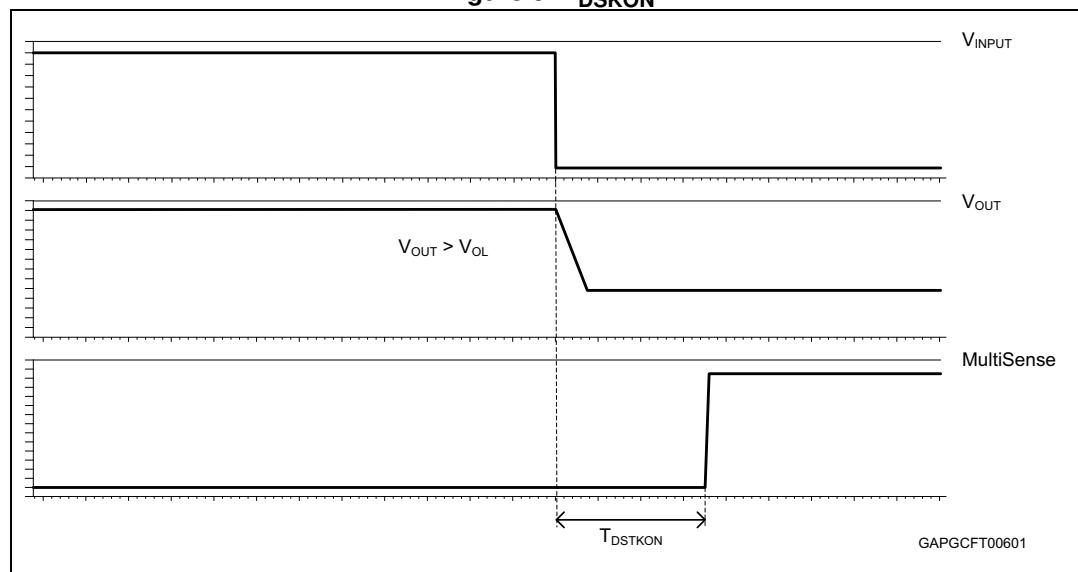
Figure 8. Multisense timings (chip temperature and V_{CC} sense mode)**Figure 9. T_{DSTKON}** 

Table 10. Truth table

Mode	Conditions	IN _X	FR	SEN	SEL _X	OUT _X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T _j < 150°C	L	X	Refer to Table 11		L	Refer to Table 11	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off
Overload	Overload or short to GND causing: T _j > T _{TSD} or ΔT _j > ΔT _{j,SD}	L	X	Refer to Table 11		L	Refer to Table 11	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off
Under-voltage	V _{CC} < V _{USD} (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when V _{CC} > V _{USD} + V _{USDhyst} (rising)
OFF-state diagnostics	Short to V _{CC}	L	X	Refer to Table 11		H	Refer to Table 11	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	Refer to Table 11		< 0 V	Refer to Table 11	

Table 11. MultiSense multiplexer addressing

SEn	SEL ₂	SEL ₁	SEL ₀	MUX channel	MultiSense output				
					Nomal mode	Overload	OFF-state diag. ⁽¹⁾	Negative output	
L	X	X	X		Hi-Z				
H	L	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z	
H	L	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z	
H	L	H	L	Channel 2 diagnostic	$I_{SENSE} = 1/K * I_{OUT2}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z	
H	L	H	H	Channel 3 diagnostic	$I_{SENSE} = 1/K * I_{OUT3}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z	
H	H	L	L	T _{CHIP} Sense	$V_{SENSE} = V_{SENSE_TC}$				
H	H	L	H	V _{CC} Sense	$V_{SENSE} = V_{SENSE_VCC}$				
H	H	H	L	T _{CHIP} Sense	$V_{SENSE} = V_{SENSE_TC}$				
H	H	H	H	V _{CC} Sense	$V_{SENSE} = V_{SENSE_VCC}$				

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic.
 Example 1: FR = 1; IN₀ = 0; OUT₀ = L (latched); MUX channel = channel 0 diagnostic; Multisense = 0
 Example 2: FR = 1; IN₀ = 0; OUT₀ = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic;
 Multisense = V_{SENSEH}

2.4 Waveforms

Figure 10. Latch functionality - behavior in hard short circuit condition ($T_{AMB} \ll T_{TSD}$)

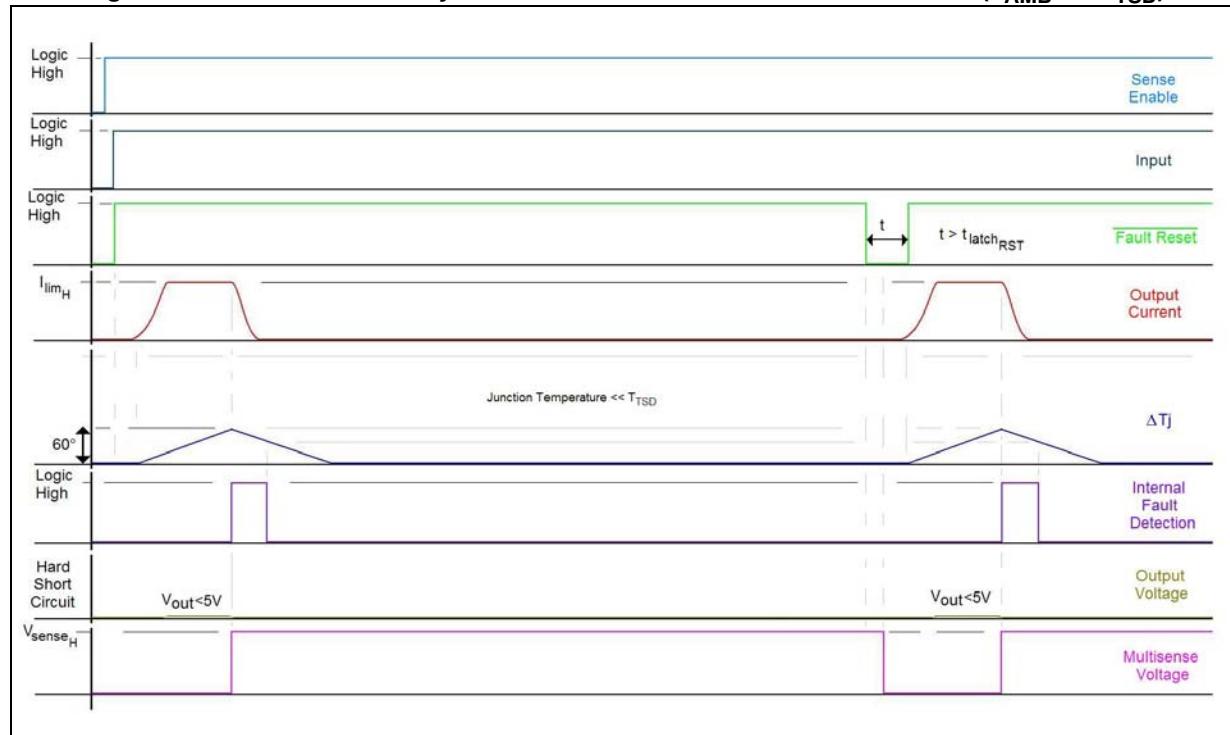


Figure 11. Latch functionality - behavior in hard short circuit condition

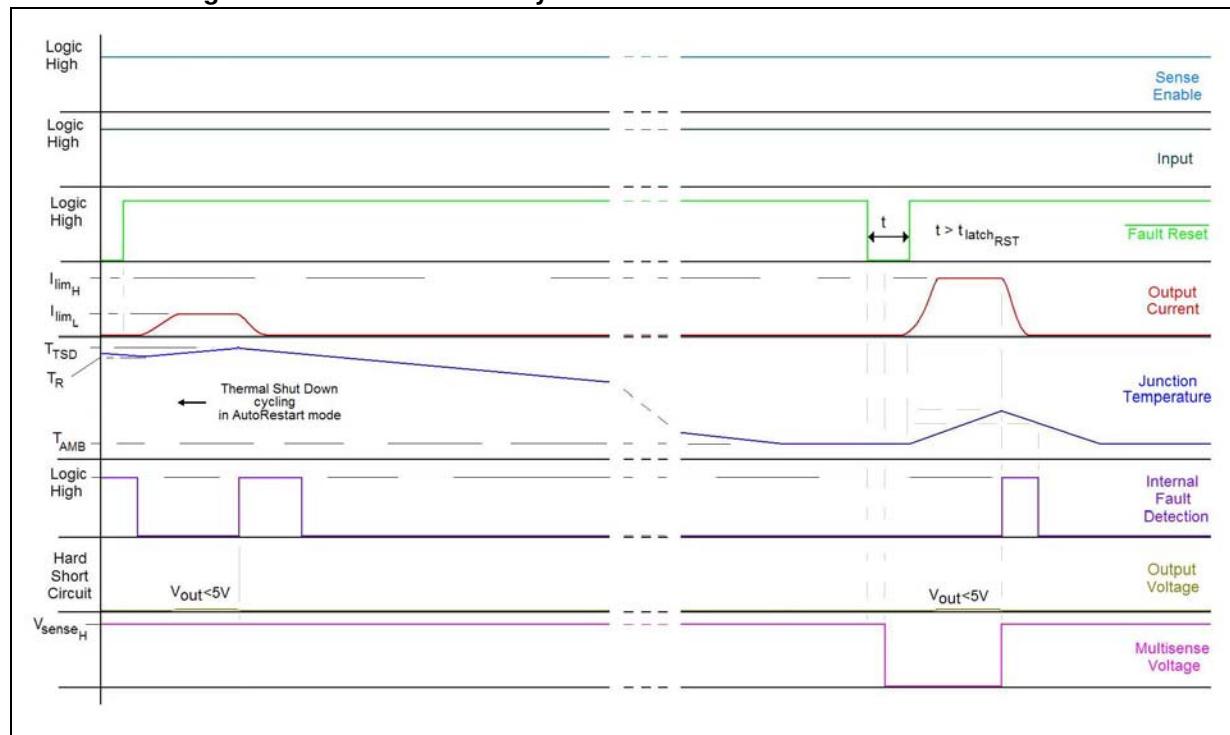


Figure 12. Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

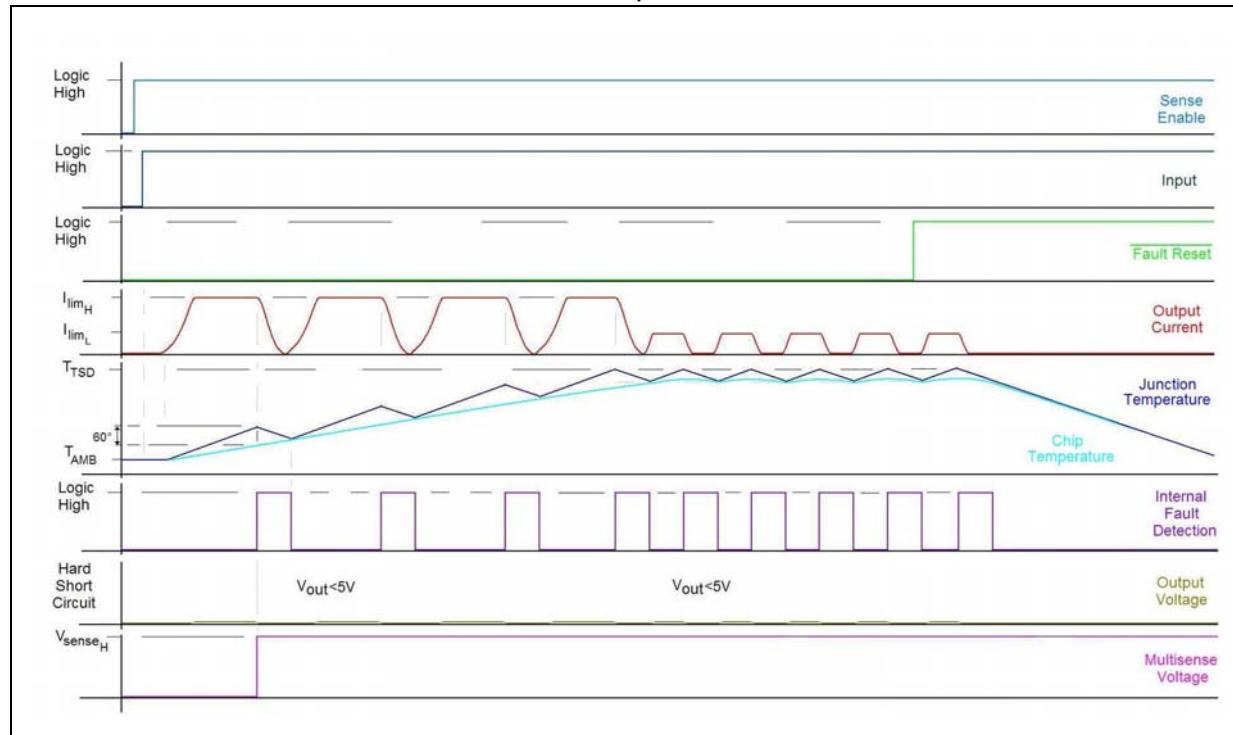


Figure 13. Standby mode activation

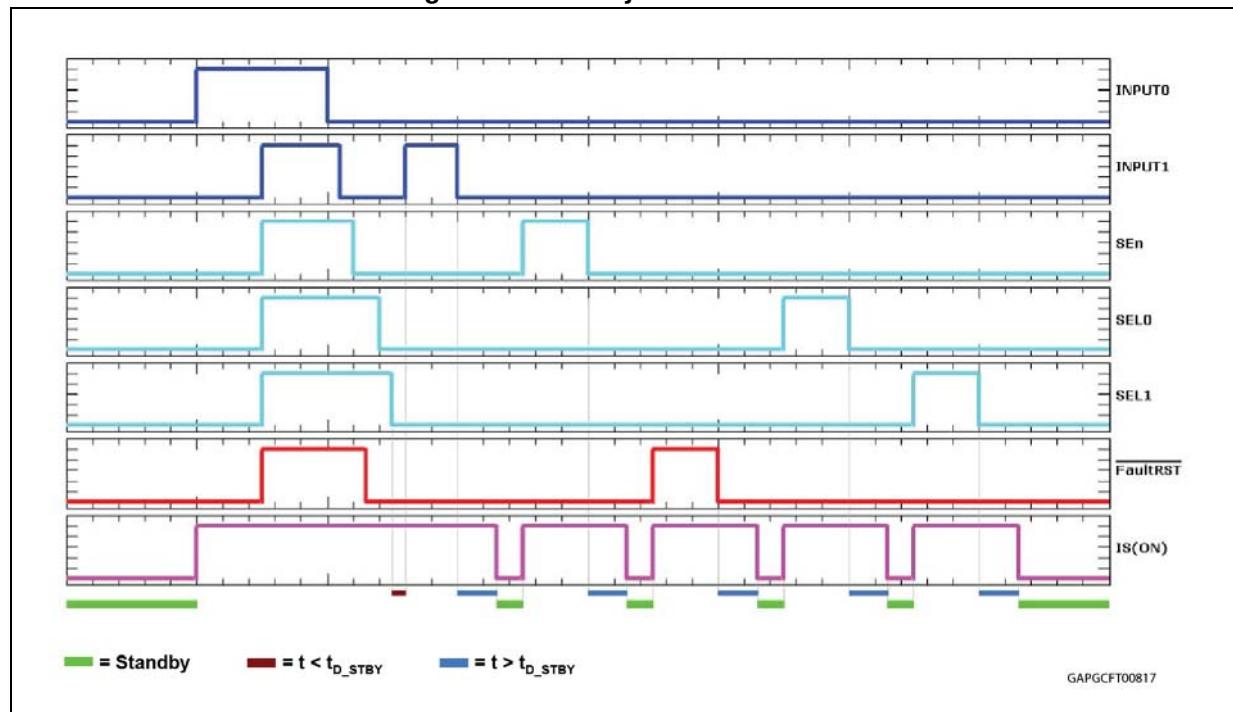


Figure 14. Standby state diagram