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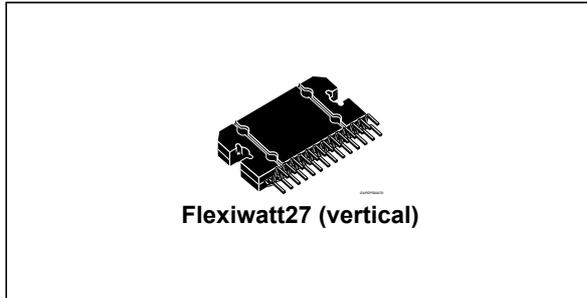
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4 x 45 W power amplifier with full I²C diagnostics, SSR and low voltage operation

Datasheet - production data



- Standby/mute pin
- Linear thermal shutdown with multiple thermal warnings
- ESD protection
- Very robust against misconnections
- Improved SVR suppression during battery transients
- Capable to operate down to 6 V (e.g. "Start-stop")
- Selectable SSR (speaker safety routine)

Features

- Multipower BCD technology
- MOSFET output power stage
- DMOS power output
- High output power capability 4x25 W/4 Ω @ 14.4 V, 1 kHz, 10% THD, 4 x 45 W max power
- 2 Ω driving capability (64 W max power)
- Full I²C bus driving:
 - Standby
 - Independent front/rear soft play/mute
 - Selectable gain 26 dB /16 dB (for low noise line output function)
 - I²C bus digital diagnostics (including DC and AC load detection)
- Flexible fault detection through integrated diagnostic
- DC offset detection
- Four independent short circuit protections
- Clipping detector pin with selectable threshold (2 %/10 %)

Description

The TDA75616LV is a new quad bridge car radio amplifier, designed in BCD technology, in order to include a wide range of innovative features in a very compact and flexible device.

The TDA75616LV is equipped with the most complete diagnostics array that communicates the status of each speaker through the I²C bus.

TDA75616LV has been designed to be very robust against several kinds of misconnections.

The TDA75616LV is equipped with the SSR (speaker safety routine), a procedure able to check the offset at the speakers and automatically shut down the power amplifier in case of dangerous DC voltage.

It is moreover compliant to the most recent OEM specifications for low voltage operation (so called 'start-stop' battery profile during engine stop), helping car manufacturers to reduce the overall emissions and thus contributing to environment protection.

Table 1. Device summary

Order code	Package	Packing
TDA75616LV-48X	Flexiwatt27 (vertical)	Tube

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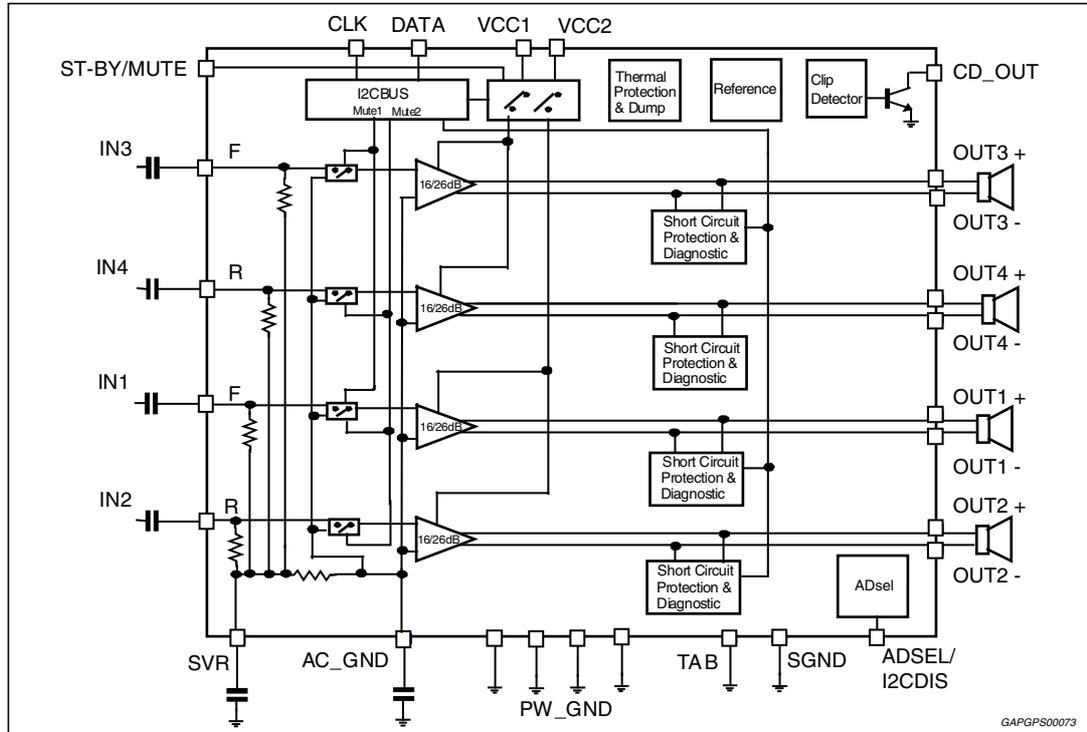
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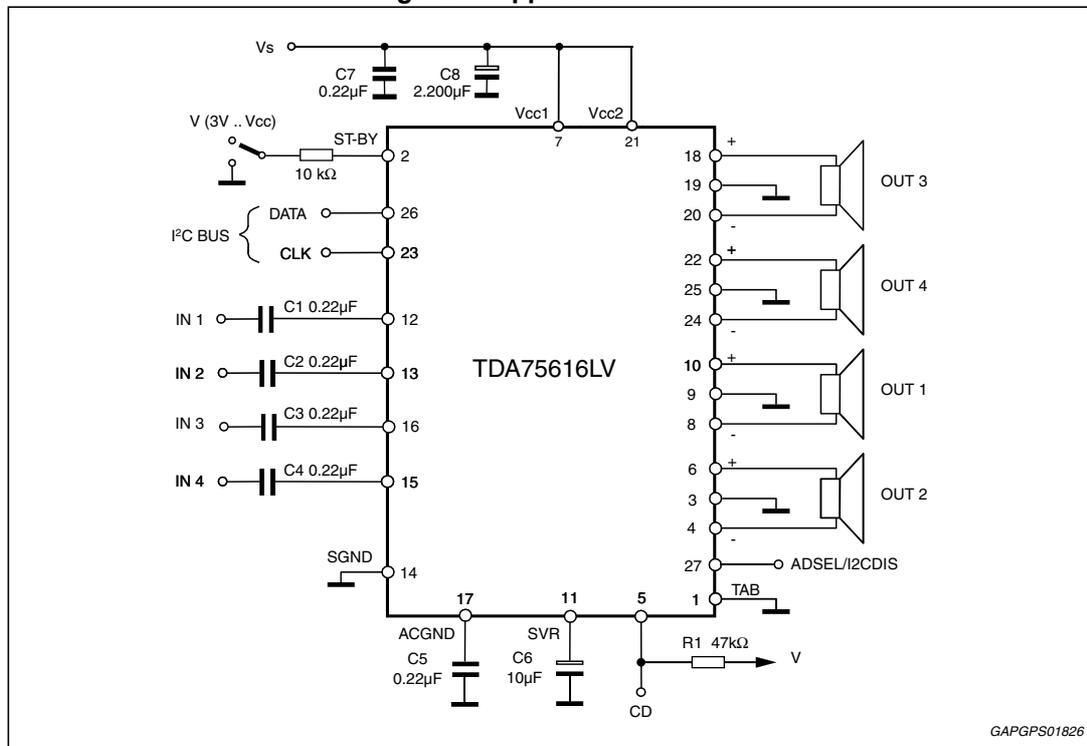
1 Block diagram and application circuits

Figure 1. Block diagram



GAPGPS00073

Figure 2. Application circuit



GAPGPS01826

2 Pins description

For channel name reference: CH1 = LF, CH2 = LR, CH3 = RF and CH4 = RR.

Figure 3. Pins connection diagram (top of view)

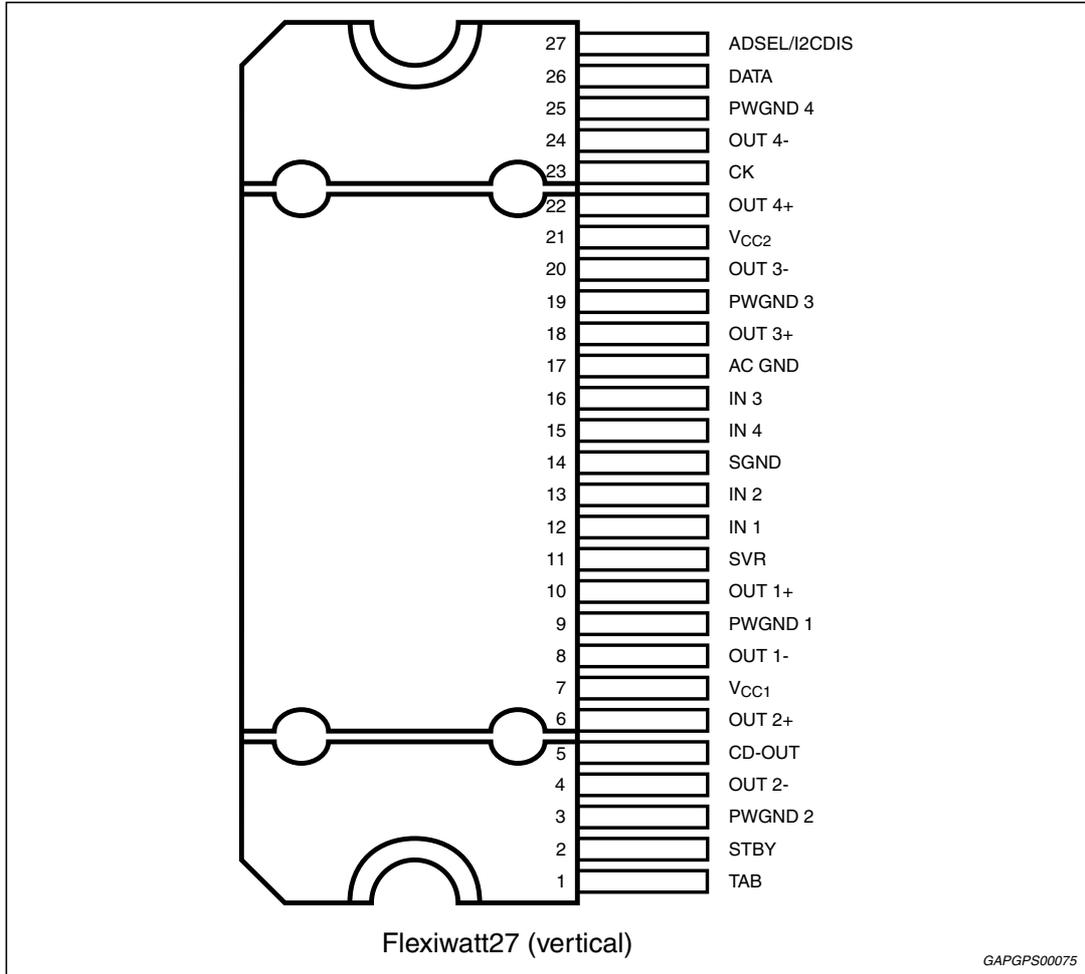


Table 2. Pins list description

Pin #	Pin name	Function
1	TAB	-
2	STBY	Standby pin
3	PWGND2	Channel 2 output power ground
4	OUT2-	Channel 2, - output
5	CD	Clip detector output pin
6	OUT2+	Channel 2, + output
7	VCC1	Supply voltage pin1
8	OUT1-	Channel 1, - output
9	PWGND1	Channel 1 output power ground
10	OUT1+	Channel 1, + output
11	SVR	SVR pin
12	IN1	Input pin, channel 1
13	IN2	Input pin, channel 2
14	SGND	Signal ground pin
15	IN4	Input pin, channel 4
16	IN3	Input pin, channel 3
17	AC GND	AC ground
18	OUT3+	Channel 3, + output
19	PWGND3	Channel 3 output power ground
20	OUT3-	Channel 3, - output
21	VCC2	Supply voltage pin2
22	OUT4+	Channel 4, + output
23	CK	I ² C bus clock
24	OUT4-	Channel 4, - output
25	PWGND4	Channel 4 output power ground
26	DATA	I ² C bus data pin/gain selector
27	ADSEL/I2CDIS	Address selector pin/ I ² C bus disable (legacy select)

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{op}	Operating supply voltage ⁽¹⁾	18	V
V_S	DC supply voltage	28	V
V_{peak}	Peak supply voltage (for $t_{max} = 50$ ms)	50	V
GNDmax	Ground pins voltage	-0.3 to 0.3	V
V_{CK}, V_{DATA}	CK and DATA pin voltage	-0.3 to 6	V
V_{cd}	Clip detector voltage	-0.3 to 5.5	V
V_{stby}	STBY pin voltage	-0.3 to V_{op}	V
I_O	Output peak current (not repetitive $t_{max} = 100$ ms)	8	A
	Output peak current (repetitive $f > 10$ kHz)	6	
P_{tot}	Power dissipation $T_{case} = 70^\circ\text{C}$	85	W
T_{stg}, T_j	Storage and junction temperature ⁽²⁾	-55 to 150	$^\circ\text{C}$
T_{amb}	Operative temperature range	-40 to +105	$^\circ\text{C}$

1. For $R_L = 2 \Omega$ the output current limit might be reached for $V_{OP} > 16$ V; thus triggering self-protection.

2. A suitable dissipation system should be used to keep T_j inside the specified limits.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal resistance junction-to-case Max.	1	$^\circ\text{C}/\text{W}$

3.3 Electrical characteristics

Refer to the test circuit, $V_S = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $G_V = 26\text{ dB}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V_S	Supply voltage range	$R_L = 4\ \Omega$	6	-	18	V
		$R_L = 2\ \Omega$	6	-	16 ⁽¹⁾	
I_d	Total quiescent drain current	-	-	165	250	mA
R_{IN}	Input impedance	-	45	60	70	k Ω
V_{AM}	Min. supply mute threshold	IB1(D7) = 1	7	-	8	V
		IB1(D7) = 0 (default) ⁽²⁾	5	-	6	
V_{OS}	Offset voltage	Mute & play	-80	-	80	mV
V_{dth}	Dump threshold	-	18.5	-	20.5	V
I_{SB}	Standby current	$V_{\text{standby}} = 0$	-	1	5	μA
SVR	Supply voltage rejection	$f = 100\text{ Hz to }10\text{ kHz}$; $V_r = 1\text{ Vpk}$; $R_g = 600\ \Omega$	60	70	-	dB
T_{ON}	Turn on timing (Mute play transition)	D2/D1 (IB1) 0 to 1	-	25	50	ms
T_{OFF}	Turn off timing (Play mute transition)	D2/D1 (IB1) 1 to 0	-	25	50	ms
TH_{WARN1}	Average junction temperature for TH warning 1	DB1 (D7) = 1	-	155	-	$^\circ\text{C}$
TH_{WARN2}	Average junction temperature for TH warning 2	DB4 (D7) = 1	-	140	-	
TH_{WARN3}	Average junction temperature for TH warning 3	DB4 (D6) = 1	-	125	-	
Audio performances						
P_O	Output power	Max. power ⁽³⁾ $V_S = 15.2\text{ V}$, $R_L = 4\ \Omega$	-	45	-	W
		THD = 10 %, $R_L = 4\ \Omega$	23	25	-	W
		THD = 1 %, $R_L = 4\ \Omega$	-	22	-	W
		$R_L = 2\ \Omega$; THD 10 %	-	44	-	W
		$R_L = 2\ \Omega$; THD 1 %	-	33	-	W
		$R_L = 2\ \Omega$; Max. power ⁽³⁾ $V_S = 14.4\text{ V}$	-	64	-	W
THD	Total harmonic distortion	$P_O = 1\text{ W to }10\text{ W}$	-	0.015	0.1	%
		$P_O = 1\text{-}10\text{ W}$, $f = 10\text{ kHz}$	-	0.15	0.5	%
		$G_V = 16\text{ dB}$; $V_O = 0.1\text{ to }5\text{ VRMS}$	-	0.01	0.05	%
C_T	Cross talk	$f = 1\text{ kHz to }10\text{ kHz}$, $R_g = 600\ \Omega$	50	65	-	dB
G_{V1}	Voltage gain 1	-	25	26	27	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ΔG_{V1}	Voltage gain match 1	-	-1	-	1	dB
G_{V2}	Voltage gain 2	-	15	16	17	dB
ΔG_{V2}	Voltage gain match 2	-	-1	-	1	dB
E_{IN1}	Output noise voltage 1	$R_g = 600 \Omega$ 20 Hz to 22 kHz	-	45	60	μV
E_{IN2}	Output noise voltage 2	$R_g = 600 \Omega$; $G_V = 16$ dB 20 Hz to 22 kHz	-	20	30	μV
BW	Power bandwidth	-	100	-	-	kHz
CMRR	Input CMRR	$V_{CM} = 1$ Vpk-pk; $R_g = 0 \Omega$	-	70	-	dB
ΔV_{OITU}	ITU Pop filter output voltage	Standby to Mute and Mute to Standby transition $T_{amb} = 25 \text{ }^\circ\text{C}$, ITU-R 2K, $C_{svr} = 10 \mu F$ $V_s = 14.4$ V	-7.5	-	+7.5	mV
		Mute to Play transition $T_{amb} = 25 \text{ }^\circ\text{C}$, ITU-R 2K, $V_s = 14.4$ V ⁽⁴⁾	-7.5	-	+7.5	mV
		Play to Mute transition $T_{amb} = 25 \text{ }^\circ\text{C}$, ITU-R 2K, $V_s = 14.4$ V ⁽⁵⁾	-7.5	-	+7.5	mV
Clip detector						
CD_{LK}	Clip det. high leakage current	CD off / $V_{CD} = 6$ V	-	0	5	μA
CD_{SAT}	Clip det sat. voltage	CD on; $I_{CD} = 1$ mA	-	-	300	mV
CD_{THD}	Clip det THD level	D0 (IB1) = 1	5	10	15	%
		D0 (IB1) = 0	1	2	3	%
Control pin characteristics						
V_{SBY}	Standby/mute pin for standby	-	0	-	1.2	V
V_{MU}	Standby/mute pin for mute	-	2.9	-	3.5	V
V_{OP}	Standby/mute pin for operating	-	4.5	-	18	V
I_{MU}	Standby/mute pin current	$V_{st-by/mute} = 4.5$ V	-	1	5	μA
		$V_{st-by/mute} < 1.2$ V	-	0	5	μA
A_{SB}	Standby attenuation	-	90	110	-	dB
A_M	Mute attenuation	-	80	100	-	dB

Table 5. Electrical characteristics (continued)

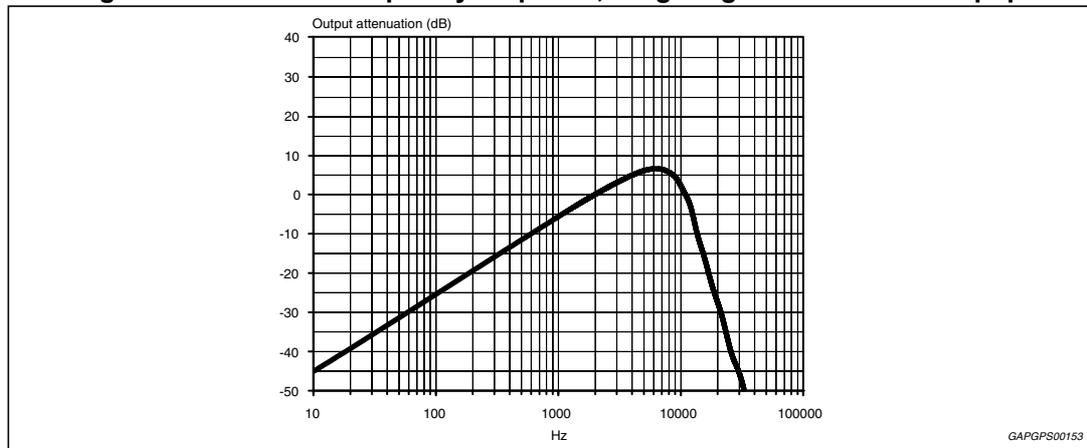
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Turn on diagnostics 1 (Power amplifier mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in short circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to Vs)		Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).		1.8	-	Vs -1.8	V
Lsc	Shorted load det.		-	-	0.5	Ω
Lop	Open load det.		85	-	-	Ω
Lnop	Normal load det.		1.5	-	45	Ω
Turn on diagnostics 2 (Line driver mode)						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to Vs)	-	Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).	-	1.8	-	Vs -1.8	V
Lsc	Shorted load det.	-	-	-	1.5	Ω
Lop	Open load det.	-	330	-	-	Ω
Lnop	Normal load det.	-	7	-	180	Ω
Permanent diagnostics 2 (Power amplifier mode or line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in short circuit to GND)	Power amplifier in mute or play, one or more short circuits protection activated	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the output is considered in short circuit to Vs)		Vs -1.2	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).		1.8	-	Vs -1.8	V
L _{SC}	Shorted load det.	Power amplifier mode	-	-	0.5	Ω
		Line driver mode	-	-	1.5	Ω
V _O	Offset detection	Power amplifier in play, AC input signals = 0	±1.5	±2	±2.5	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{NLH}	Normal load current detection	$V_O < (V_S - 5)\mu k$, IB2 (D7) = 0	500	-	-	mA
I_{OLH}	Open load current detection		-	-	250	mA
I_{NLL}	Normal load current detection	$V_O < (V_S - 5)\mu k$, IB2 (D7) = 1	250	-	-	mA
I_{OLL}	Open load current detection		-	-	125	mA
I²C bus interface						
S_{CL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	1.5	V
V_{IH}	Input high voltage	-	2.3	-	-	V

- When $V_S > 16\text{ V}$ the output current limit is reached (triggering embedded internal protections).
- In legacy mode only low threshold option is available.
- Saturated square wave output.
- Voltage ramp on STBY pin:
from 3.3 V to 4.2 V in $t \geq 40\text{ ms}$.
In case of I²C mode command IB1(D1) = 1 (Mute → Unmute rear channels) and/or IB1(D2) = 1 (Mute → Unmute front channels) must be transmitted before to start the voltage ramp on STBY pin.
- Voltage ramp on STBY pin:
from 4.05 V to 3.55 V in $t \geq 40\text{ ms}$.
In case of I²C mode command IB1(D1) = 0 Unmute → Mute rear channels) and/or IB1(D2) = 0 (Unmute → Mute front channels) must be NOT transmitted before to start the voltage ramp on STBY pin.

Figure 4. ITU R-ARM frequency response, weighting filter for transient pop



4 Diagnostics functional description

4.1 Turn-on diagnostic

It is recommended to activate this function at the turn-on (standby out) through an I²C bus request. Detectable output faults are:

- Short to GND
- Short to Vs
- Short across the speaker
- Open speaker

To verify if any of the above misconnections are in place, a subsonic (inaudible) current pulse (Figure 5) is internally generated, sent through the speaker(s) and sunk back. The Turn On diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I²C reading).

If the "standby out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (during the pulse the power stage stays 'off', showing high impedance at the outputs).

Afterwards, when the Amplifier is biased, the PERMANENT diagnostic takes place. The previous Turn On state is kept until a short appears at the outputs.

Figure 5. Turn-on diagnostic: working principle

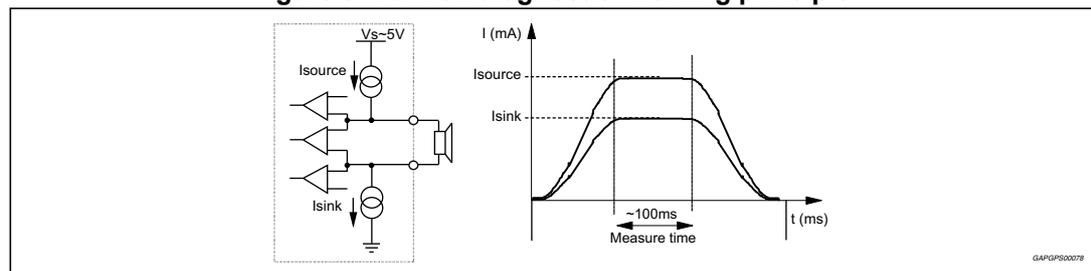


Figure 6 and 7 show SVR and OUTPUT waveforms at the turn-on (stand-by out) with and without turn-on diagnostic.

Figure 6. SVR and output behavior (Case 1: without turn-on diagnostic)

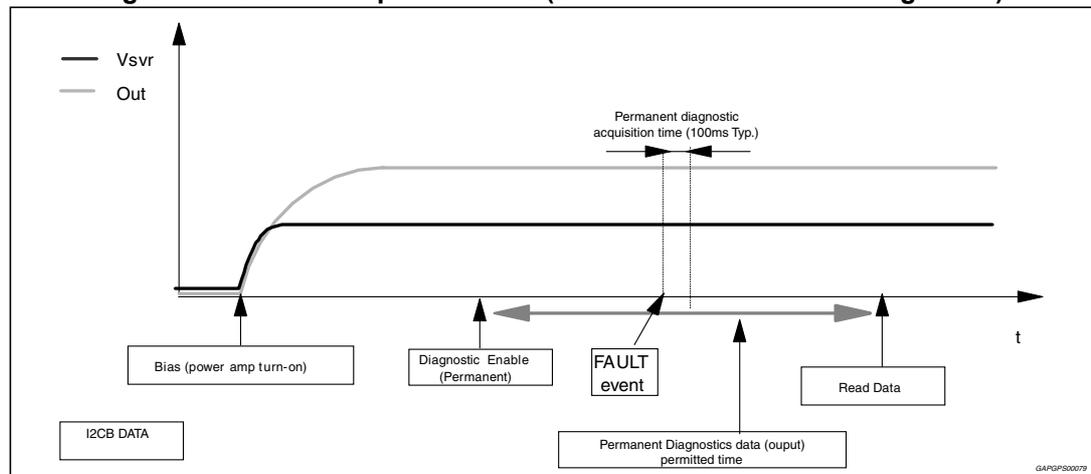
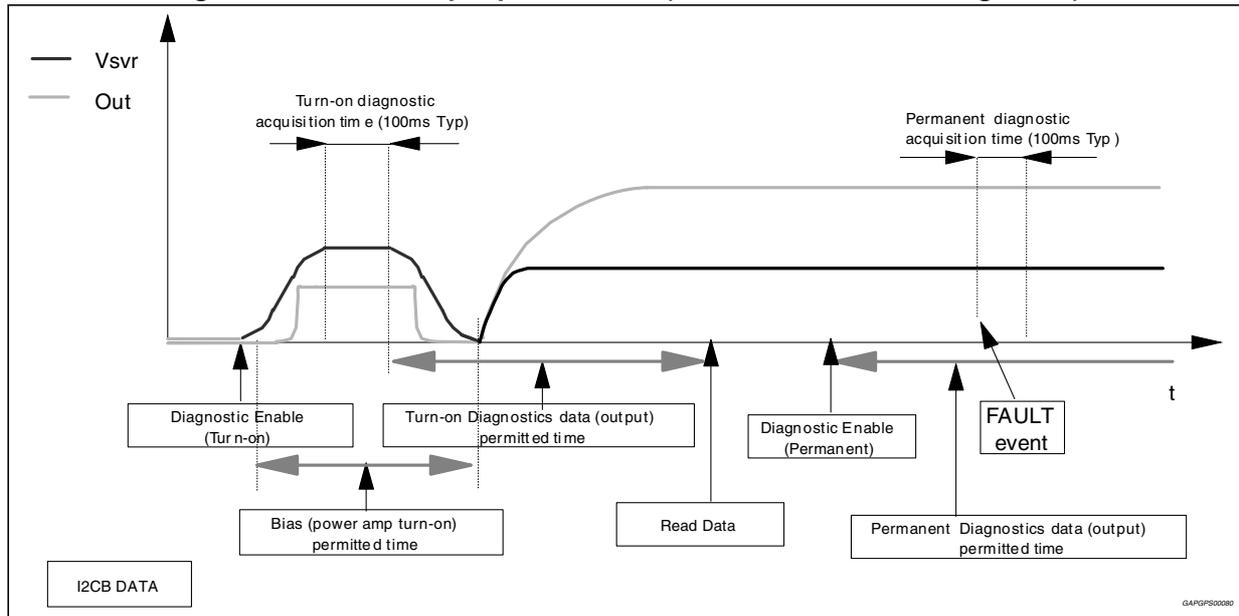
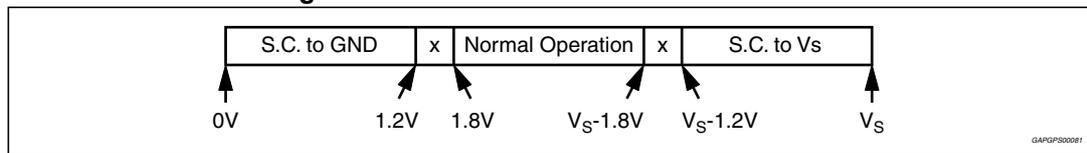


Figure 7. SVR and output pin behavior (Case 2: with turn-on diagnostic)



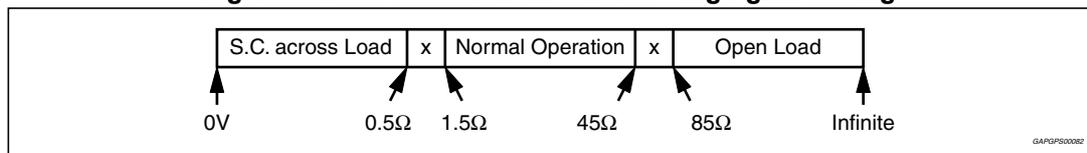
The information related to the outputs status is read and memorized at the end of the current pulse plateau. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for Short to GND / Vs the fault-detection thresholds remain unchanged from 26 dB to 16 dB gain setting. They are as follows:

Figure 8. Short circuit detection thresholds



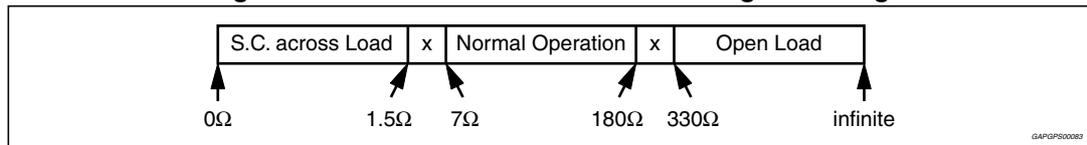
Concerning Short across the speaker / Open speaker, the threshold varies from 26 dB to 16 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

Figure 9. Load detection thresholds - high gain setting



If the Line-Driver mode ($G_v = 16$ dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

Figure 10. Load detection threshold - low gain setting



4.2 Permanent diagnostics

Detectable conventional faults are:

- Short to GND
- Short to V_s
- Short across the speaker

The following additional feature is provided:

- Output offset detection (see [Section 5](#))

The TDA75616LV has 2 operating status:

1. **RESTART mode.** The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms ([Figure 11](#)). Restart takes place when the overload is removed.
2. **DIAGNOSTIC mode.** It is enabled via I²C bus and it self activates if an output overload (such as to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows ([Figure 12](#)):
 - To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns active.
 - Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
 - After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I²C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.
 - To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (over half a second is recommended).

Figure 11. Restart timing without diagnostic enable (permanent) - Each 1 mS time, a sampling of the fault is done

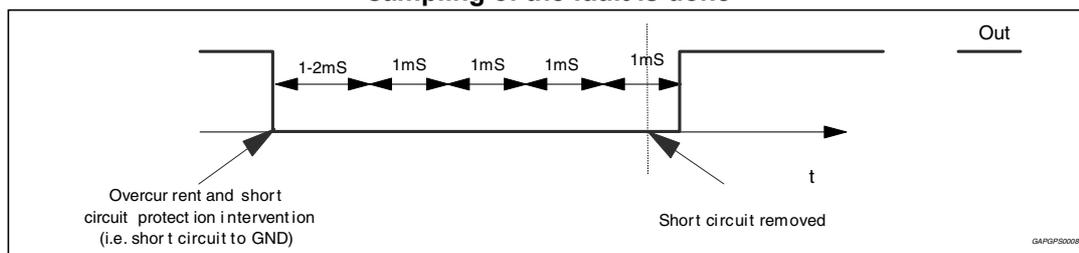
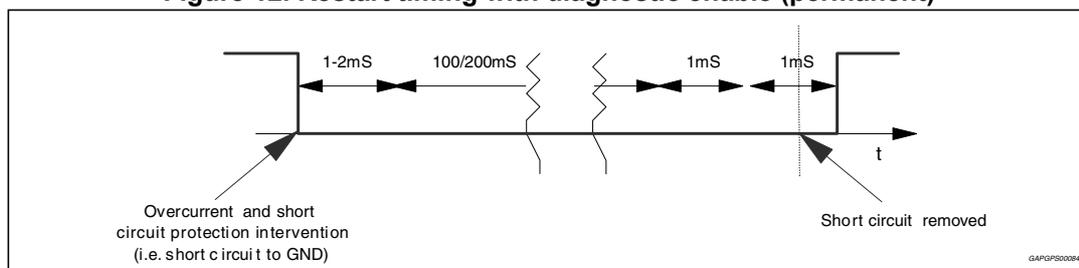


Figure 12. Restart timing with diagnostic enable (permanent)



4.3 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitive (AC) coupled loads.

This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, and it is enabled by setting (IB2-D2) = 1. Two different detection levels are available:

- High current threshold IB2 (D7) = 0
I_{out} > 500 mA_{pk} = normal status
I_{out} < 250 mA_{pk} = open tweeter
- Low current threshold IB2 (D7) = 1
I_{out} > 250 mA_{pk} = normal status
I_{out} < 125 mA_{pk} = open tweeter

To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such as to determine an output current higher than 500 mA_{pk} with IB2(D7) = 0 (higher than 250 mA_{pk} with IB2(D7) = 1) in normal conditions and lower than 250 mA_{pk} with IB2(D7) = 0 (lower than 125 mA_{pk} with IB2(D7)=1) should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2> up to the I²C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses over the above threshold over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 kHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

Figure 13 and *14* shows the load impedance as a function of the peak output voltage and the relevant diagnostic fields.

It is recommended to keep output voltage always below 8 V (high threshold case) or 4 V (low threshold case) to avoid the circuit to be saturated (causing wrong detection cases).

This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

Figure 13. Current detection high: load impedance |Z| vs. output peak voltage

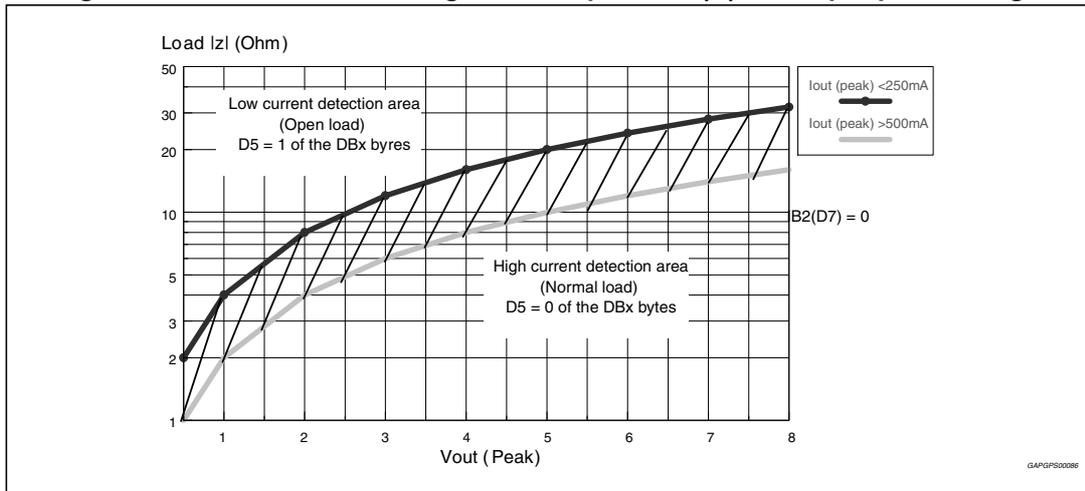
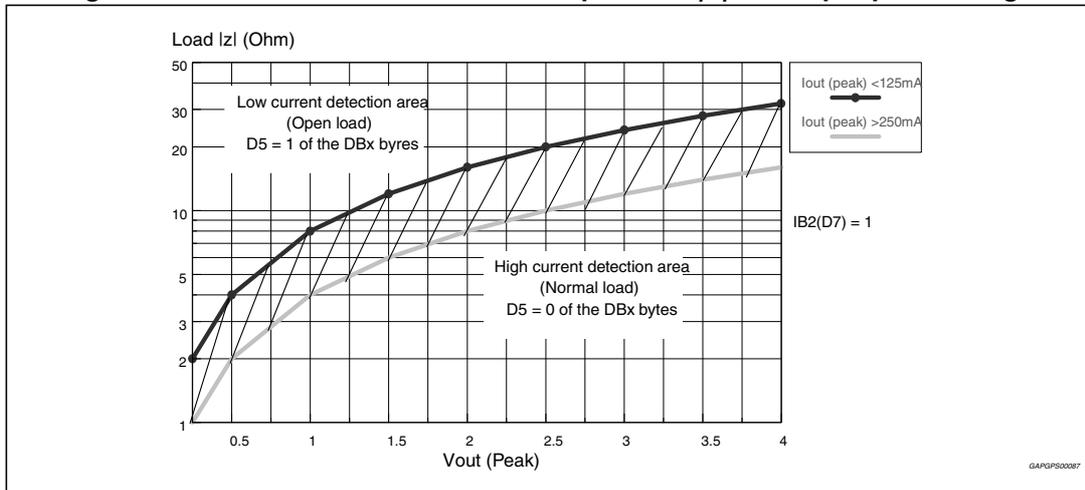


Figure 14. Current detection low: load impedance |Z| vs. output peak voltage



5 Output DC offset detection

The TDA75616LV can detect any DC output offset exceeding ± 2 V. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating. Every time the power amplifier switches on, the SSR automatically mutes the device in case of offset. In play mode, the offset is signalled out on I²C bus.

5.1 Offset detection and mute at start-up, SSR (Speaker Safety Routine)

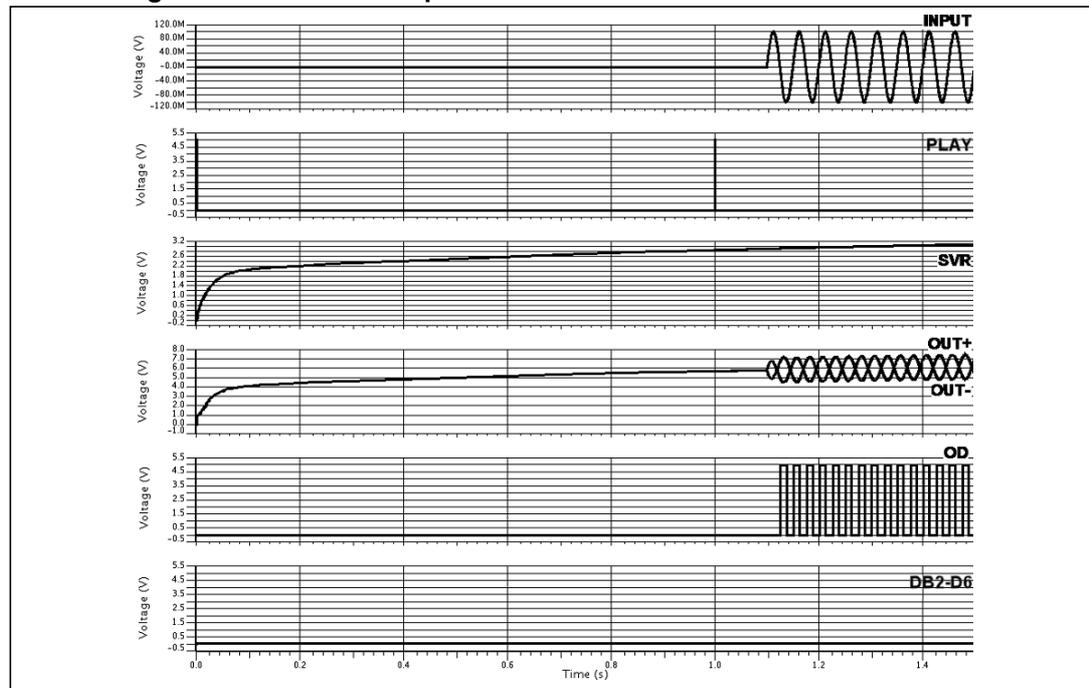
TDA75616LV embeds a speaker safety routine in order to protect the speakers in case of big output offset. This protection mechanism can automatically mute the device within 40 ms when it detects an offset bigger than 2 V at the output. No external circuit is required for this feature.

The SSR requires the MCU to turn on the audio power amplifier in a proper sequence. The MCU should at first turn on the device in MUTE condition and, after a suitable time to completely power on the device, which is about 1 s, send a PLAY command to it and make sure there is no signal applied to any of the inputs for at least 100 ms.

The SSR can be enabled acting on IB2-D0 bit.

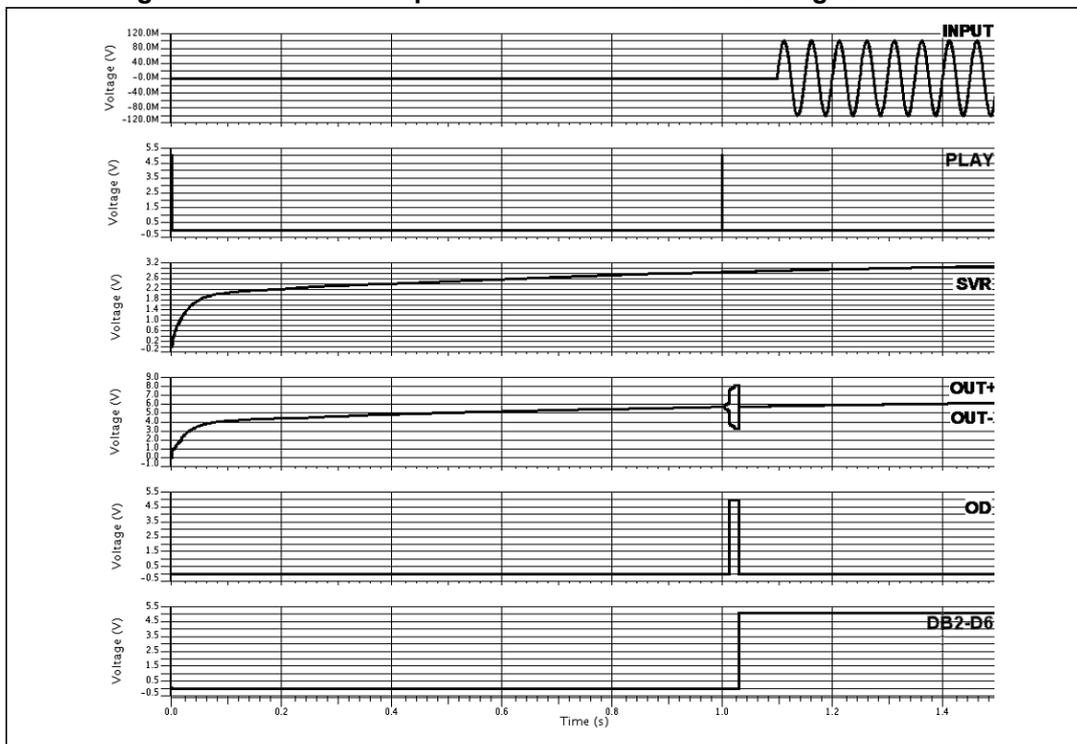
See [Figure 15](#). The power amplifier switches on and no input signal is applied. After 1 s the SVR is fully charged and the output dc voltage is set. The MCU sends the PLAY command and the offset, on all the channels, is checked. In case the detected offset is null or, anyhow, lower than 2 V, the power amplifier is kept alive and the audio signal can be applied after 100 ms.

Figure 15. Power on sequence with a detected offset lower than 2 V



Look at the *Figure 16*. The power amplifier switches on and no input signal is applied. After 1 s the SVR is fully charged and the output dc voltage is set. The MCU sends the PLAY command and the offset, on all the channels, is checked. If an offset bigger than 2 V is detected, the power amplifier is switched off within 40 ms.

Figure 16. Power on sequence with a detected offset higher than 2 V



This action is pointed out on the I²C bus, bit DB2-D6. This flag is seen by the microcontroller which can take proper actions.

A standby command (hardware or by I²C) can reset the power amplifier

5.2 Offset detection in normal operation

It is a diagnostics function which has to be performed with low-level output AC signal (or $V_{in} = 0$).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if it is persistent of all the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

6 Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I²C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn-on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 Ω speaker unconnected is considered as double fault.

Table 6. Double fault table for turn on diagnostic

	S. GND	S. Vs	S. Across L.	Open L.
S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. Vs	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	S. Across L.	N.A.
Open L.	/	/	/	Open L. (*)

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive Car Radio Turn-on).

6.1 Faults availability

All the results coming from I²C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out.

To guarantee always resident functions, every kind of diagnostic cycle (Turn-on, Permanent, Offset) is activated again after any I²C reading operation. So, when the micro reads the I²C, a new cycle will be able to start, but the read data will come from the previous diag. cycle (i.e. The device is in Turn-on state, with a short to Gnd, then the short is removed and micro reads I²C. The short to GND is still present in bytes, because it is the result of the previous cycle. If another I²C reading operation occurs, the bytes do not show the short). In general to observe a change in Diagnostic bytes, two I²C reading operations are necessary.

7 Thermal protection

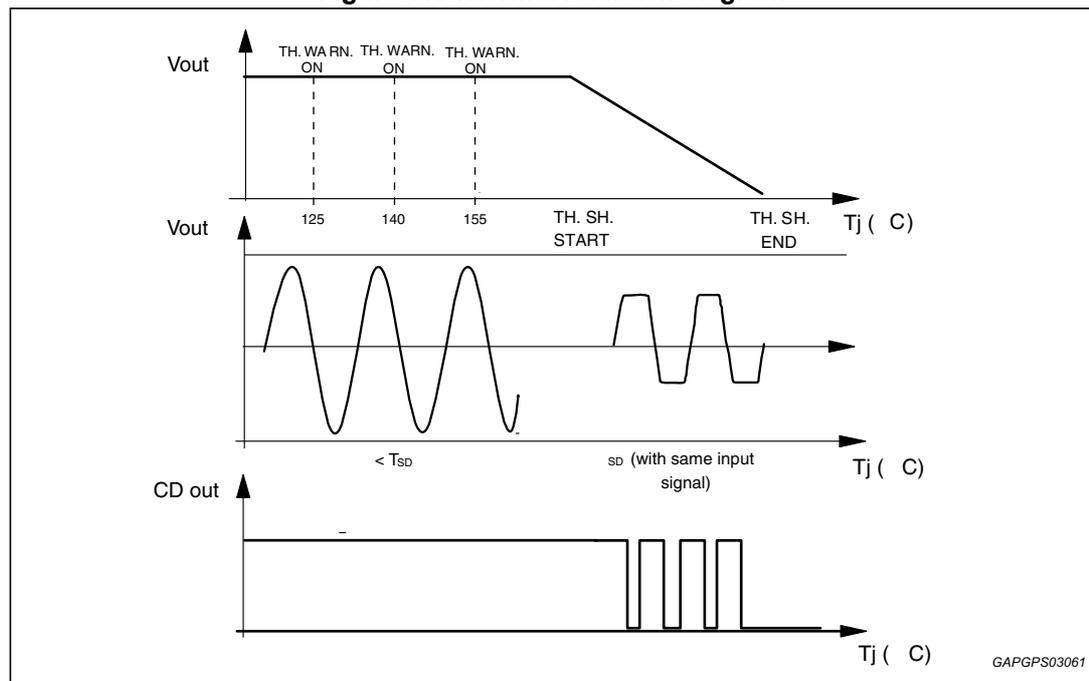
Thermal protection is implemented through thermal foldback (*Figure 17*).

Thermal foldback begins limiting the audio input to the amplifier stage as the junction temperatures rise above the normal operating range. This effectively limits the output power capability of the device thus reducing the temperature to acceptable levels without totally interrupting the operation of the device.

The output power will decrease to the point at which thermal equilibrium is reached. Thermal equilibrium will be reached when the reduction in output power reduces the dissipated power such that the die temperature falls below the thermal foldback threshold. Should the device cool, the audio level will increase until a new thermal equilibrium is reached or the amplifier reaches full power. Thermal foldback will reduce the audio output level in a linear manner.

Three thermal warning are available through the I²C bus data. After thermal shut down threshold is reached, the CD could toggle (as shown in *Figure 17*) or stay low, depending on signal level.

Figure 17. Thermal foldback diagram



7.1 Fast muting

The muting time can be shortened to less than 1.5 ms by setting (IB2) D5 = 1. This option can be useful in transient battery situations (i.e. during car engine cranking) to quickly turnoff the amplifier to avoid any audible effects caused by noise/transients being injected by preamp stages. The bit must be set back to “0” shortly after the mute transition.

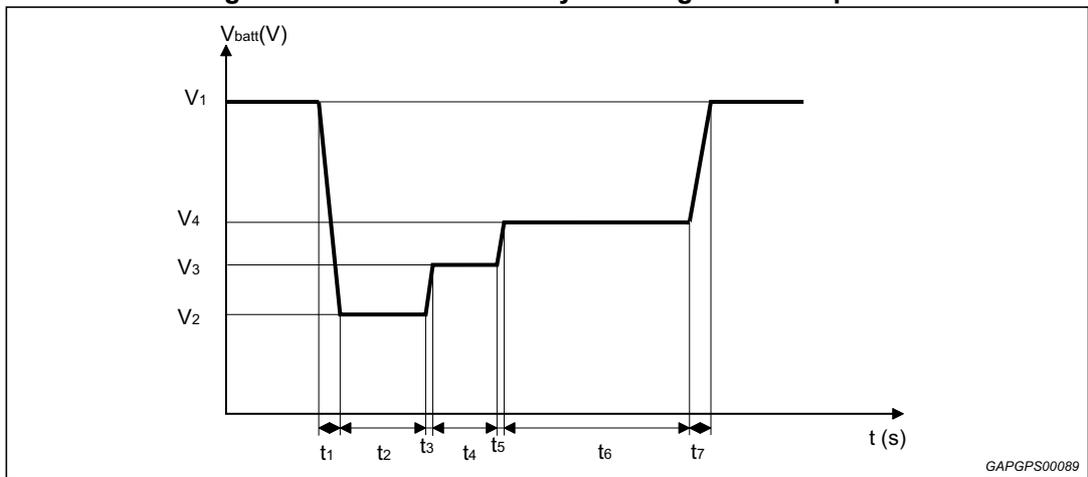
8 Battery transitions management

8.1 Low voltage operation (“start stop”)

The most recent OEM specifications require automatic stop of car engine at traffic light, in order to reduce emissions of polluting substances. The TDA75616LV, thanks to its innovating design, allows to go on playing sound when battery falls down to 6/7 V during such conditions, without producing pop noise. The maximum system power will be reduced accordingly.

Supported battery cranking curves are shown below, indicating the shape and duration of allowed battery transitions.

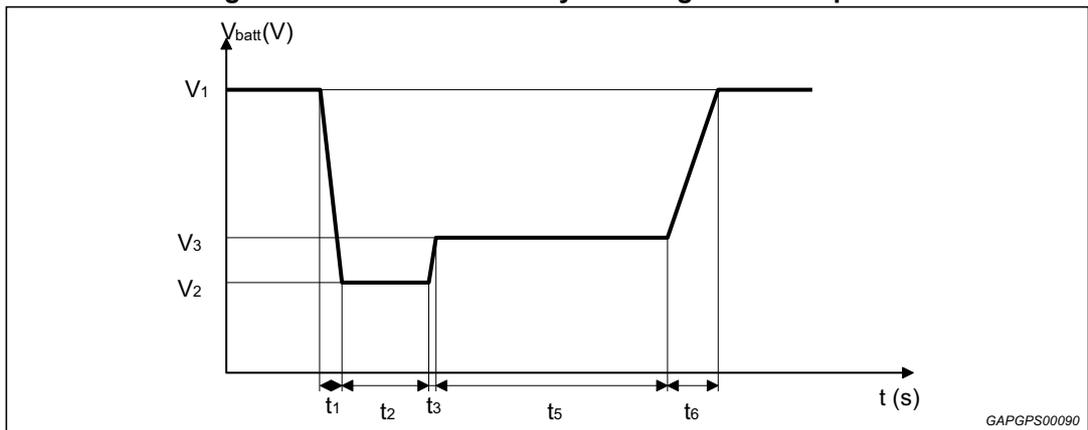
Figure 18. Worst case battery cranking curve sample 1



$V_1 = 12\text{ V}; V_2 = 6\text{ V}; V_3 = 7\text{ V}; V_4 = 8\text{ V}$

$t_1 = 2\text{ ms}; t_2 = 50\text{ ms}; t_3 = 5\text{ ms}; t_4 = 300\text{ ms}; t_5 = 10\text{ ms}; t_6 = 1\text{ s}; t_7 = 2\text{ ms}$

Figure 19. Worst case battery cranking curve sample 2



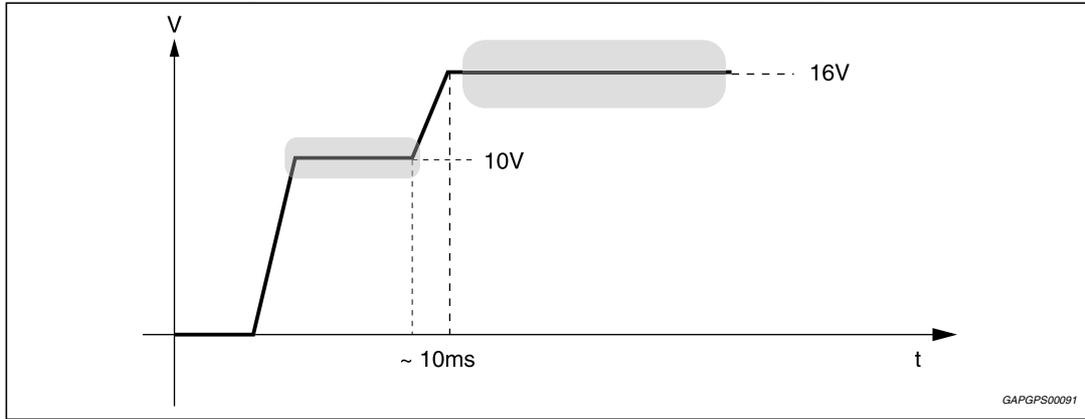
$V_1 = 12\text{ V}; V_2 = 6\text{ V}; V_3 = 7\text{ V}$

$t_1 = 2\text{ ms}; t_2 = 5\text{ ms}; t_3 = 15\text{ ms}; t_4 = 1\text{ s}; t_5 = 50\text{ ms}$

8.2 Advanced battery management

In addition to compatibility with low V_{batt} , the TDA75616LV is able to sustain upwards fast battery transitions (like the one showed in [Figure 20](#)) without causing unwanted audible effect, thanks to the innovative circuit topology.

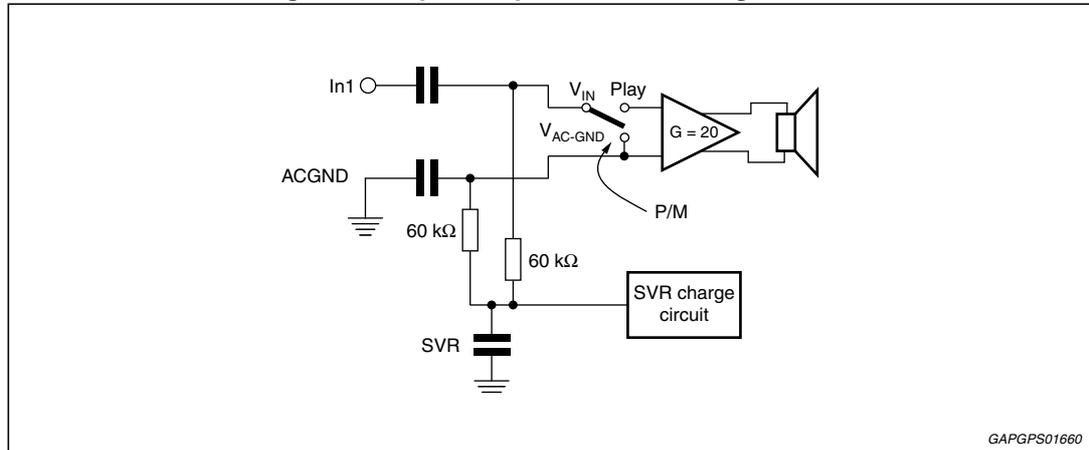
Figure 20. Upwards fast battery transitions diagram



9 Application suggestion

9.1 Inputs impedance matching

Figure 21. Inputs impedance matching circuit



The above is a simplified input stage where it is visible that the AC-GND impedance ($60\text{ k}\Omega$) is the same as the input one.

During battery variations the SVR voltage is moved and V_{IN} and V_{AC-GND} tracks it through the two R-C networks.

Any differences of this two time constants can produce a differential input voltage, which can produce a noise.

Consequently, any additional passive components at the inputs (other than the input capacitors) such as series resistance or R dividers must be compensated for at AC-GND level by connecting the same equivalent resistance in series to C_{AC-GND} .

A good 1:1 matching ($Z_{AC-GND} = Z_{IN}$) is therefore recommended to minimize pop. This rule applies to both "4-CH operation" and "2-CH operation", as any unused input has to be AC-grounded (through the same C_{IN} value).