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MC56F847XX

MC56F847XX

Supports the 56F84789VLL, 56F84786VLK, 56F84769VLL, 56F84766VLK, 56F84763VLH

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. Each device combines, on a single chip, the processing power of a DSP and the functionality of an MCU with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - Smart sensors
  - Fire and security systems
  - Switched-mode power supply and power management
  - Uninterruptible Power Supply (UPS)
  - Solar and wind power generator
  - Power metering
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Handheld power tools
  - Circuit breaker
  - Medical device/equipment
  - Instrumentation
  - Lighting

- DSC based on 32-bit 56800EX core
  - Up to 100 MIPS at 100 MHz core frequency
  - DSP and MCU functionality in a unified, C-efficient architecture

- On-chip memory
  - Up to 288 KB (256 KB + 32 KB) flash memory, including up to 32 KB FlexNVM
  - Up to 32 KB RAM
  - Up to 2 KB FlexRAM with EEE capability
  - 100 MHz program execution from both internal flash memory and RAM
  - On-chip flash memory and RAM can be mapped into both program and data memory spaces

- Analog
  - Two high-speed, 8-channel, 12-bit ADCs with dynamic x2, x4 programmable amplifier
  - One 20-channel, 16-bit ADC
  - Four analog comparators with integrated 6-bit DAC references
  - One 12-bit DAC

- PWMs and timers
  - Two eFlexPWM modules with up to 24 PWM outputs, one including 8 channels with high resolution NanoEdge placement
  - Two 16-bit quad timer (2 x 4 16-bit timers)
  - Two Periodic Interval Timers (PITs)
  - One Quadrature Decoder
  - Two Programmable Delay Blocks (PDBs)

- Communication interfaces
  - Three high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to three queued SPI (QSPI) modules
  - Two SMBus-compatible I2C ports
  - One flexible controller area network (FlexCAN) module

- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)

- Clocks
  - Two on-chip relaxation oscillators: 8 MHz (400 kHz at standby mode) and 32 kHz
  - Crystal / resonator oscillator

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except RESETB pin)

- LQFP packages:
  - 64-pin
  - 80-pin
  - 100-pin

Table of Contents

1 Overview

1.1 MC56F844xx/5xx/7xx product family

The following table lists major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844xx/5xx/7xx family

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
Core freq. (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC Channels (ADCA and ADCB)	2x8	2x8	2x8	2x8	2x8	2x8	2x5	2x8	2x5	2x8	2x8	2x8	2x8	2x8	2x8	2x5	2x8	2x5
12-bit Cyclic ADC Conversion time (ADCA and ADCB)	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	300 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns	600 ns
16-bit SAR ADC (with Temperature Sensor) channels (ADCC)	16	10	16	10	8	8	–	8	–	16	10	16	10	–	8	–	8	–
PWMA High-res channels	8	8	8	8	8	8	6	8	6	0	0	0	0	0	0	0	0	0

Table continues on the next page...

Table 1. 56F844xx/5xx/7xx family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
PWMA Std channels	4	1	4	1	1	1	0	1	0	12	12	12	12	9	9	6	9	6
PWMA Input capture channels	12	9	12	9	9	9	6	9	6	12	12	12	12	9	9	6	9	6
PWMB Std channels	12	9 [2]	12	9 [2]	–	–	–	–	–	12	9 [2]	12	9 [2]	–	–	–	–	–
PWMB Input capture channels	12	7	12	7	–	–	–	–	–	12	7	12	7	–	–	–	–	–
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	–	–	1	–	–	–	–
Quad Decoder	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	1	1	1	1	1	3	2	3	2	1	1	1	1	1
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total includes FlexNVM and assumes no FlexNVM is used with FlexRAM for EEPROM.
2. The outputs of PWMB_3A and PWM_3B are available through the on-chip inter-module crossbar.

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Supports concurrent instruction fetches in the same cycle, and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic

- 32-bit internal primary data buses support 8-bit, 16-bit, and 32-bit data movement, plus addition, subtraction, and logical operations
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, which effectively supports DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers correspond to nine address registers (R0, R1, R2, R3, R4, R5, N, N3, M01)
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions enable compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack, with the stack's depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation parameters

- Up to 100 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-chip memory and memory protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.

    - Concurrent accesses provide increased performance.
    - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
    - Up to 144 KW program/data flash memory, including FlexNVM
    - Up to 16 KW dual port data/program RAM
    - Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
    - Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

1.5 Interrupt Controller

- Five interrupt priority levels
    - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
    - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
    - Interrupt level 3 is highest priority and non-maskable. Its sources include:
        - Illegal instructions
        - Hardware stack overflow
        - SWI instruction
        - EOnce interrupts
        - Misaligned data accesses
    - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Two PWM modules contain 4 identical submodules, each with up to 3 outputs per submodule, and up to 100 MHz PWM operating clock
- 16 bits of resolution for center, edge-aligned, and asymmetrical PWMs

- PWMA with NanoEdge high resolution
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - 390 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled.
  - Fractional clock digital dithering: 5-bit digital fractional clock accumulation for enhanced resolution of PWM period and edge placement, which is effectively equivalent to 390 ps resolution in the overall accumulative period.
- PWM outputs can be configured as complementary output pairs or independent outputs
- PWMB with 10 ns resolution at 100 MHz PWM operation clock
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input:
  - Channels not used for PWM generation can be used for buffered output compare functions.
  - Channels not used for PWM generation can be used for input capture functions.
  - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware (or other PWM) is supported.
- Double-buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware.
- Support for double-switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event.
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs):
  - 2 x 8-channel external inputs

    - Built-in x1, x2, x4 programmable gain pre-amplifier
    - Maximum ADC clock frequency up to 20 MHz, having period as low as a 50-ns
    - Single conversion time of 8.5 ADC clock cycles
    - Additional conversion time of 6 ADC clock cycles
- Support of analog inputs for single-ended and differential conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by *any* module connected to the internal crossbar module, such as PWM, timer, GPIO, and comparator modules.
- Support for simultaneous triggering and software-triggering conversions
- Support for a multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results.
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, comparators, quad-timers, eFlexPWMs, PDBs, EWM, quadrature decoder, and select I/O pins
- User-defined input/output pins for all modules connected to the crossbar
- DMA request and interrupt generation from the crossbar
- Write-once protection for all registers
- AND-OR-INVERT function provides a universal Boolean function generator that uses a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution

- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.6 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.6.7 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 25 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers

- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter

1.6.10 Flex Controller Area Network (FlexCAN) module

- Clock source from PLL or XOSC/CLKIN
- Implementation of CAN protocol Version 2.0 A/B
- Standard and extended data frames
- Data length of 0 to 8 bytes
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers: each Message Buffer can be configured as receive or transmit, and supports standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode, supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

1.6.11 Computer Operating Properly (COP) watchdog

- Programmable timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected

- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.12 Power supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (V_{DD} > 2.1 V)
- Brownout reset (V_{DD} < 1.9 V)
- Critical warn low-voltage interrupt (LVI2.0)
- Peripheral low-voltage interrupt (LVI2.7)

1.6.13 Phase-locked loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.14 Clock sources

1.6.14.1 On-chip oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.14.2 Crystal oscillator

- Support for both high ESR crystal oscillator (ESR greater than 100 Ω) and ceramic resonator
- Operating frequency: 4–16 MHz

1.6.15 Cyclic Redundancy Check (CRC) generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation

- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance (except RESETB pin)
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins (except JTAG and RESETB) default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block diagrams

The 56800EX core is based on a modified dual Harvard-style architecture, consisting of three execution units operating in parallel, and allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

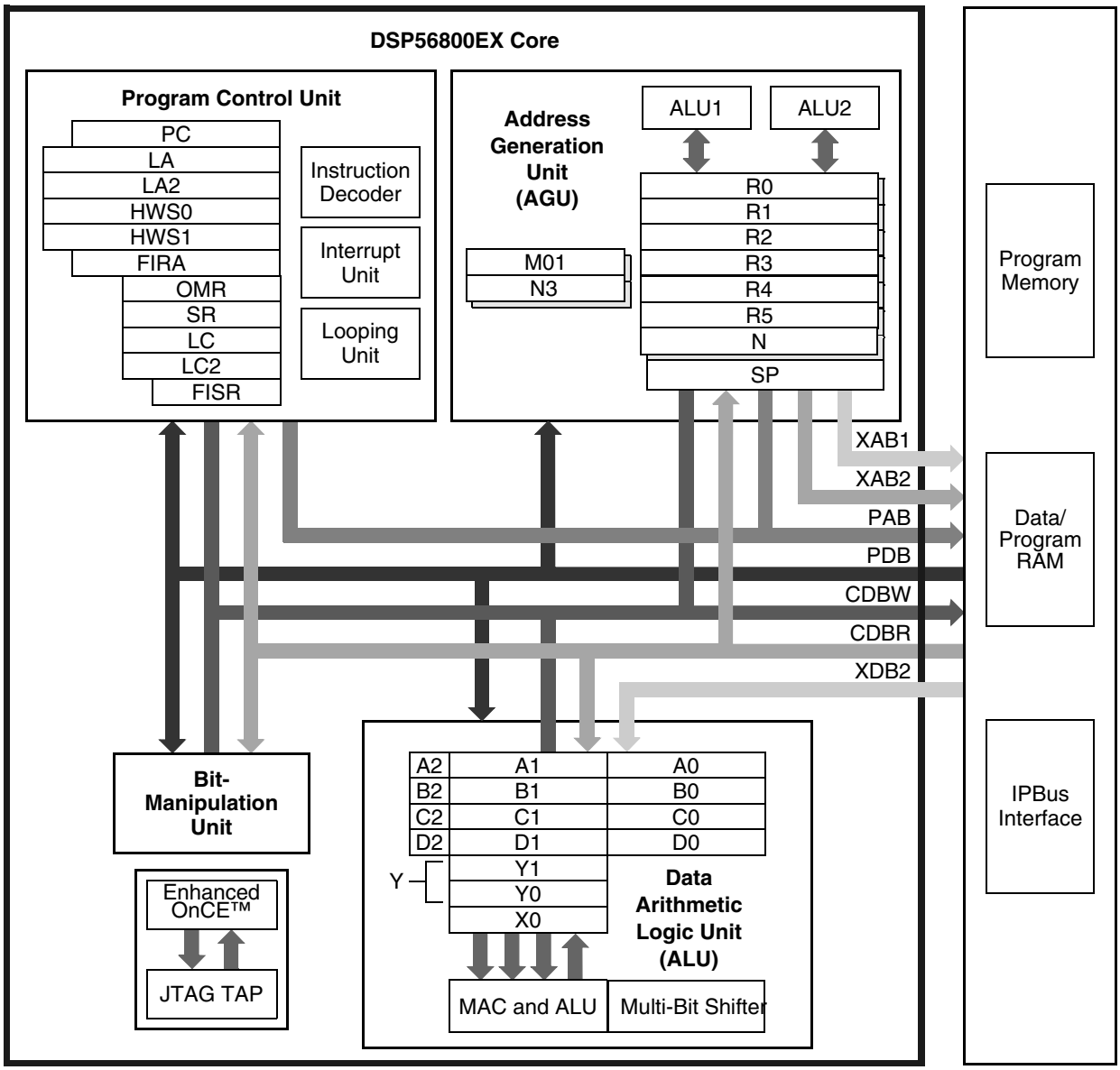

Figure 1. 56800EX basic block diagram

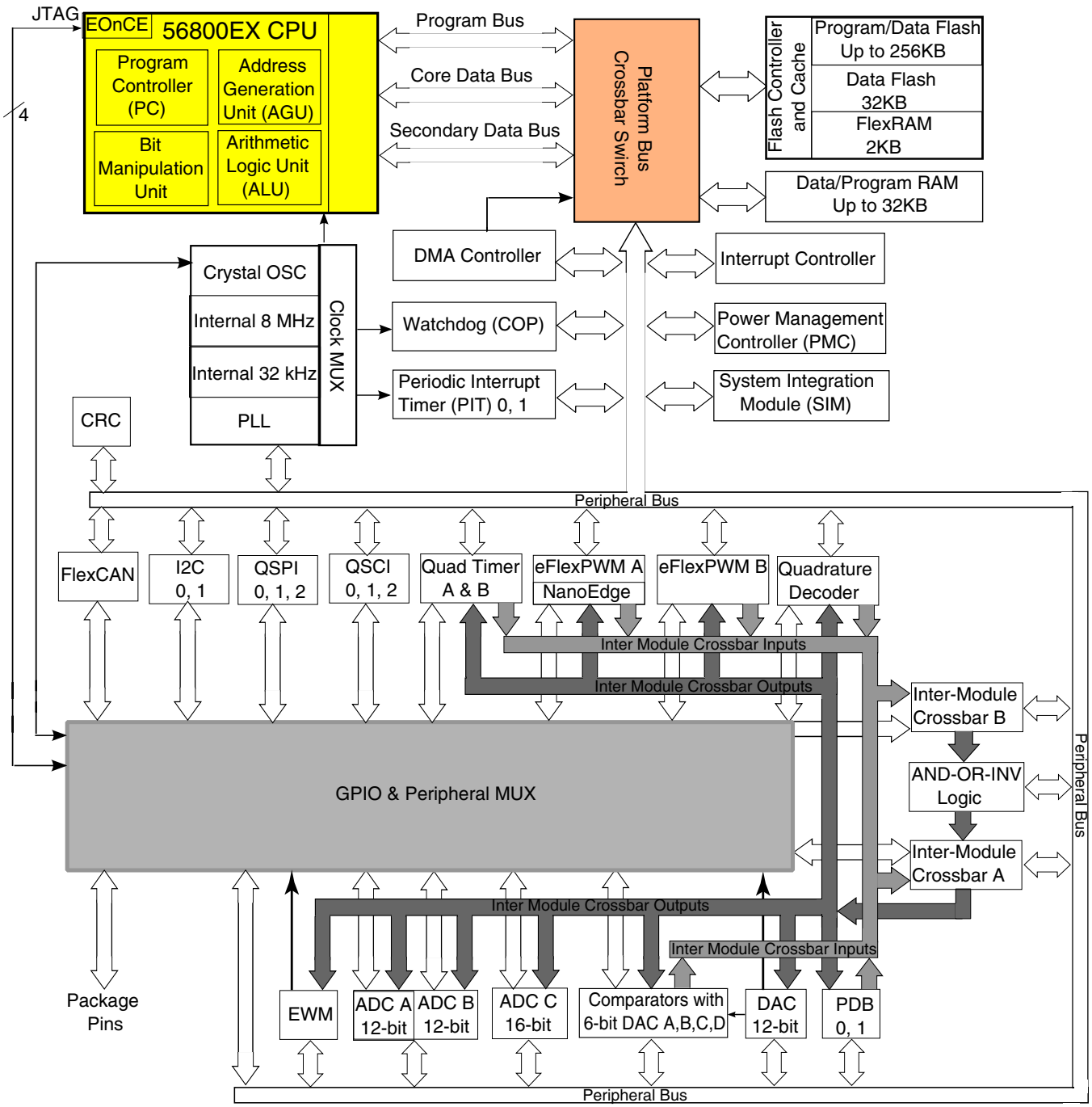

Figure 2. System diagram

2 MC56F847xx signal and pin descriptions

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through the GPIO module peripheral enable registers (GPIO_x_PER) and the SIM module GPIO peripheral select (GPSx) registers. All GPIO ports can be individually programmed as an input or output (using bit manipulation).

- There are 2 PWM modules: PWM**A**, PWM**B**. Each PWM module has 4 submodules: PWMA has PWMA_**0**, PWMA_**1**, PWMA_**2**, PWMA_**3**; PWMB has PWMB_0, PWMB_1, PWMB_2, PWMB_3. Each PWM module's submodules have 3 pins (A, B, X) each, with the syntax for the pins being PWMA_0**A**, PWMA_0**B**, PWMA_0**X**, and PWMA_1A, PWMA_1B, PWMA_1X, and so on. Each submodule pin can be configured as a PWM output or as a capture input.
- PWMA_FAULT0, PWMA_FAULT1, and similar signals are inputs used to disable selected PWMA (or PWMB) outputs, in cases where the fault conditions originate off-chip.
- EWM_OUT_B is the output of the External Watchdog Module (EWM), and is active low (denoted by the "_B" part of the syntax).

For the MC56F84**7XX** products, which use 64-pin LQFP, 80-pin LQFP, and 100-pin LQFP packages:

Table 2. Signal descriptions

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
V_{DD}	7	-	-	Supply	Supply	I/O Power — Supplies 3.3 V power to the chip I/O interface.
V_{DD}	43	35	29			
V_{DD}	67	54	44			
V_{DD}	96	76	60			
V_{SS}	8	-	-	Supply	Supply	I/O Ground — Provide ground for the device I/O interface.
V_{SS}	15	11	-			
V_{SS}	44	36	30			
V_{SS}	66	53	43			
V_{SS}	97	77	61			
V_{DDA}	31	26	22	Supply	Supply	Analog Power — Supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	32	27	23	Supply	Supply	Analog Ground — Supplies an analog ground to the analog modules. It must be connected to a clean power supply.

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
V_{CAP}	16	12	-	On-chip regulator output voltage	On-chip regulator output voltage	Connect a 2.2uF or greater bypass capacitor between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. V_{CAP} is used to observe core voltage.
V_{CAP}	35	30	26			
V_{CAP}	93	73	57			
TDI	100	80	64	Input	Input, internal pullup enabled	Test Data Input — Provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TDI.
(GPIOD0)				Input/ Output	Input, internal pullup enabled	GPIO Port D0
TDO	98	78	62	Output	Output	Test Data Output — This tri-stateable pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK. After reset, the default state is TDO.
(GPIOD1)				Input/ Output	Input, internal pullup enabled	GPIO Port D1
TCK	1	1	1	Input	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. After reset, the default state is TCK.
(GPIOD2)				Input/ Output	Input, internal pullup enabled	GPIO Port D2

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
TMS	99	79	63	Input	Input, internal pullup enabled	Test Mode Select Input — Used to sequence the JTAG TAP controller state machine. It is sampled on the rising edge of TCK and has an internal pullup resistor. After reset, the default state is TMS. **NOTE:** Always tie the TMS pin to V_{DD} through a 2.2K resistor, if needed to keep an on-board debug capability. Otherwise, tie the TMS pin directly to V_{DD}.
(GPIOD3)				Input/ Output	Input, internal pullup enabled	GPIO Port D3
$\overline{\text{RESET}}$or **RESETB**	2	2	2	Input	Input, internal pullup enabled (This pin is 3.3V only.)	Reset — A direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronously with the internal clocks after a fixed number of internal clocks. After reset, the default state is $\overline{\text{RESET}}$. To filter noise on the RESETB pin, install a capacitor (up to 0.1 uF) on it.
(GPIOD4)				Input/ Open-drain Output	Input, internal pullup enabled	GPIO Port D4 — Can be individually programmed as an input or open-drain output pin. $\overline{\text{RESET}}$ functionality is disabled in this mode and the device can be reset only through Power-On Reset (POR), COP reset, or software reset.
GPIOA0	22	17	13	Input/ Output	Input	GPIO Port A0; after reset, the default state is GPIOA0.
(ANA0&CMPA_IN3)				Input		ANA0 is input to channel 0 of ADCA; CMPA_IN3 is input 3 of analog comparator A. When used as an analog input, the signal goes to both places (ANA0 and CMPA_IN3), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
(CMPC_O)				Output		Analog comparator C output
GPIOA1	23	18	14	Input/ Output	Input	GPIO Port A1: After reset, the default state is GPIOA1.
(ANA1&CMPA_IN0)				Input		ANA1 is input to channel 1 of ADCA; CMPA_IN0 is input 0 of analog comparator A. When used as an analog input, the signal goes to both places (ANA1 and CMPA_IN0), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOA2	24	19	15	Input/ Output	Input	GPIO Port A2: After reset, the default state is GPIOA2.
(ANA2&VREFHA&CMPA_IN1)				Input		ANA2 is input to channel 2 of ADCA; VREFHA is the reference high of ADCA; CMPA_IN1 is input 1 of analog comparator A. When used as an analog input, the signal goes to both places (ANA2 and CMPA_IN1), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin. This input can be configured as either ANA2 or VREFHA using the ADCA control register.
GPIOA3	25	20	16	Input/ Output	Input	GPIO Port A3: After reset, the default state is GPIOA3.
(ANA3&VREFLA&CMPA_IN2)				Input		ANA3 is input to channel 3 of ADCA; VREFLA is the reference low of ADCA; CMPA_IN2 is input 2 of analog comparator A. When used as an analog input, the signal goes to both places (ANA3 and CMPA_IN2), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin. This input can be configured as either ANA3 or VREFLA using the ADCA control register.
GPIOA4	21	16	12	Input/ Output	Input	GPIO Port A4: After reset, the default state is GPIOA4.
(ANA4&ANC8&CMPD_IN0)				Input		ANA4 is input to channel 4 of ADCA; ANC8 is input to channel 8 of ADCC; CMPD_IN0 is input 0 of analog comparator D. When used as an analog input, the signal goes to all three places (ANA4 and ANC8 and CMPA_IN0), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA5	20	15	11	Input/ Output	Input	GPIO Port A5: After reset, the default state is GPIOA5.
(ANA5&ANC9)				Input		ANA5 is input to channel 5 of ADCA; ANC9 is input to channel 9 of ADCC. When used as an analog input, the signal goes to both places (ANA5 and ANC9), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOA6	19	14	10	Input/ Output	Input	GPIO Port A6: After reset, the default state is GPIOA6.
(ANA6&ANC10)				Input		ANA6 is input to channel 6 of ADCA; ANC10 is input to channel 10 of ADCC. When used as an analog input, the signal goes to both places (ANA6 and ANC10), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA7	17	13	9	Input/ Output	Input	GPIO Port A7: After reset, the default state is GPIOA7.
(ANA7&ANC11)				Input		ANA7 is input to channel 7 of ADCA; ANC11 is input to channel 11 of ADCC. When used as an analog input, the signal goes to both places (ANA7 and ANC11), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA8	18	-	-	Input/ Output	Input	GPIO Port A8: After reset, the default state is GPIOA8.
(ANC16&CMPD_IN1)				Input		ANC16 is input to channel 16 of ADCC; CMPD_IN1 is input 1 of analog comparator D. When used as an analog input, the signal goes to both places (ANC16 and CMPD_IN1), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA9	14	-	-	Input/ Output	Input	GPIO Port A9: After reset, the default state is GPIOA9.
(ANC17&CMPD_IN2)				Input		ANC17 is input to channel 17 of ADCC; CMPD_IN2 is input 2 of analog comparator D. When used as an analog input, the signal goes to both places (ANC17 and CMPD_IN2), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOA10	13	-	-	Input/ Output	Input	GPIO Port A10: After reset, the default state is GPIOA10.
(ANC18&CMPD_IN3)				Input		ANC18 is input to channel 18 of ADCC; CMPD_IN3 is input 3 of analog comparator D. When used as an analog input, the signal goes to both places (ANC18 and CMPD_IN3), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOA11	37	32	-	Input/ Output	Input	GPIO Port A11: After reset, the default state is GPIOA11.
(ANC19&VREFHC)				Input		ANC19 is input to channel 19 of ADCC. VREFHC is the analog reference high of ADCC.
GPIOB0	33	28	24	Input/ Output	Input	GPIO Port B0: After reset, the default state is GPIOB0.
(ANB0&CMPB_IN3)				Input		ANB0 is input to channel 0 of ADCB; CMPB_IN3 is input 3 of analog comparator B. When used as an analog input, the signal goes to both places (ANB0 and CMPB_IN3), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOB1	34	29	25	Input/ Output	Input	GPIO Port B1: After reset, the default state is GPIOB1.
(ANB1&CMPB_IN0)				Input		ANB1 is input to channel 1 of ADCB; CMPB_IN0 is input 0 of analog comparator B. When used as an analog input, the signal goes to both places (ANB1 and CMPB_IN0), but the glitch on this pin during ADC sampling may interfere with other analog inputs shared on this pin.
GPIOB2	36	31	27	Input/ Output	Input	GPIO Port B2: After reset, the default state is GPIOB2.
(ANB2&VREFHB&CMPC_IN3)				Input		ANB2 is input to channel 2 of ADCB; VREFHB is the reference high of ADCB; CMPC_IN3 is input 3 of analog comparator C. When used as an analog input, the signal goes to both places (ANB2 and CMPC_IN3), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin. This input can be configured as either ANB2 or VREFHB using the ADCB control register.
GPIOB3	42	34	28	Input/ Output	Input	GPIO Port B3: After reset, the default state is GPIOB3.
(ANB3&VREFLB&CMPC_IN0)				Input		ANB3 is input to channel 3 of ADCB; VREFLB is the reference low of ADCB; CMPC_IN0 is input 0 of analog comparator C. When used as an analog input, the signal goes to both places (ANB3 and CMPC_IN0), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin. This input can be configured as either ANB3 or VREFLB using the ADCB control register.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOB4	30	25	21	Input/ Output	Input	GPIO Port B4: After reset, the default state is GPIOB4.
(ANB4&ANC12&CMPC_IN1)				Input		ANB4 is input to channel 4 of ADCB; ANC12 is input to channel 12 of ADCC; CMPC_IN1 is input 1 of analog comparator C. When used as an analog input, the signal goes to all three places (ANB4 and ANC12 and CMPC_IN1), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin.
GPIOB5	29	24	20	Input/ Output	Input	GPIO Port B5: After reset, the default state is GPIOB5.
(ANB5&ANC13&CMPC_IN2)				Input		ANB5 is input to channel 5 of ADCB; ANC13 is input to channel 13 of ADCC; CMPC_IN2 is input 2 of analog comparator C. When used as an analog input, the signal goes to all three places (ANB5 and ANC13 and CMPC_IN2), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin.
GPIOB6	28	23	19	Input/ Output	Input	GPIO Port B6: After reset, the default state is GPIOB6.
(ANB6&ANC14&CMPB_IN1)				Input		ANB6 is input to channel 6 of ADCB; ANC14 is input to channel 14 of ADCC; CMPB_IN1 is input 1 of analog comparator B. When used as an analog input, the signal goes to all three places (ANB6 and ANC14 and CMPB_IN1), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin.
GPIOB7	26	21	17	Input/ Output	Input	GPIO Port B7: After reset, the default state is GPIOB7.
(ANB7&ANC15&CMPB_IN2)				Input		ANB7 is input to channel 7 of ADCB; ANC15 is input to channel 14 of ADCC; CMPB_IN2 is input 2 of analog comparator B. When used as an analog input, the signal goes to all three places (ANB7 and ANC15 and CMPB_IN2), but the glitch during ADC sampling on this pin may interfere with other analog inputs shared on this pin.
GPIOB8	38	33	33	Input/ Output	Input	GPIO Port B8: After reset, the default state is GPIOB8.
(ANC20&VREFLC)				Input		ANC20 is input to channel 20 of ADCC; VREFLC is the reference low of ADCC .

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOB9	39	-	-	Input/ Output	Input	GPIO Port B9: After reset, the default state is GPIOB9.
(ANC21)				Input		Input to channel 21 of ADCC
(XB_IN9)				Input		Crossbar module input 9
(MISO2)				Input/ Output		Master in/slave out for SPI2 —In master mode, MISO2 pin is the data input. In slave mode, MISO2 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOB10	40	-	-	Input/ Output	Input	GPIO Port B10: After reset, the default state is GPIOB10.
(ANC22)				Input		Input to channel 22 of ADCC
(XB_IN8)				Input		Crossbar module input 8
(MOSI2)				Input/ Output		Master out/slave in for SPI2— In master mode, MOSI2 pin is the data output. In slave mode, MOSI2 pin is the data input.
GPIOB11	41	-	-	Input/ Output	Input	GPIO Port B11: After reset, the default state is GPIOB11.
(ANC23)				Input		Input to channel 23 of ADCC
(XB_IN7)				Input		Crossbar module input 7
(SCLK2)				Input/ Output		SPI2 serial clock — In master mode, SCLK2 pin is an output, clocking slaved listeners. In slave mode, SCLK2 pin is the data clock input.
GPIOC0	3	3	3	Input/ Output	Input	GPIO Port C0: After reset, the default state is GPIOC0.
(EXTAL)				Analog Input		The external crystal oscillator input (EXTAL) connects the internal crystal oscillator input to an external crystal or ceramic resonator.
(CLKIN0)				Input		External clock input.[2]
GPIOC1	4	4	4	Input/ Output	Input	GPIO Port C1: After reset, the default state is GPIOC1.
(XTAL)				Analog Output		The external crystal oscillator output (XTAL) connects the internal crystal oscillator output to an external crystal or ceramic resonator.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOC2	5	5	5	Input/ Output	Input	GPIO Port C2: After reset, the default state is GPIOC2.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single-wire operation
(TB0)				Input/ Output		Quad timer module B channel 0 input/ output
(XB_IN2)				Input		Crossbar module input 2
(CLKO0)				Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	11	9	7	Input/ Output	Input	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)				Input/ Output		Quad timer module A channel 0 input/ output
(CMPA_O)				Output		Analog comparator A output
(RXD0)				Input		SCI0 receive data input
(CLKIN1)				Input		External clock input 1
GPIOC4	12	10	8	Input/ Output	Input	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)				Input/ Output		Quad timer module A channel 1 input/ output
(CMPB_O)				Output		Analog comparator B output
(XB_IN8)				Input		Crossbar module input 8
(EWM_OUT_B)				Output		External Watchdog Module output
GPIOC5	27	22	18	Input/ Output	Input	GPIO Port C5: After reset, the default state is GPIOC5.
(DACO)				Analog Output		12-bit digital-to-analog output
(XB_IN7)				Input		Crossbar module input 7
GPIOC6	49	39	31	Input/ Output	Input	GPIO Port C6: After reset, the default state is GPIOC6
(TA2)				Input/ Output		Quad timer module A channel 2 input/ output
(XB_IN3)				Input		Crossbar module input 3
(CMP_REF)				Analog Input		Input 5 of analog comparator A and B and C and D.

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Table 2. Signal descriptions (continued)

Signal Name	100 LQFP	80 LQFP	64 LQFP	Type	State During Reset[1]	Signal Description
GPIOC7	50	40	32	Input/ Output	Input	GPIO Port C7: After reset, the default state is GPIOC7.
($\overline{SS0\_B}$)				Input/ Output		In slave mode, $\overline{SS0\_B}$ indicates to the SPI module that the current transfer is to be received.
(TXD0)				Output		SCI0 transmit data output or transmit/ receive in single-wire operation
GPIOC8	52	41	33	Input/ Output	Input	GPIO Port C8: After reset, the default state is GPIOC8.
(MISO0)				Input/ Output		Master in/slave out —In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO0 line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)				Input		SCI0 receive data input.
(XB_IN9)				Input		Crossbar module input 9
GPIOC9	53	42	34	Input/ Output	Input	GPIO Port C9: After reset, the default state is GPIOC9.
(SCLK0)				Input/ Output		SPI0 serial clock — In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input.
(XB_IN4)				Input		Crossbar module input 4
GPIOC10	54	43	35	Input/ Output	Input	GPIO Port C10: After reset, the default state is GPIOC10.
(MOSI0)				Input/ Output		Master out/slave in — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input.
(XB_IN5)				Input		Crossbar module input 5
(MISO0)				Input/ Output		Master in/slave out — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO0 line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOC11	58	47	37	Input/ Output	Input	GPIO Port C11: After reset, the default state is GPIOC11.
(CANTX)				Open-drain Output		CAN transmit data output
(SCL1)				Input/ Open-drain Output		I^2C1 serial clock
(TXD1)				Output		SCI1 transmit data output or transmit/ receive in single wire operation

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