Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# NTD4960N

# Power MOSFET
## 30 V, 55 A, Single N−Channel, DPAK/IPAK

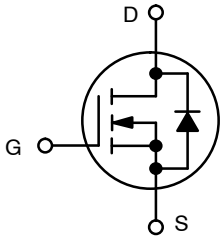
### Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Three Package Variations for Design Flexibility
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications
- CPU Power Delivery
- DC−DC Converters
- Recommended for High Side (Control)

**ON Semiconductor®**

**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 8.0 mΩ @ 10 V | 55 A |
| | 12.7 mΩ @ 4.5 V | |

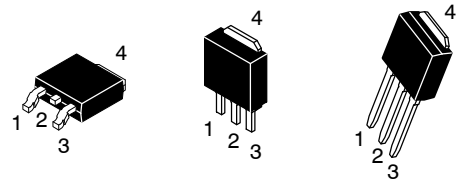



**N−CHANNEL MOSFET**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

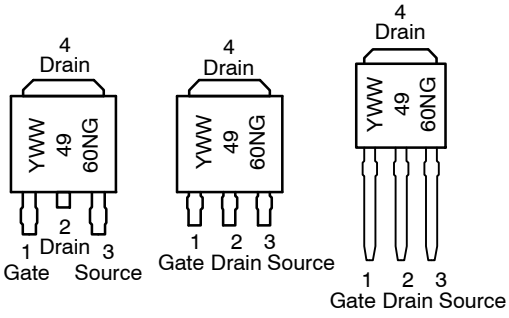
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 11.1 | A |
| | | $T_A$ = 85°C | | 8.0 | |
| Power Dissipation $R_{\theta JA}$ (Note 1) | | $T_A$ = 25°C | $P_D$ | 1.68 | W |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | ID | 8.9 | A |
| | | $T_A$ = 85°C | | 6.4 | |
| Power Dissipation $R_{\theta JA}$ (Note 2) | | $T_A$ = 25°C | $P_D$ | 1.07 | W |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $I_D$ | 55 | A |
| | | $T_C$ = 85°C | | 40 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $P_D$ | 35.71 | W |
| Pulsed Drain Current | $t_p$=10μs | $T_A$ = 25°C | $I_{DM}$ | 137 | A |
| Current Limited by Package | | $T_A$ = 25°C | $I_{DmaxPkg}$ | 45 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 29.7 | A |
| Drain to Source dV/dt | | | dV/dt | 6 | V/ns |
| Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25°C, $V_{DD}$ = 50 V, $V_{GS}$ = 10 V, $I_L$ = 32 $A_{pk}$, L = 0.1 mH, $R_G$ = 25 Ω) | | | EAS | 51.2 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.




**CASE 369AA DPAK (Bent Lead) STYLE 2** | **CASE 369AC 3 IPAK (Straight Lead)** | **CASE 369D IPAK (Straight Lead DPAK)**

### MARKING DIAGRAMS & PIN ASSIGNMENTS




Y = Year
WW = Work Week
4960N = Device Code
G = Pb−Free Package

### ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 3 | °C/W |
| Junction−to−TAB (Drain) | $R_{\theta JC-TAB}$ | 3.5 | |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 74.5 | |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 116.5 | |

1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 25 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.5 | | 2.5 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 5.0 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 30 A | | 6.1 | 8.0 | mΩ |
| | | | $I_D$ = 15 A | | 6.1 | | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 30 A | | 10 | 12.7 | mΩ |
| | | | $I_D$ = 15 A | | 10 | | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 1.5 V, $I_D$ = 15 A | | | 48 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 15 V | | | 1300 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 342 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 169 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | | | 11 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.2 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 4.0 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 4.7 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | | | 22 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 12 | | ns |
| Rise Time | $t_r$ | | | | 20 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 15 | | |
| Fall Time | $t_f$ | | | | 4.0 | | |

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Assume terminal length of 110 mils.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 11.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 7.0 | | ns |
| Rise Time | $t_r$ | | | | 17 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 22 | | |
| Fall Time | $t_f$ | | | | 3.0 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A | $T_J$ = 25°C | | 0.9 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.76 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIS/dt = 100 A/μs, $I_S$ = 30 A | | | 13.0 | | ns |
| Charge Time | $t_a$ | | | | 7.0 | | |
| Discharge Time | $t_b$ | | | | 6.0 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 4.0 | | nC |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance (Note 5) | $L_S$ | $T_A$ = 25°C | | | 2.49 | | nH |
| Drain Inductance, DPAK | $L_D$ | | | | 0.0164 | | |
| Drain Inductance, IPAK (Note 5) | $L_D$ | | | | 1.88 | | |
| Gate Inductance (Note 5) | $L_G$ | | | | 3.46 | | |
| Gate Resistance | $R_G$ | | | | 1.0 | | Ω |

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Assume terminal length of 110 mils.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTD4960NT4G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NTD4960N−1G | IPAK (Pb−Free) | 75 Units / Rail |
| NTD4960N−35G | IPAK Trimmed Lead (Pb−Free) | 75 Units / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL PERFORMANCE CURVES

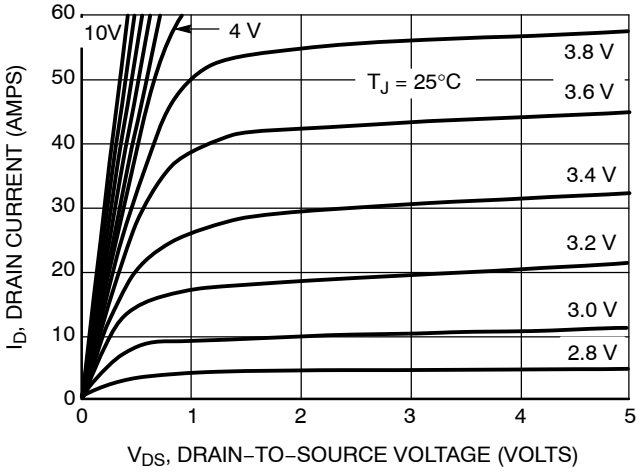



**Figure 1. On−Region Characteristics**

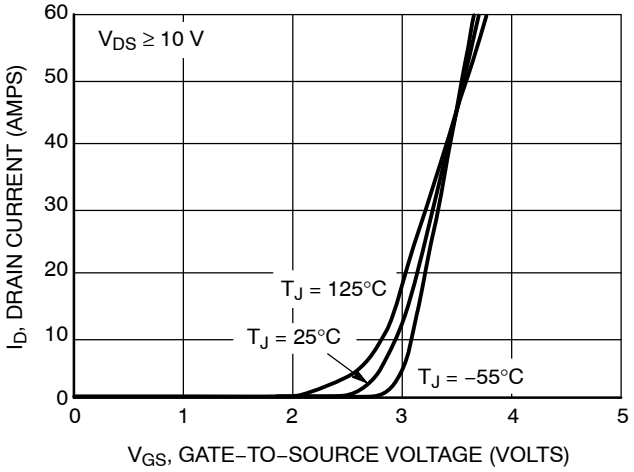



**Figure 2. Transfer Characteristics**

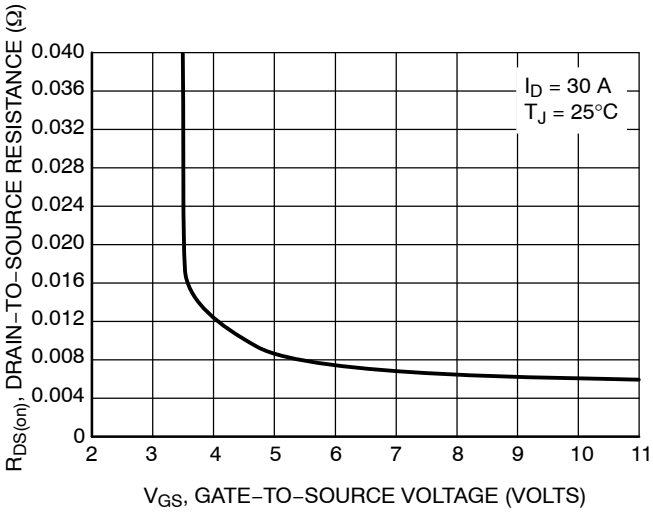



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

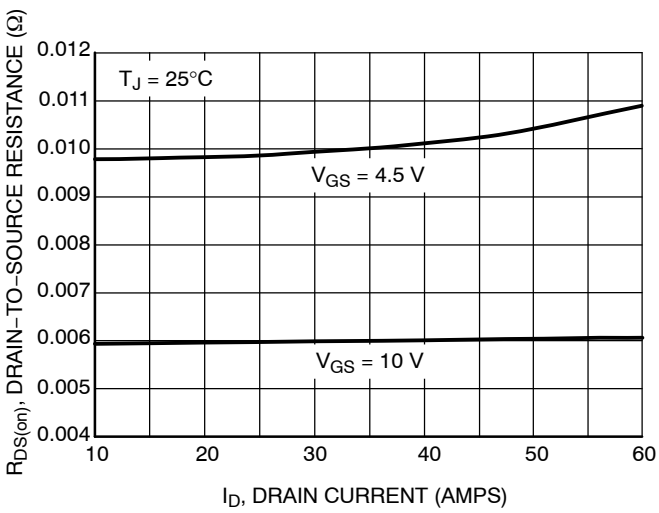



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

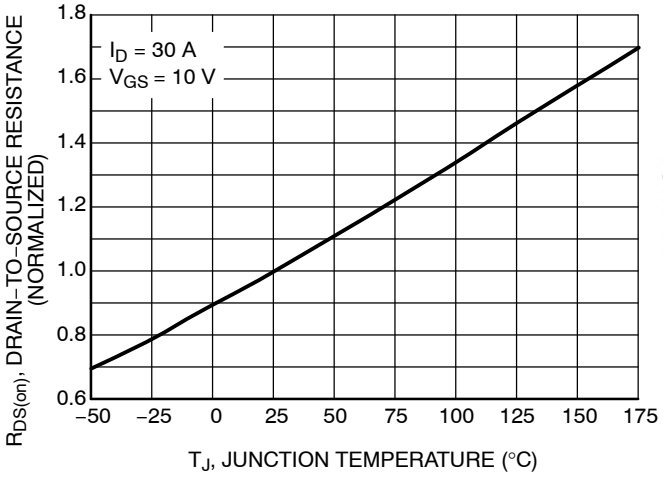



**Figure 5. On−Resistance Variation with Temperature**

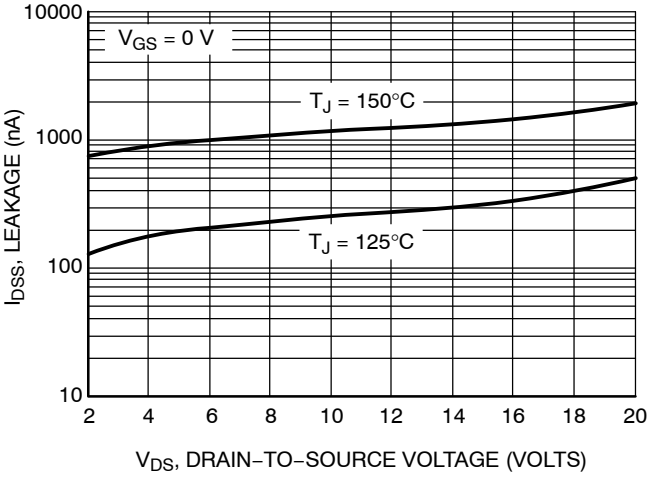



**Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage**

## TYPICAL PERFORMANCE CURVES

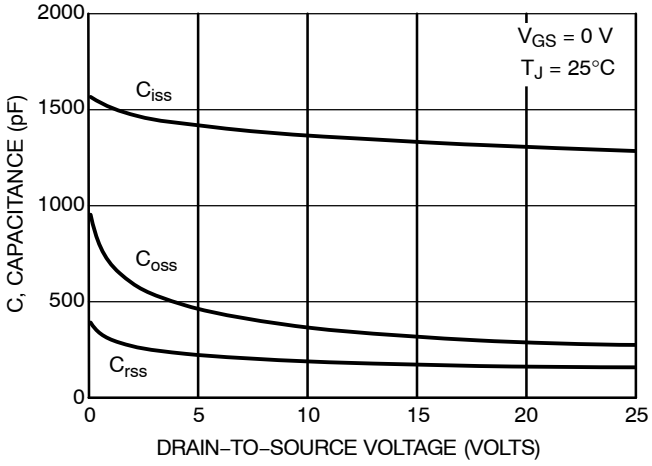



**Figure 7. Capacitance Variation**

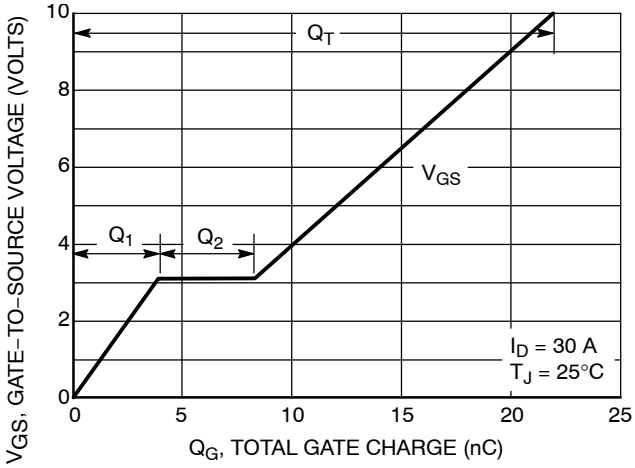



**Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge**

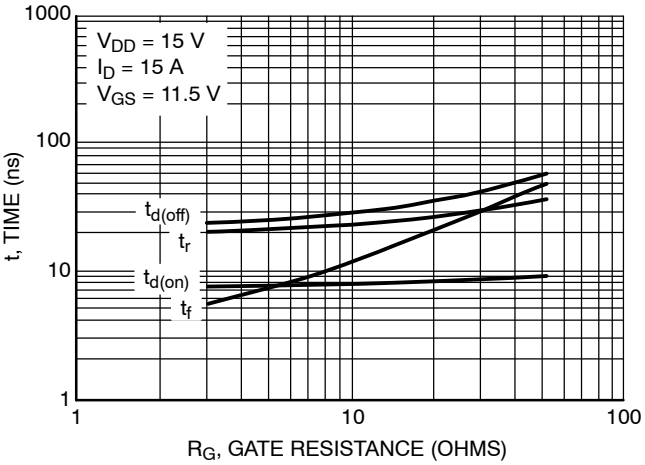



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

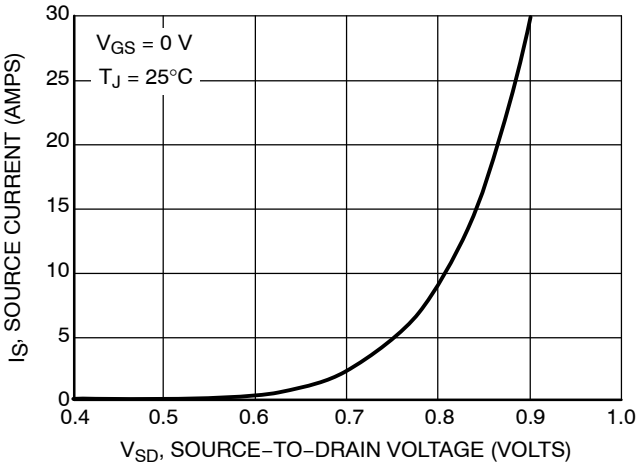



**Figure 10. Diode Forward Voltage vs. Current**

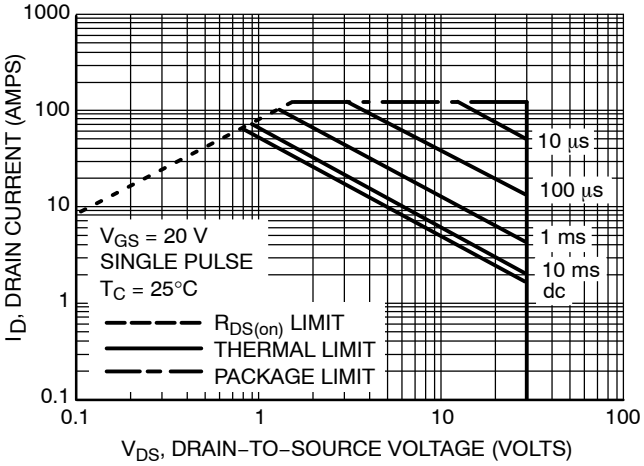



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

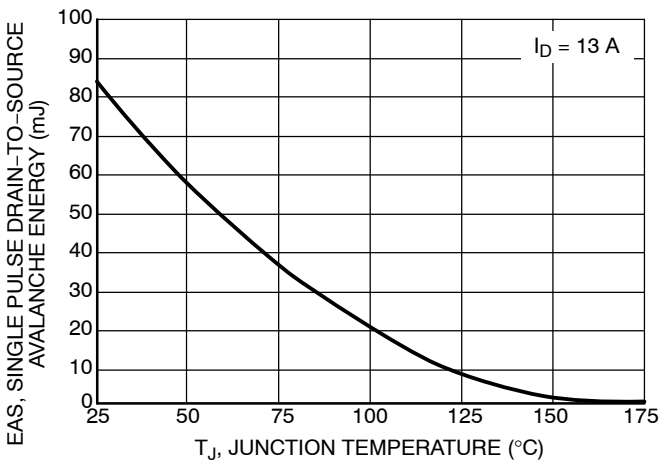
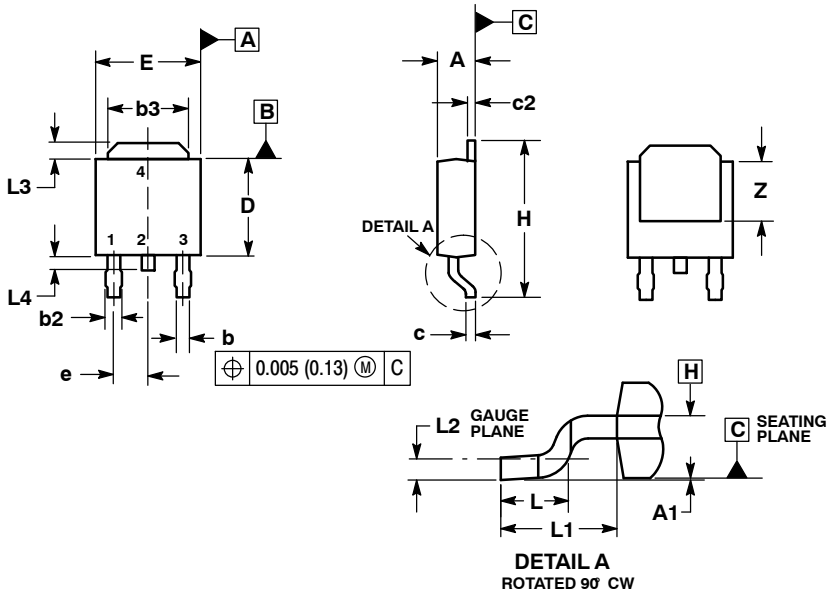



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## PACKAGE DIMENSIONS

**DPAK (SINGLE GUAGE)**
CASE 369AA−01
ISSUE B

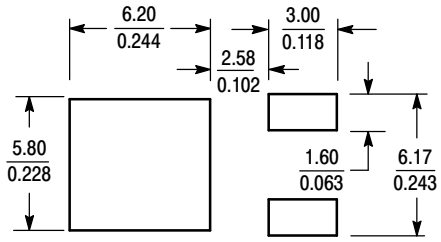



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | −−− | 0.040 | −−− | 1.01 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

### SOLDERING FOOTPRINT*

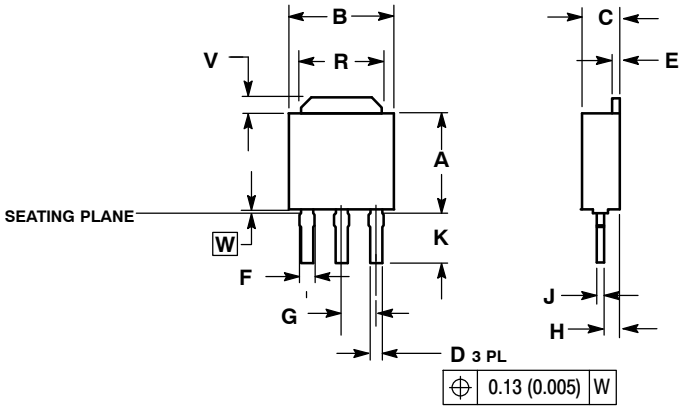



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

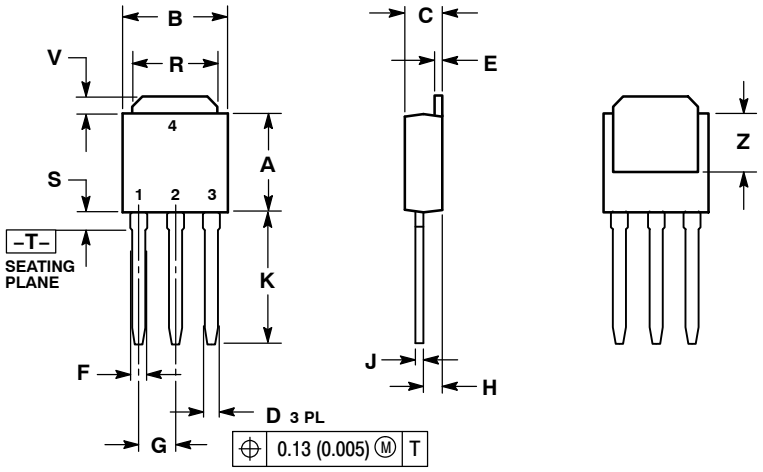
### 3 IPAK, STRAIGHT LEAD
CASE 369AC−01
ISSUE O




NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.043 | 0.94 | 1.09 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.134 | 0.142 | 3.40 | 3.60 |
| R | 0.180 | 0.215 | 4.57 | 5.46 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| W | 0.000 | 0.010 | 0.000 | 0.25 |

### IPAK (STRAIGHT LEAD DPAK)
CASE 369D−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



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