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ISL8274M

30A/30A Dual-Channel Digital PMBus Step-Down Power Module

FN8931
Rev.1.00
Jan 4, 2018

The ISL8274M is a complete PMBus enabled DC/DC, dual-channel, step-down advance power supply, capable of delivering up to 30A per channel and optimized for high power density applications.

Operating across an input voltage range of 4.5V to 14V, the ISL8274M offers adjustable output voltages down to 0.6V and achieves up to 95.5% conversion efficiencies. A unique ChargeMode™ control architecture provides a single clock cycle response to an output load step and can support switching frequencies up to 1.06MHz. The power module integrates all power and most passive components and requires only a few external components to operate. A set of optional external resistors allows the user to easily configure the device for standard operation. For advanced configurations, a standard PMBus interface addresses tasks such as sequencing and fault management, as well as real-time full telemetry and point-of-load monitoring. Additionally, the nonvolatile memory can store the desired custom configuration and settings.

A fully customizable voltage, current, and temperature protection scheme ensures safe operation for the ISL8274M under abnormal operating conditions. The device is also supported by the PowerNavigator™ software, a full digital power train development environment.

The ISL8274M is available in a low profile, compact 18mm x 23mm x 7.5mm fully encapsulated, thermally enhanced HDA package.

Applications

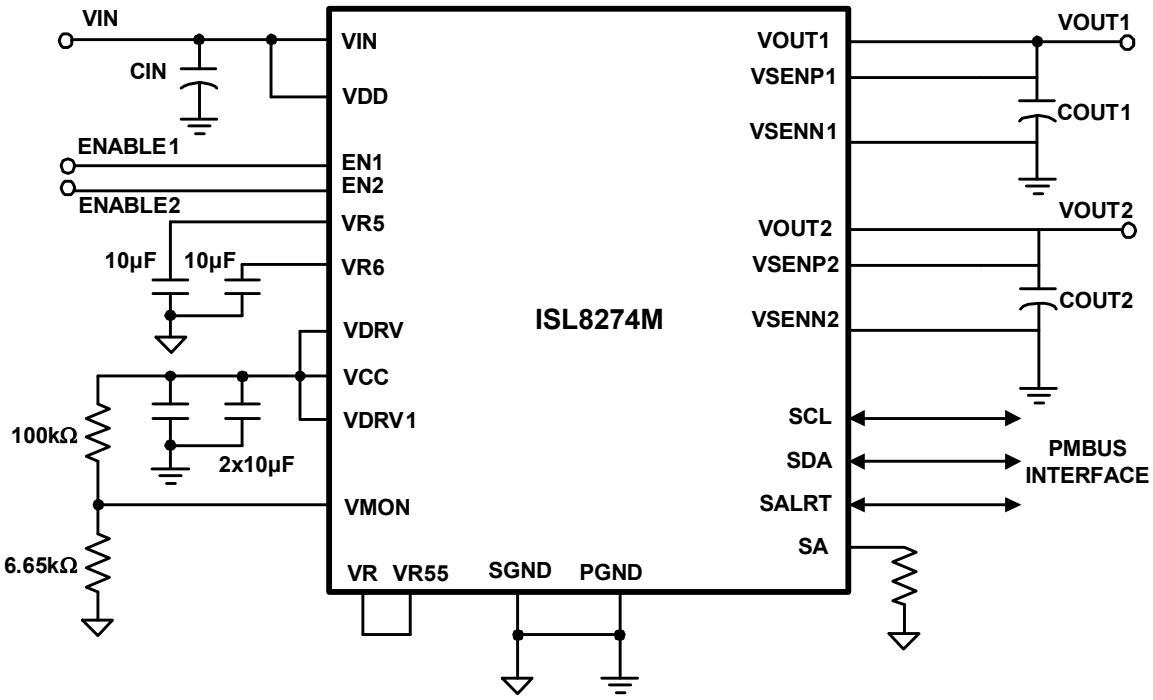
- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Features

- Complete digital power supply
- 30A/30A dual-channel output current
  - 4.5V to 14V single rail input voltage
  - Up to 95.5% efficiency
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - ±1.2% accuracy over line/load/temperature
- ChargeMode control loop architecture
  - 296kHz to 1.06MHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- PMBus interface and/or pin-strap mode
  - Fully programmable through PMBus
  - Pin-strap mode for standard settings
  - Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and f_{SW}
- Advanced soft-start/stop, sequencing, and tracking
- Internal nonvolatile memory
- Complete over/undervoltage, current, and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced 18mm x 23mm x 7.5mm HDA package

Related Literature

- For a full list of related documents, visit our website
  - ISL8274M product page



Note: This figure represents a typical implementation of the ISL8274M. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

Figure 1. Application Circuit

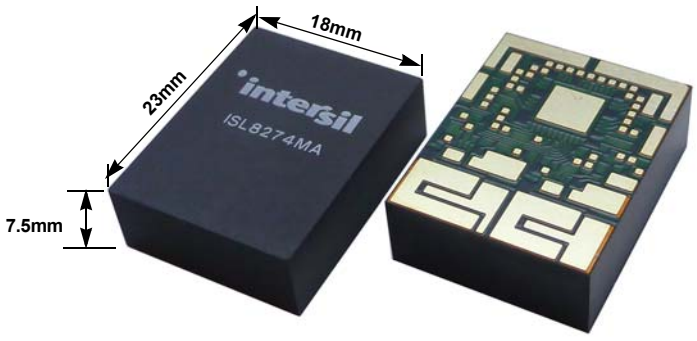
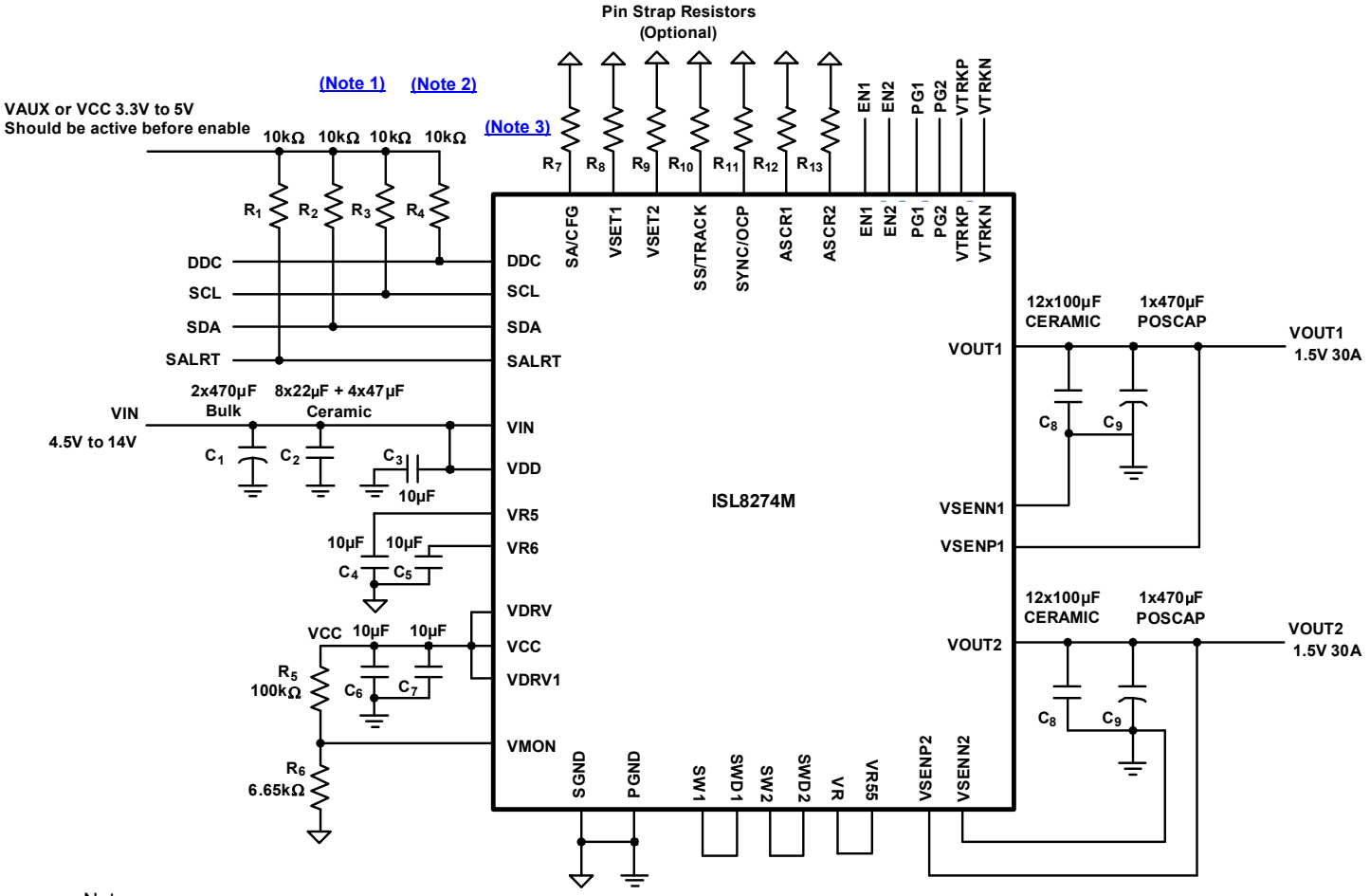


Figure 2. Small Package for High Power Density

Contents

1. Overview

1.1 Typical Application Circuits



Notes:

1. R_2 and R_3 are not required if the PMBus host already has I^2C pull-up resistors.
2. Only one R_4 per DDC bus is required when multiple modules share the same DDC bus.
3. R_7 through R_{13} can be selected according to the tables for the pin-strap resistor setting in this document. If the PMBus configuration is chosen to overwrite the pin-strap configuration, R_8 through R_{13} can be non-populated.
4. V25, VR, and VR55 do not need external capacitors. V25 can be no connection.

Figure 3. ISL8274M Digital PMBus Module Dual 30A/30A Application with Pinstrap Settings

1.2 ISL8274M Internal Block Diagram

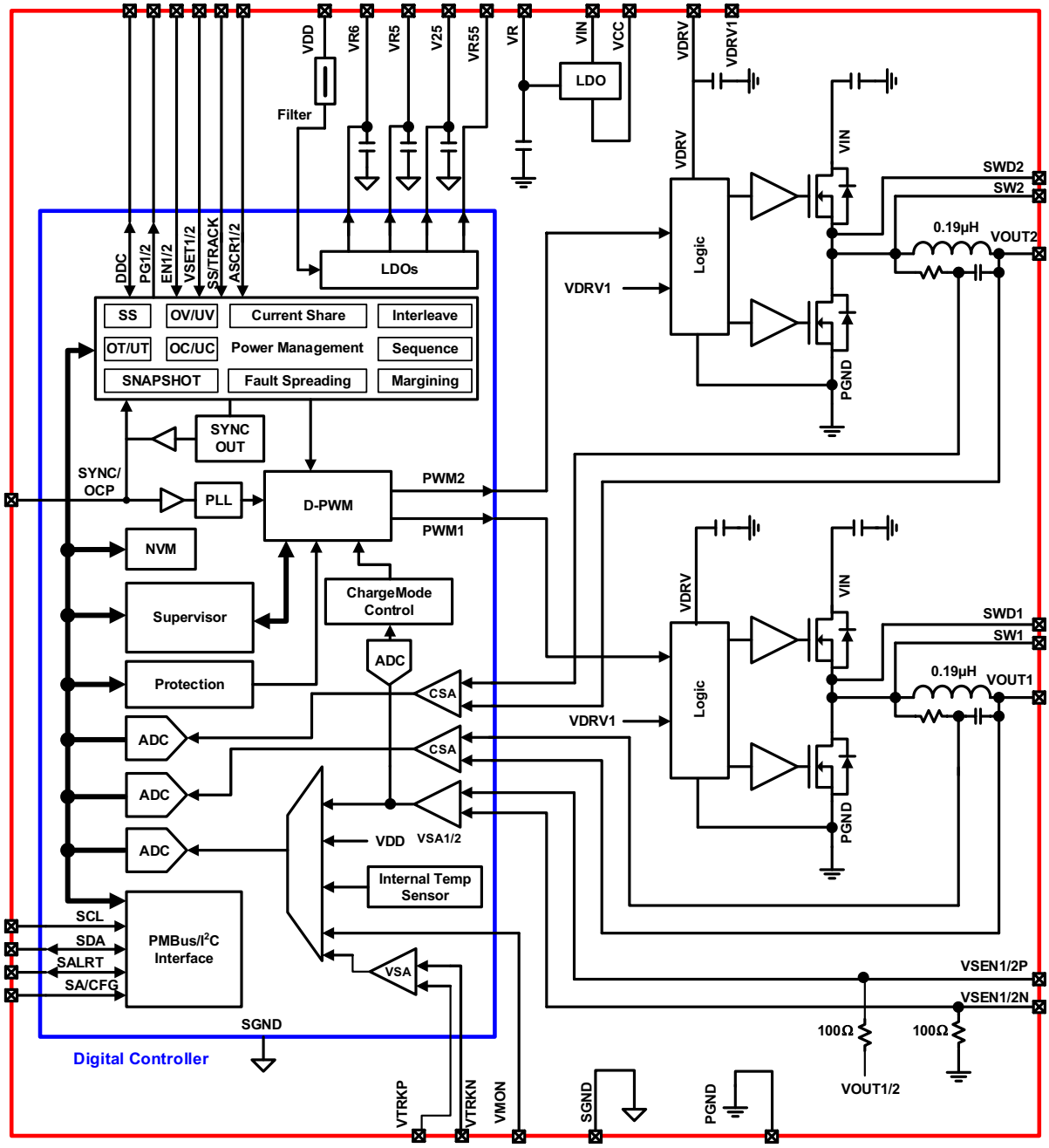


Figure 4. Internal Block Diagram

1.3 Ordering Information

Part Number (Notes 5, 6, 7)	Part Marking	Temp Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8274MAIRZ	ISL8274MA	-40 to +85	58 LD 18x23 HDA Module	Y58.18x23
ISL8274MEVAL1Z	Evaluation Board			

Notes:

5. Add “-T” suffix for 100 unit tape and reel option. Refer to TB347 for details on reel specifications.
6. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
7. For Moisture Sensitivity Level (MSL), see the product information page for the ISL8274M. For more information on MSL, see TB363.

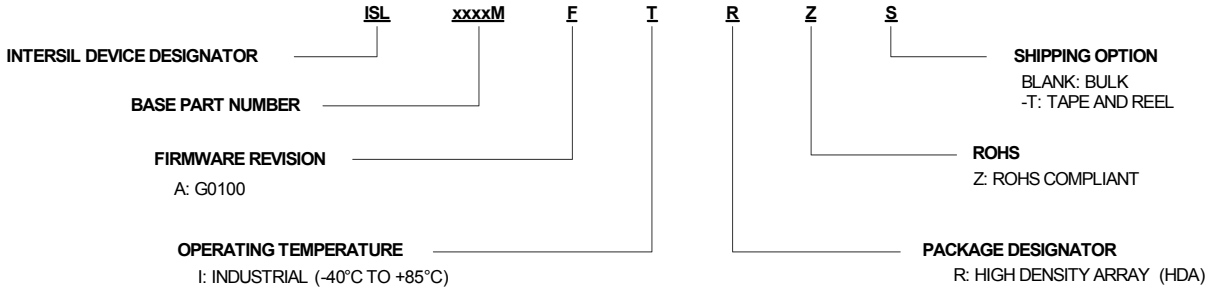
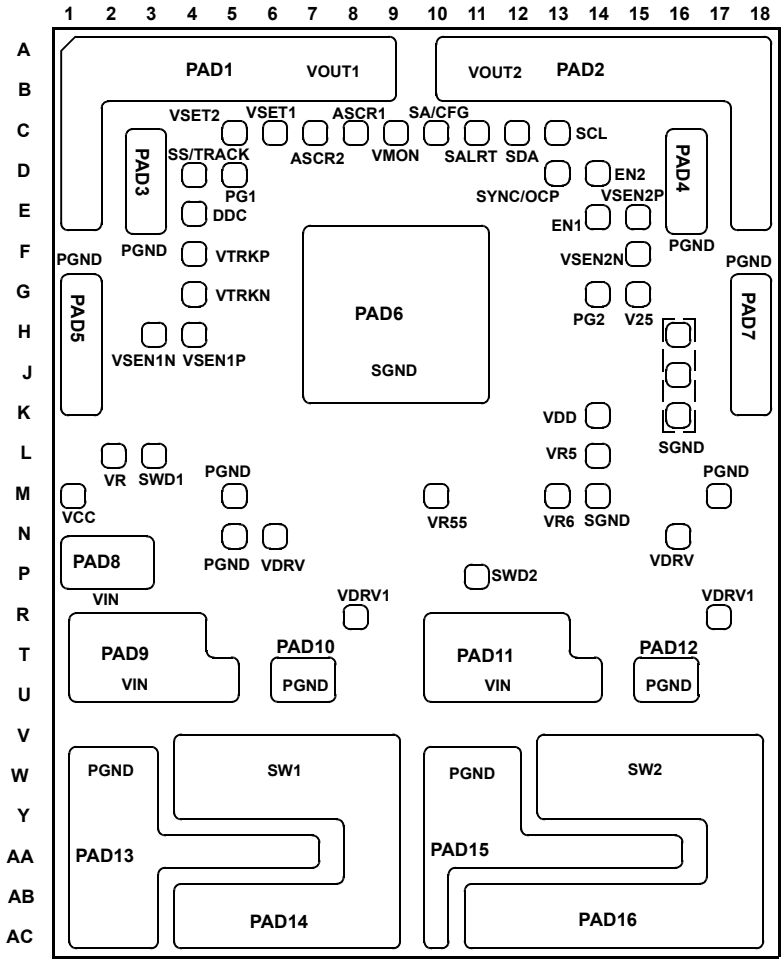


Table 1. Key Differences Between Family of Parts

Part	Description	V_{IN} Range (V)	V_{OUT} Range (V)	I_{OUT} (A)
ISL8274M	Digital DC/DC PMBus Dual Channel 30A/30A Module	4.5 - 14	0.6 - 5.0	30/30
ISL8272M	Digital DC/DC PMBus Single Channel 50A Module	4.5 - 14	0.6 - 5.0	50
ISL8273M	Digital DC/DC PMBus Single Channel 80A Module	4.5 - 14	0.6 - 2.5	80
ZL9024M	Digital DC/DC PMBus Single Channel 33A Module	2.75-4	0.6 - 1.5	33

1.4 Pin Configuration

ISL8274M
(58 Ld HDA)
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Type	Description
PAD1	VOUT1	PWR	Power supply output voltage. Channel 1 provides an output voltage from 0.6V to 5V. Refer to the "Functional Description" on page 21 to set the maximum output current from these pads.
PAD2	VOUT2	PWR	Power supply output voltage. Channel 2 provides an output voltage from 0.6V to 5V. Refer to the "Functional Description" on page 21 to set the maximum output current from these pads.
PAD3, PAD4, PAD5, PAD7, PAD10, PAD12, PAD13, PAD15	PGND	PWR	Power ground. Refer to the "Layout Guide" on page 33 for the PGND pad connections and I/O capacitor placement.
PAD6	SGND	PWR	Signal ground. Refer to "Layout Guide" on page 33 for the SGND pad connections.
PAD8, PAD9, PAD11	VIN	PWR	Input power supply voltage to power the module. Input voltage ranges from 4.5V to 14V.
PAD14	SW1	PWR	Switching node pads for Channel 1. The SW1 pad is used to dissipate the heat and provide the good thermal performance. Refer to "Layout Guide" on page 33 for the SW1 pad connections.
PAD16	SW2	PWR	Switching node pads for Channel 2. The SW2 pad is used to dissipate the heat and provide the good thermal performance. Refer to "Layout Guide" on page 33 for the SW2 pad connections.
C5	VSET2	I	Output voltage selection pin for Channel 2. Used to set VOUT2 set point and VOUT2 max.
C6	VSET1	I	Output voltage selection pin for Channel 1. Used to set VOUT1 set point and VOUT1 max.
C7	ASCR2	I	ChargeMode control ASCR parameters selection pin for Channel 2. Used to set ASCR gain and residual values.
C8	ASCR1	I	ChargeMode control ASCR parameters selection pin for Channel 1. Used to set ASCR gain and residual values.
C9	VMON	I	Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider.
C10	SA/CFG	I	Serial address selection pin. Used to assign unique address for each individual device or to enable certain management features. This pin also sets the UVLO level.
C11	SALRT	O	Serial alert. Connect to external host if desired. SALRT is asserted low upon a warning or a fault event and deasserted when warning or fault is cleared. A pull-up resistor is required.
C12	SDA	I/O	Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required.
C13	SCL	I/O	Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required.
D4	SS/ TRACK	I	Soft-start/stop selection pin. Used to set turn on/off delay and ramp time as well as tracking configuration.
D5	PG1	O	Power-good output for Channel 1. Power-good output can be an open drain that requires a pull-up resistor or push-pull output that can drive a logic input.
D13	SYNC/ OCP	I/O	Clock synchronization input and OCP setting pin. Used to set the frequency of the internal switch clock, to sync to an external clock or to output internal clock. If external synchronization is used, the external clock must be active before enable. Different OCP level can be set with this pin.
D14	EN2	I	Enable pin for Channel 2. Logic high to enable the module output.
E14	EN1	I	Enable pin for Channel 1. Logic high to enable the module output.
E4	DDC	I/O	A Digital-DC bus. This dedicated bus provides the communication between devices for features such as sequencing, fault spreading and current sharing. The DDC pin on all Digital-DC devices should be connected together. A pull-up resistor is required.
E15	VSEN2P	I	Differential output voltage sense feedback for Channel 2. Connect to positive output regulation point.
F4	VTRKP	I	Tracking sense positive input. Used to track an external voltage source.
F15	VSEN2N	I	Differential output voltage sense feedback for Channel 2. Connect to negative output regulation point.

Pin Number	Pin Name	Type	Description
G4	VTRKN	I	Tracking sense negative input (return).
G14	PG2	O	Power-good output for Channel 2. Power-good output can be an open drain that requires a pull-up resistor or push-pull output that can drive a logic input.
G15	V25	PWR	Internal 2.5V reference used to power internal circuitry. No external capacitor required for this pin. Not recommended to power external circuits.
H3	VSEN1N	I	Differential output voltage sense feedback for Channel 1. Connect to a negative output regulation point.
H4	VSEN1P	I	Differential output voltage sense feedback for Channel 1. Connect to a positive output regulation point.
H16, J16, K16, M14	SGND	PWR	Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer.
K14	VDD	PWR	Input supply voltage for controller. Connect VDD pad to VIN supply.
L2	VR	PWR	Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace. Not recommended to power external circuits.
L3	SWD1	PWR	Switching node driving pins for Channel 1. Directly connect to the SW1 pad with short loop wires.
P11	SWD2	PWR	Switching node driving pins for Channel 2. Directly connect to the SW2 pad with short loop wires.
L14	VR5	PWR	Internal 5V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Maximum external loading current is 5mA.
M1	VCC	PWR	Internal LDO output. Connect VCC to VDRV for internal LDO driving.
M5, M17, N5	PGND	PWR	Power grounds. Using multiple vias to connect the PGND pins to the internal PGND layer.
M10	VR55	PWR	Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to the VR pin. Not recommended to power external circuit.
M13	VR6	PWR	Internal 6V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin. Not recommended to power external circuit.
N6, N16	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input application, use external supply or connect this pin to VIN.
R8, R17	VDRV1	I	Bias pin of the internal FET drivers. Always tie to VDRV.

Table 2. ISL8274M Design Guide Matrix and Output Voltage Response

V_{OUT} (V)	I_{OUT} (A)	Avg OCP (A)	COUT_Bulk (µF)	COUT_Ceramic (µF)	ASCR Gain	ASCR Residual	Peak-to-Peak (mV)	Frequency (kHz)
5	25	30	1*470	6*100	275	100	170	1067
5	20	25	1*470	6*100	175	80	150	615
3.3	25	30	1*470	8*100	300	90	150	800
3.3	20	25	1*470	8*100	175	80	140	571
2.5	30	35	1*470	9*100	600	100	110	1067
2.5	25	30	1*470	9*100	350	100	120	615
2.5	20	25	1*470	9*100	175	90	100	471
1.8	30	35	1*470	12*100	600	100	90	889
1.8	25	30	1*470	12*100	250	100	100	421
1.8	20	25	1*470	12*100	200	100	100	364
1.5	30	35	1*470	12*100	525	90	90	889
1.5	25	30	1*470	12*100	250	100	90	421

Table 2. ISL8274M Design Guide Matrix and Output Voltage Response (Continued)

V_{OUT} (V)	I_{OUT} (A)	Avg OCP (A)	COUT_Bulk (µF)	COUT_Ceramic (µF)	ASCR Gain	ASCR Residual	Peak-to-Peak (mV)	Frequency (kHz)
1.5	20	25	1*470	12*100	140	90	100	320
1.2	30	35	1*470	12*100	600	110	70	727
1.2	25	30	4*470	12*100	250	80	60	296
1	30	35	1*470	12*100	450	110	80	615
1	25	30	5*470	12*100	250	80	50	296
0.6	30	35	7*470	12*100	300	90	50	296

Notes:

8. 2x470µF (EEE-1EA471P) and 12x22µF (GRM32ER71E226KE15L) are used for all conditions in the evaluation board.
9. 100µF (GRM31CD80J107ME39L) ceramic and 470µF (6TPF470MAH) are selected for output capacitor in the evaluation board.
10. Peak-to-peak V_{OUT} deviation is measured under 50%-100% load transient while 12V input applied.
11. ASCR gain and residual was designed to achieve 50° phase margin over temperature. (Ambient temperature from -40°C to +85°C).
12. Frequency is selected to achieve the highest efficiency at full load as well as avoid saturation of the inductor. For instance, select 615kHz instead of 296kHz if 1V, 26A is required to avoid inductor saturation. Although better efficiency is obtained at 296kHz supporting 1V, 25A, higher frequency can be selected because less output capacitance is required to meet the transient response specification.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Supply Voltage, VIN Pin	-0.3	17	V
Input Supply Voltage for Controller, VDD Pin	-0.3	17	V
MOSFET Switch Node Voltage, SW1/2, SWD1/2 (Note 13)	-0.3	25	V
MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin	-0.3	6.0	V
Output Voltage, VOUT1/2 Pin	-0.3	6.0	V
Internal Reference Supply Voltage			
VR6 Pin	-0.3	6.6	V
VR, VR5, VR55 Pin	-0.3	6.5	V
V25 Pin	-0.3	3	V
Logic I/O Voltage for DDC, EN1/2, PG1/2, ASCR1/2, SA/CFG, SCL, SDA, SALRT, SYNC/OCP, SS/TRACK, VMON, VSET1/2	-0.3	6.0	V
Analog Input Voltages			
VSEN1P, VSEN2P, VTRKP	-0.3	6.0	V
VSEN1N, VSEN2N, VTRKN	-0.3	0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

Note:
13. Do not apply DC voltage higher than 17V to the pins.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
58 Ld HDA Package (Notes 14, 15)	5.3	1.1

Notes:
14. θ_{JA} is defined by simulation in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers.
15. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+125	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	see Figure 33		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{IN}	4.5	14	V
Input Supply Voltage Range for Controller, V_{DD}	4.5	14	V
Output Voltage Range, V_{OUT}	0.6	5	V
Output Current Range, $I_{OUT(DC)}$ Per Channel (Note 18)	0	30	A
Operating Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Input and Supply Characteristics						
Input Supply Current for Controller	I_{DD}	V_{IN} = V_{DD} = 12V, V_{OUT} = 0V, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
5V Internal Reference Supply	V_{R5}	I_{VR5} < 5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply	V_{25}		**2.25**	2.5	**2.75**	V
Internal LDO Output Voltage	V_{CC}			5.3		V
Internal LDO Output Current	I_{VCC}	V_{IN} = V_{DD} = 12V, V_{CC} connected to VDRV, module enabled	**50**			mA
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Read Back Total Error (Note 19)	$V_{DD\_READ\_ERR}$	PMBus Read		±2		% FS
Output Characteristics						
Output Voltage Adjustment Range	V_{OUT_RANGE}		**0.54**		**5.5**	V
Output Voltage Set-Point Resolution	V_{OUT_RES}	Configured using PMBus		±0.025		%V_{OUT}
Output Voltage Set-Point Accuracy (Notes 17, 19)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ T_A ≤ +85°C)	**-1.2**		**1.2**	%
Output Voltage Read Back Resolution	$V_{OUT\_READ\_RES}$			±0.15		% FS
Output Voltage Read Back Total Error (Note 19)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**2**	% FS
Output Ripple Voltage	V_{OUT_RIPPLE}	V_{OUT} = 1.5V, C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF ceramic		1		%
Output Current Read Back Resolution	$I_{OUT\_READ\_RES}$	ISENSE_CONFIG default setting		0.2		A
Output Current Range (Note 18)	I_{OUT_RANGE}	Per channel			**30**	A
Output Current Read Back Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load V_{OUT} = 1.5V		±3		A
Soft-Start and Sequencing						
Delay Time from Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using PMBus	**2**		**300**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using PMBus	**0.5**		**120**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs
Delay Time from Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using PMBus	**2**		**300**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Output Voltage Fall Time	t_{OFF_FALL}	Configured using PMBus	**0.5**		**120**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
Power-Good						
Power-Good Delay	V_{PG_DELAY}	Configured using PMBus	**0**		**5000**	ms
Temperature Sense						
Temperature Sense Range	T_{SENSE_RANGE}	Configurable using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	-5		5	°C
Fault Protection						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 19)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 17)	V_{OUT_OV/UV_ACCY}		**-2**		**2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 19)	I_{LIMIT_ACCY}	Tested at IOUT_AVG_OC_FAULT_LIMIT = 35A		±10		% FS
Over-temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		115		°C
		Configured using PMBus	**-40**		**115**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C
Oscillator and Switching Characteristics						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC clock equal to 500kHz is not supported	**-10**		**10**	%

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 16)	Typ	Max (Note 16)	Unit
Logic Input/Output Characteristics						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	DDC, EN1/2, PG1/2, SA/CFG, SCL, SDA, ASCR1/2, SS/TRACK, SALRT, SYNC/OCP, V_{MON}, $V_{SET1/2}$	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus Interface Timing Characteristic						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

Notes:

16. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design. Controller is independently tested before module assembly.
17. V_{OUT} measured at the termination of the VSEN1/2P and VSEN1/2N sense points.
18. The MAX load current is determined by the thermal "Derating Curves" on page 20.
19. "FS" stands for full scale of recommended maximum operation range.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10.

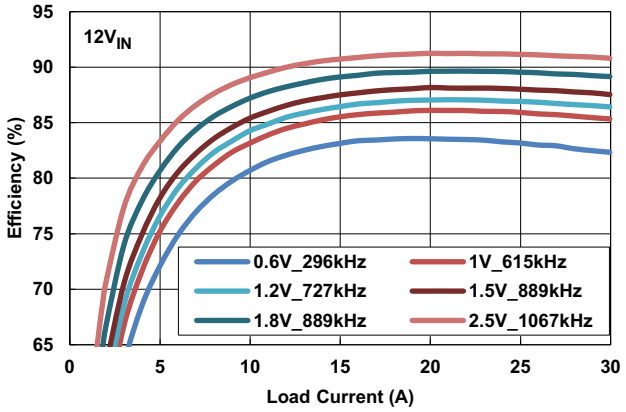


Figure 5. Single Channel Efficiency vs Output Current

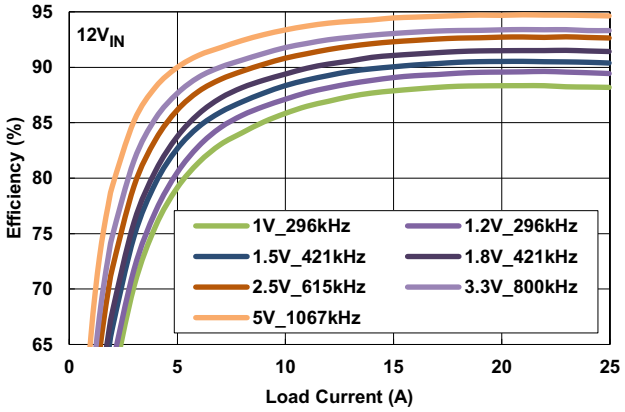


Figure 6. Single Channel Efficiency vs Output Current

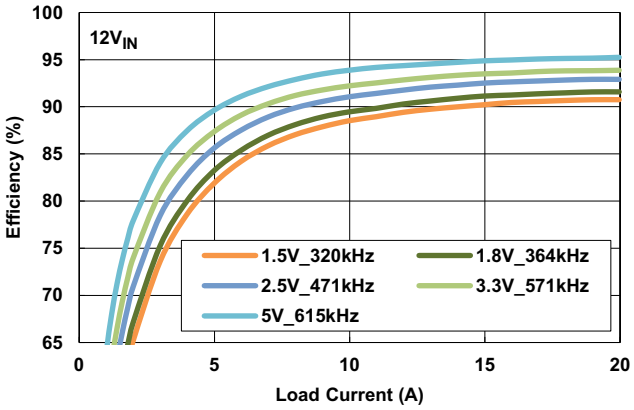


Figure 7. Single Channel Efficiency vs Output Current

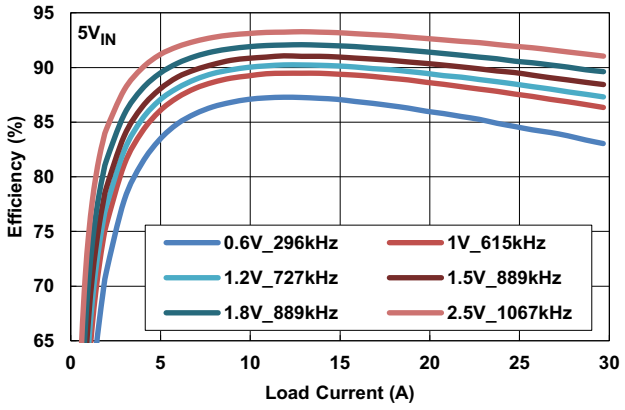


Figure 8. Single Channel Efficiency vs Output Current

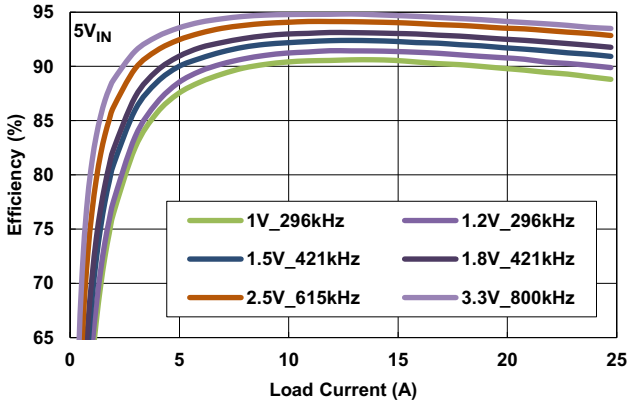


Figure 9. Single Channel Efficiency vs Output Current

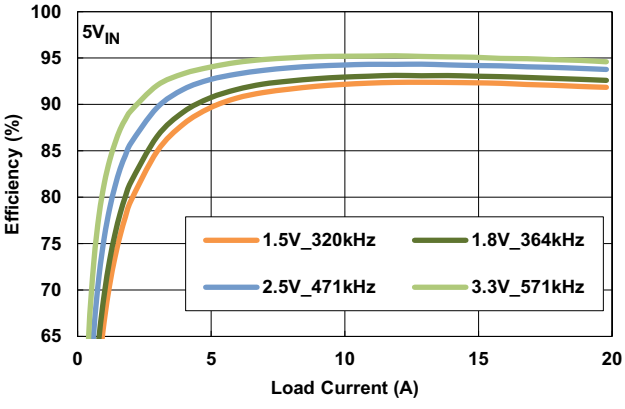


Figure 10. Single Channel Efficiency vs Output Current

3.2 Startup and Shutdown

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted.

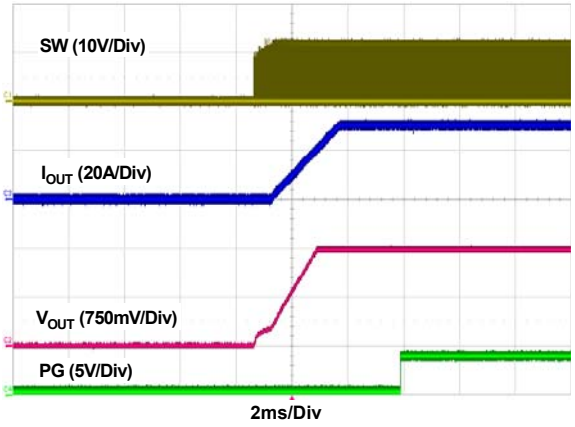


Figure 11. Single Channel Startup $12V_{IN}$, $1.5V_{OUT}$, 30A

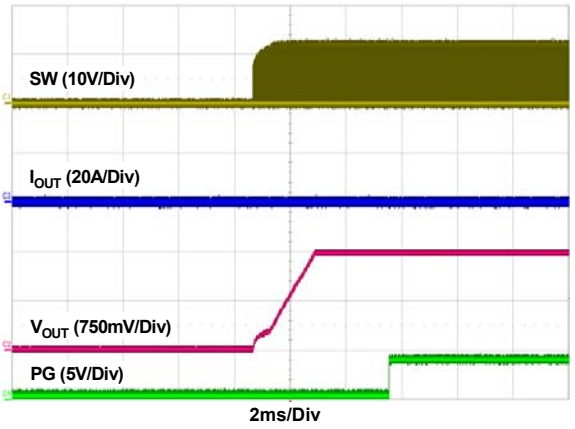


Figure 12. Single Channel Startup $12V_{IN}$, $1.5V_{OUT}$, 0A

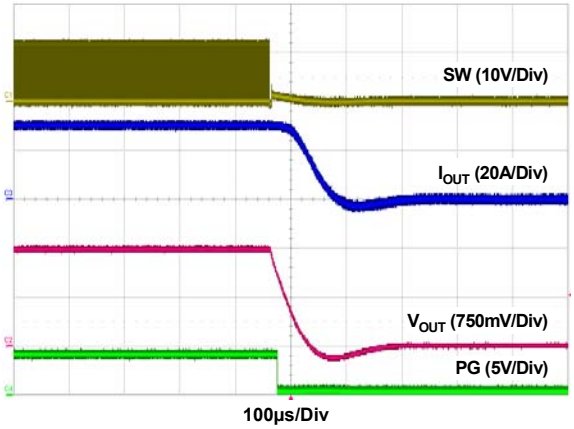


Figure 13. Single Channel Shutdown $12V_{IN}$, $1.5V_{OUT}$, 30A

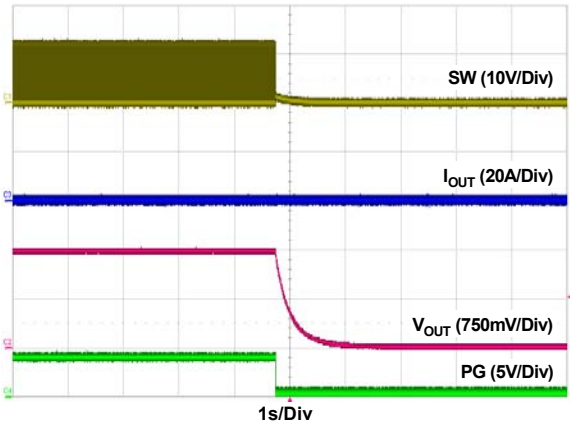


Figure 14. Single Channel Shutdown $12V_{IN}$, $1.5V_{OUT}$, 0A

3.3 Derating Curves

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10. Load current is applied per channel, two channels are operating at the same time.

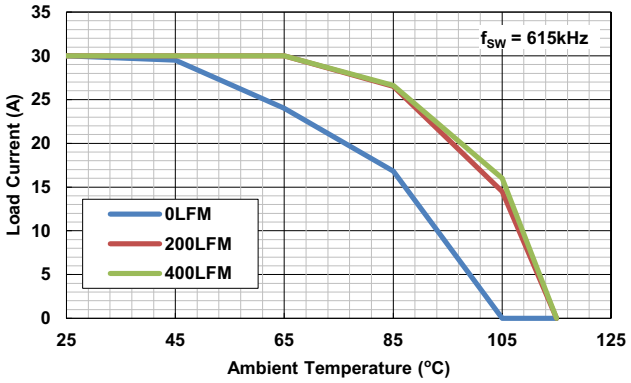


Figure 15. $12V_{IN}$ to $1V_{OUT}$

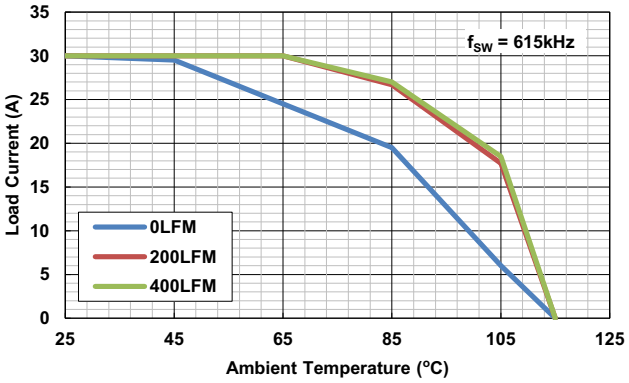


Figure 16. $5V_{IN}$ to $1V_{OUT}$

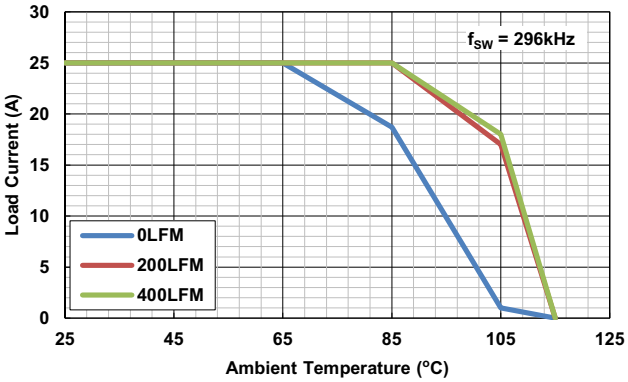


Figure 17. $12V_{IN}$ to $1V_{OUT}$

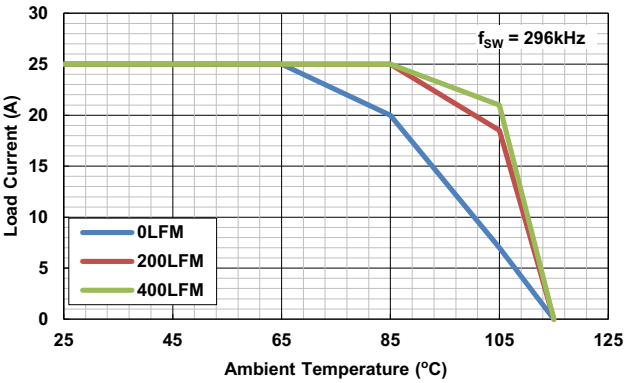


Figure 18. $5V_{IN}$ to $1V_{OUT}$

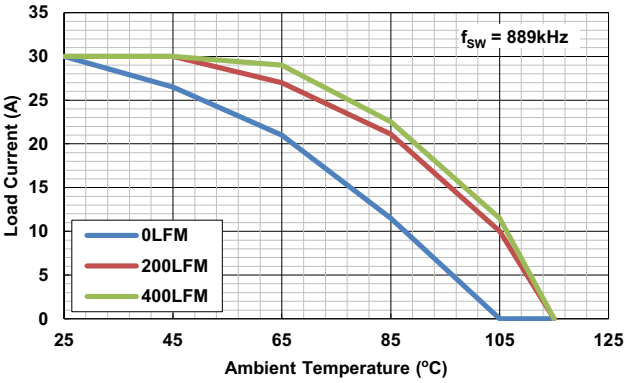


Figure 19. $12V_{IN}$ to $1.5V_{OUT}$

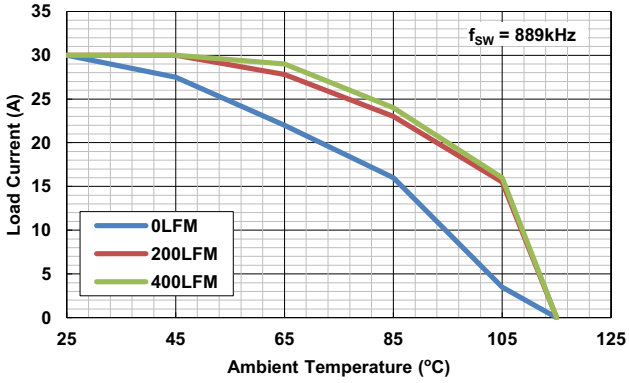


Figure 20. $5V_{IN}$ to $1.5V_{OUT}$

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 2 on page 10. Load current is applied per channel, two channels are operating at the same time. **(Continued)**

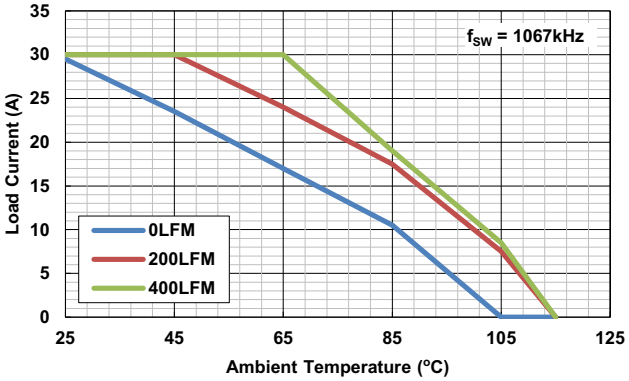


Figure 21. $12V_{IN}$ to $2.5V_{OUT}$

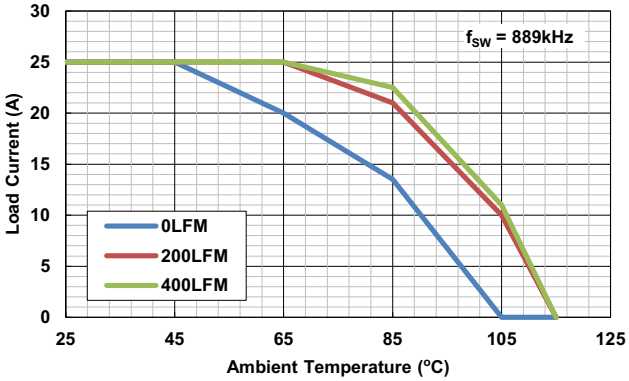


Figure 22. $5V_{IN}$ to $2.5V_{OUT}$

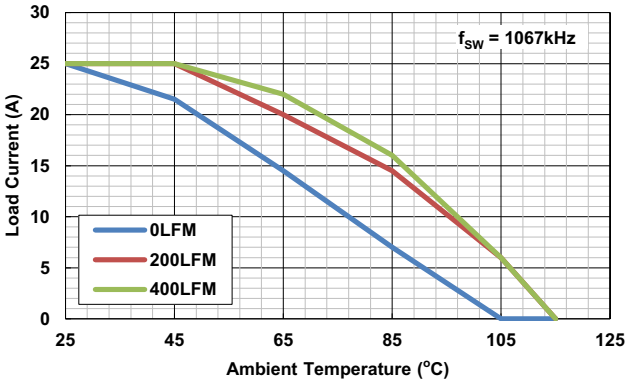


Figure 23. $12V_{IN}$ to $5V_{OUT}$

3.4 Transient Response Performance

Operating condition: T_A = +25°C, no air flow. Refer to Table 2 on page 10 for output capacitor and ASCR settings. Typical values are used unless otherwise noted.

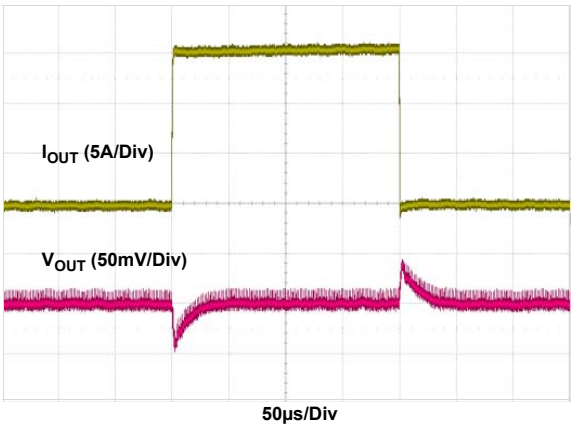


Figure 24. 0A-15A, >10A/µs, $12V_{IN}$,$1V_{OUT}$, 615kHz

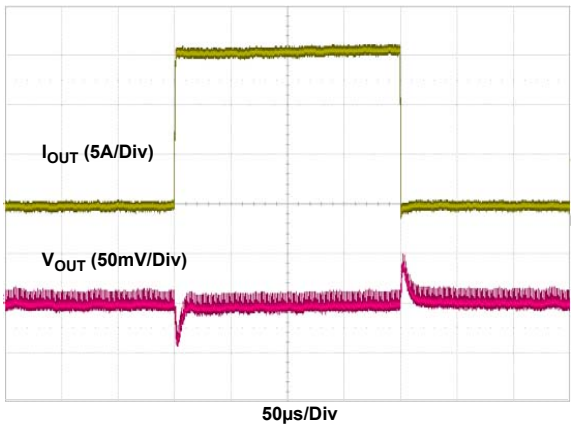


Figure 25. 0A-15A, >10A/µs, $12V_{IN}$,$1.5V_{OUT}$, 889kHz

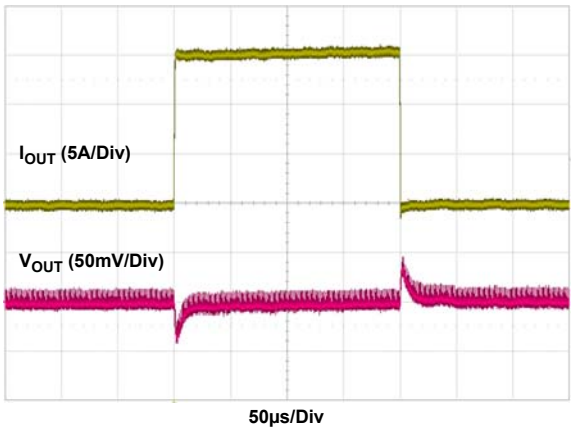


Figure 26. 0A-15A, >10A/µs, $12V_{IN}$,$1.8V_{OUT}$, 889kHz

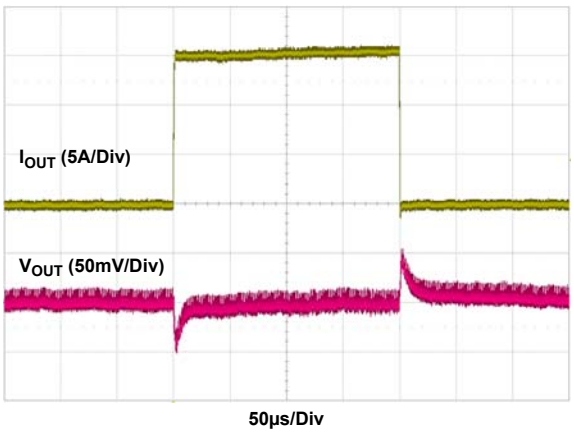


Figure 27. 0A-15A, >10A/µs, $12V_{IN}$, $2.5V_{OUT}$, 1067kHz

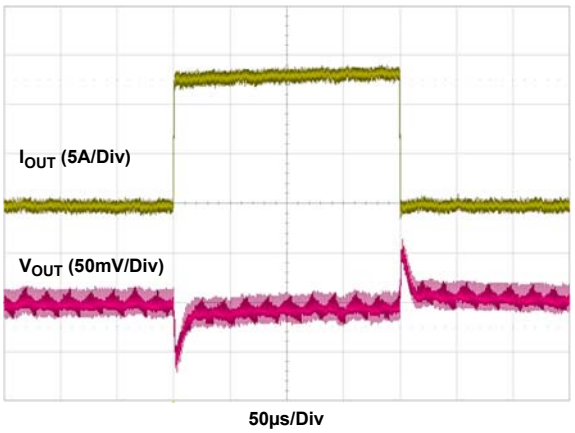


Figure 28. 0A-12.5A, >10A/µs, $12V_{IN}$, $3.3V_{OUT}$, 800kHz

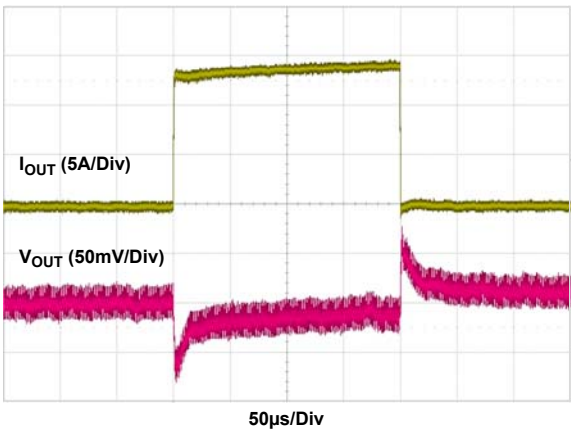


Figure 29. 0A-12.5A, >10A/µs, $12V_{IN}$, $5V_{OUT}$, 1067kHz

4. Functional Description

4.1 SMBus Communications

The ISL8274M provides a PMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ISL8274M can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The ISL8274M accepts most standard PMBus commands. When configuring the device using PMBus commands, it is recommended that the enable pin is tied to SGND.

The SMBus device address is the only parameter that must be set by the external pins. All other device parameters can be set using PMBus commands.

The ISL8274M can operate without the PMBus in pin-strap mode with configurations programmed by pin-strap resistors, such as output voltage, ASCR setting, switching frequency, OCP limit, device SMBus address, input UVLO, soft-start/stop, and tracking.

4.2 Output Voltage Selection

The output voltages of both channels may be set to a voltage between 0.6V and 5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET1/2 pins are used to set the output voltage VOUT1/2 to levels as shown in Table 3. The RSET1/2 resistor is placed between the VSET1/2 pins and SGND. A standard 1% resistor is required.

Table 3. Output Voltage Resistor Settings

VOUT1/2 (V)	RSET1/2 (kΩ)
1	LOW
1.5	OPEN
3.3	HIGH
0.6	10
0.675	11
0.7	12.1
0.72	13.3
0.75	14.7
0.8	16.2
0.85	17.8
0.9	19.6
0.93	21.5
0.95	23.7
0.98	26.1
1.03	28.7
1.05	31.6
1.1	34.8
1.12	38.3
1.15	42.2
1.2	46.4
1.25	51.1
1.3	56.2
1.35	61.9

Table 3. Output Voltage Resistor Settings (Continued)

VOUT1/2 (V)	RSET1/2 (kΩ)
1.4	68.1
1.65	75
1.8	82.5
1.85	90.9
2	100
2.4	110
2.5	121
2.8	133
3	147
3.6	162
5	178

The output voltage may also be set to any value between 0.6V and 5V using the PMBus command VOUT_COMMAND. This device supports dynamic voltage scaling by allowing change to the output voltage set point during regulation. The voltage transition rate is specified by the PMBus command VOUT_TRANSITION_RATE.

By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 5.5V by the PMBus Command VOUT_MAX.

4.3 Soft-Start, Stop Delay, and Ramp Times

The ISL8274M follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. Once this process is completed, the device is ready to accept commands through the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL8274M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp-up time can be programmed to custom values using the PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 2ms to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay and ramp down time for soft-stop/off can be programmed using the PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” using the command ON_OFF_CONFIG, so that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/TRACK pin can be used to program the soft-start/stop delay time and ramp time to some typical values as well as enable/disable the tracking function shown in Table 4 on page 23.

Table 4. Soft-Start/Stop and Tracking Resistor Settings

TON_DELAY TOFF_DELAY (ms)		TON_RISE TOFF_FALL (ms)		Tracking		
Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	R (kΩ)
5	5	2	2	No	No	LOW
5	5	2	5	No	No	OPEN
5	5	5	2	No	No	HIGH
5	5	5	5	No	No	10
5	10	2	2	No	No	11
5	10	2	5	No	No	12.1
5	10	5	2	No	No	13.3
5	10	5	5	No	No	14.7
10	5	2	2	No	No	16.2
10	5	2	5	No	No	17.8
10	5	5	2	No	No	19.6
10	5	5	5	No	No	21.5
20	5	2	2	No	No	23.7
20	5	5	5	No	No	26.1
5	20	2	2	No	No	28.7
5	20	2	5	No	No	31.6
5	20	5	2	No	No	34.8
5	20	5	5	No	No	38.3
5	N/A	2	N/A	No	Track 100%	42.2
5	N/A	2	N/A	No	Track 50%	46.4
5	N/A	5	N/A	No	Track 100%	51.1
5	N/A	5	N/A	No	Track 50%	56.2
10	N/A	2	N/A	No	Track 100%	61.9
10	N/A	2	N/A	No	Track 50%	68.1
10	N/A	5	N/A	No	Track 100%	75
10	N/A	5	N/A	No	Track 50%	82.5
N/A	5	N/A	2	Track 100%	No	90.9
N/A	5	N/A	2	Track 50%	No	100
N/A	5	N/A	5	Track 100%	No	110
N/A	5	N/A	5	Track 50%	No	121
N/A	10	N/A	2	Track 100%	No	133
N/A	10	N/A	2	Track 50%	No	147
N/A	10	N/A	5	Track 100%	No	162
N/A	10	N/A	5	Track 50%	No	178

4.4 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore, the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ISL8274M integrates a tracking scheme that allows one of its outputs (Channel 1 or Channel 2) to track a voltage that is applied to the VTRKP and VTRKN pins with no external components required. The VTRKP and VTRKN pins are analog inputs that, when the tracking mode is enabled, configure the voltage applied to the VTRKP and VTRKN pins to act as a reference for the device's output regulation.

Figure 30 illustrates the typical connection and the two tracking modes:

- **Coincident** - This mode configures the ISL8274M to ramp its output voltage at the same rate as the voltage applied to the VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.
- **Ratio-metric** - This mode configures the ISL8274M to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRKP and VTRKN pins. The default setting is 50%, but an external resistor string can be used to configure a different tracking ratio. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.

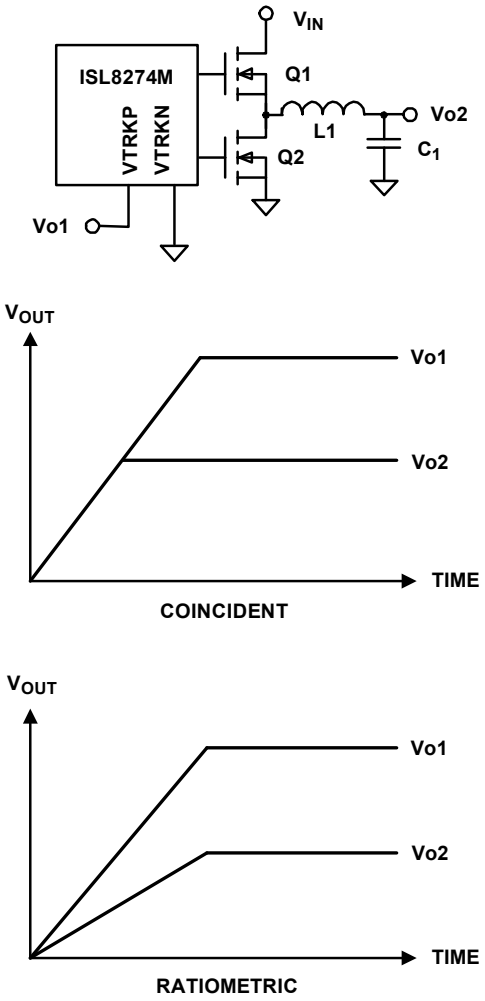


Figure 30. Tracking Modes

The master ISL8274M device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. The maximum tracking rise time is 1V/ms. The slave device must be enabled before the master. Any device that is configured for tracking mode will ignore its TON_DELAY and TON_RISE settings and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRKP and VTRKN pins. Tracking mode can be configured by using the TRACK_CONFIG command.

The VOUT_COMMAND needs to be set the same as the target tracking voltage when tracking is enabled. For example, the VOUT_COMMAND of the Page1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 100% is selected and a ramp of 1V is applied to VTRKP and VTRKN. The VOUT_COMMAND of Page 1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 50% is selected and a ramp of 2V is applied to VTRKP and VTRKN. In Tracking mode, the minimum voltage that can be tracked is ~200mV.

4.5 Power-Good

The ISL8274M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit may be changed using the PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the ISL8274M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A PG delay can be programmed using the PMBus command POWER_GOOD_DELAY.

4.6 Switching Frequency and PLL

The device's switching frequency is set from 296kHz to 1067kHz using the pin-strap method (combined with the average OCP limit setting) as shown in Table 5, or by using the PMBus command FREQUENCY_SWITCH. The ISL8274M incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. It is recommended that when using an external clock, the same frequency should be set in the FREQUENCY_SWITCH command. If the external clock is lost, the module will automatically switch to the internal clock. When using the internal oscillator, the SYNC pin can be configured as a clock source and as an external sync to other modules. Refer to "SYNC_CONFIG (E9h)" on page 67 for more information.

Table 5. Switching Frequency and OCP Limit Resistor Setting

SYNC/OCP		OCP Avg	
R (kΩ)	**Fsw (KHz)**	**Ch1 (A)**	**Ch2 (A)**
LOW	296	35	35
OPEN	889	35	35
HIGH	1067	35	35
10	296	30	35
11	296	30	30
12.1	296	25	35
13.3	296	25	30
14.7	296	25	25
16.2	320	25	35
17.8	320	25	30
19.6	320	25	25
21.5	320	20	30
23.7	320	20	25
26.1	364	25	35